Development of the Timepix4 chip

on behalf of the Medipix4 collaboration (https://medipix.web.cern.ch/)

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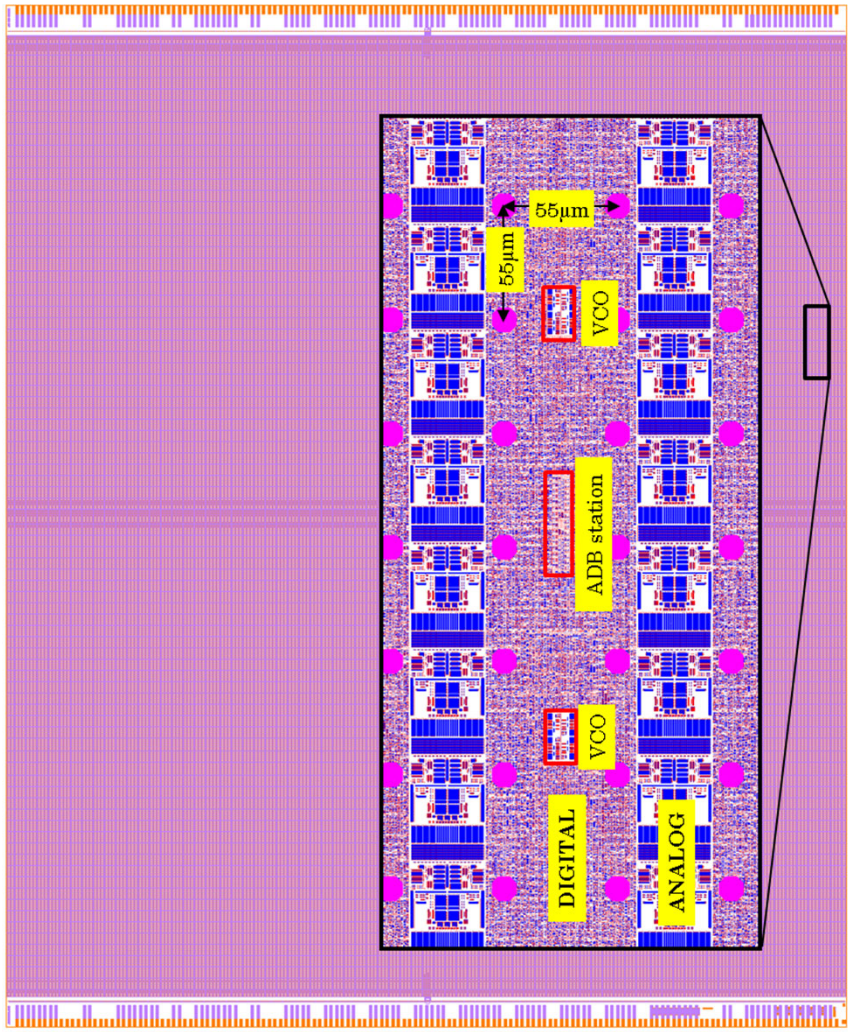
- introduction and main features of the Timepix4 chip
- the circuit design aspects
- applications opportunities
- experimental results
- summary

introduction

Timepix4: Readout ASIC for hybrid pixel detectors

Single hit (electrical signal) pixel-level processor



Features of the Timepix4 chip

technology			TSMC 65nm - 10 metal
pixel size			55 x 55 µm
chip arrangement			**4-side buttable** 3x "hidden" periphery TSV I/O pixel matrix: 512 x 448
sensitive area			**6.94 cm²**
interface			3x 147 I/O TSV / Wirebond
Readout Modes	**Tracking** (data driven)	mode	**ToT & ToA**
		data	64-bit per hit
		max hit rate	3.58×10^6 hits/mm²/s (10.8 KHz / pixel)
	Imaging (frame-based)	Mode	**CRW: Pixel Counter** (8 /16-bit)
		frame rate	up to 89kFPS
		max hit rate	~ 5×10^9 hits/mm²/s
Energy resolution @ Si sensor			~ 1keV FWHM
ENC @ Cin = 75fF			80e⁻ rms
minimum threshold			~ 500 e⁻
hit arrival timing (ToA)			**LSB=195ps,** range: 1.638ms
charge measurement (ToT)			accuracy: 80e⁻ rms, range:200ke⁻
data readout bandwidth			≤163.84 Gbps (16x @ **10.24 Gbps**)
Power Supply Voltage			1.2V
Power			~3.5W

➢ **Timepix4 is a fully digitally-controlled, 4-side tillable large-area, single threshold pixel readout chip with improved energy and time resolution and with high-rate imaging capabilities**

Particle identification and tracking
Photon (hit) detection time-resolved & energy-resolved :

- High-Energy Physics (HEP):
  - very high rate pixel telescope
  - ultra-fast sensor studies for HL-LHC)
  - beam gas interaction (PS SPS/LHC)
  - ATLAS background rad monitor and TRD detector
  - large area gas-filled TPC for ILC)

- Time-of-flight mass spectrometry
- Neutron time-of-flight imaging
- Radiation monitors
- Electron microscopy
- X-ray and powder diffraction
- Compton camera for medical diagnostics
- Gamma and neutron imaging for nuclear industry and Homeland Security

Imaging applications:

- X-ray imaging in synchrotrons with extreme high rates > 10^9 particles/mm^2/s

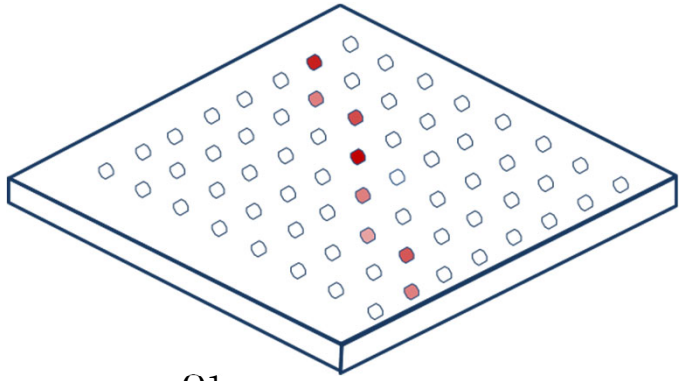
20th Anniversary Symposium on Medipix and Timepix
https://indico.cern.ch/event/782801/

- **Timepix4 a multi-application device is not fully optimized for a particular application**

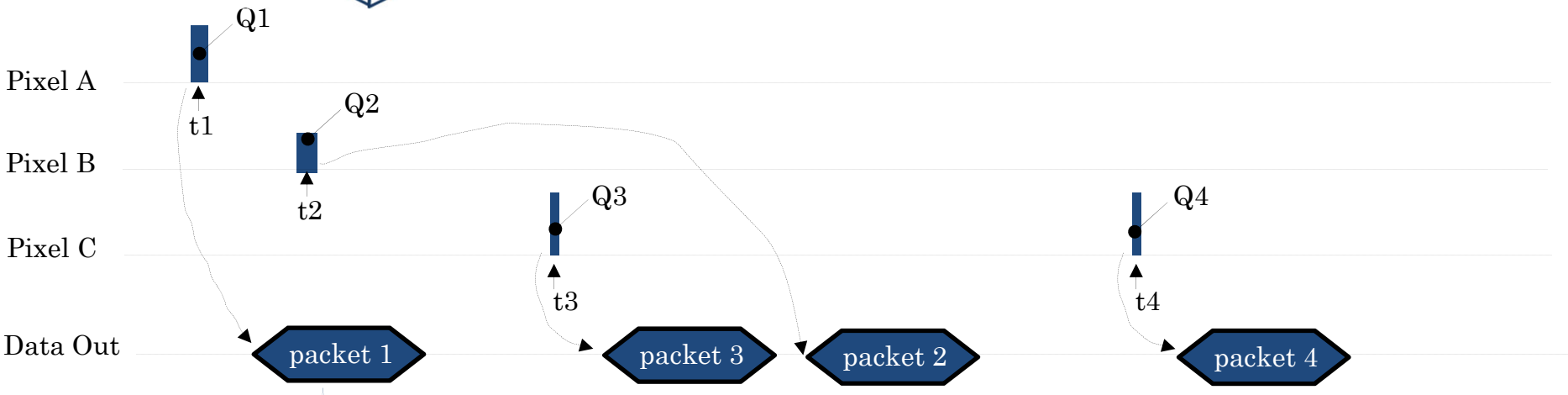
main features

Tracking readout mode: particle track detection / energy-resolved and time-resolved photon (hit) detection

Sparsely distributed hits: zero data-suppressed, continuous, Data-Driven readout



output bandwidth max / min	hit rate	
	per pixel	per mm^2
163 Gbps	10.8 KHz	3.58 MHz
40 Mbps	2.6 Hz	860 Hz



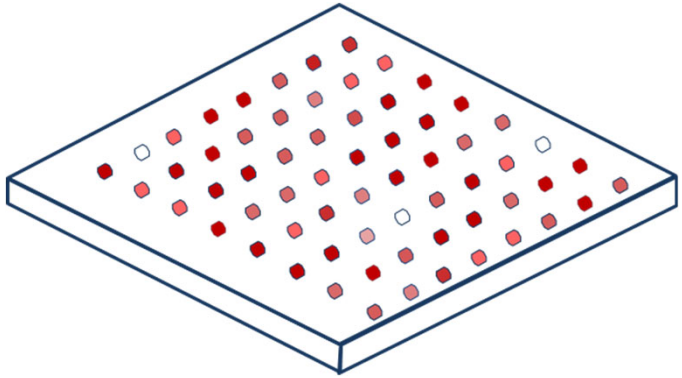
Data Packet <63:0> = pixel address <63:46>, timing data ToA <45:17>, charge(energy) data ToT < 16:1>, Pileup <0:0>

- **the data packet is created and read out immediately after the hit occurred**
- **the bandwidth of the data readout system can be adjusted to match the hit rate**
- **the hit charge info (ToT) can also be used for the correction of the time info (ToA)**

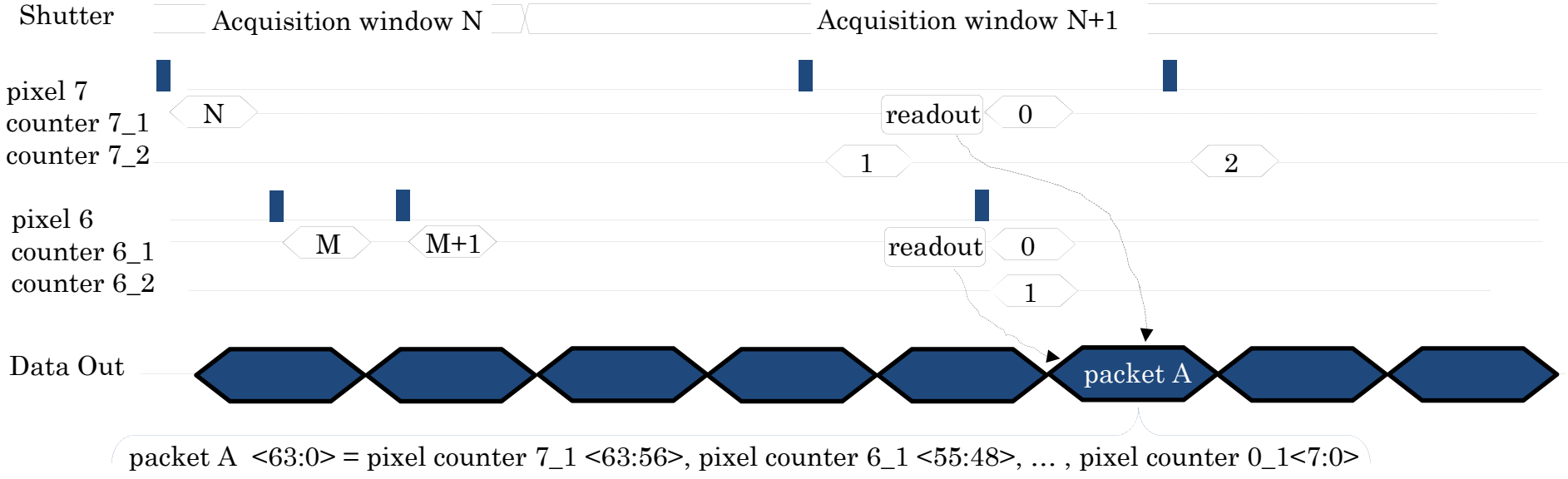
Imaging readout mode : on-pixel hit counting

Continuously distributed hits: full frame readout with continuous read-write (CRW)

- NO zero data suppression
- 8-bit or 16-bit pixel counter depth



output bandwidth max / min	Frame rate		hit rate per mm^2
	8-bit counter	16-bit counter	
163 Gbps	89 KHz	45 KHz	up to 5 GHz
40 Mbps	21 Hz	11 Hz	



- **continuous data taking and pixel matrix readout with two hit counters per pixel**
- **the on-pixel hit counter is read out regularly once per frame**

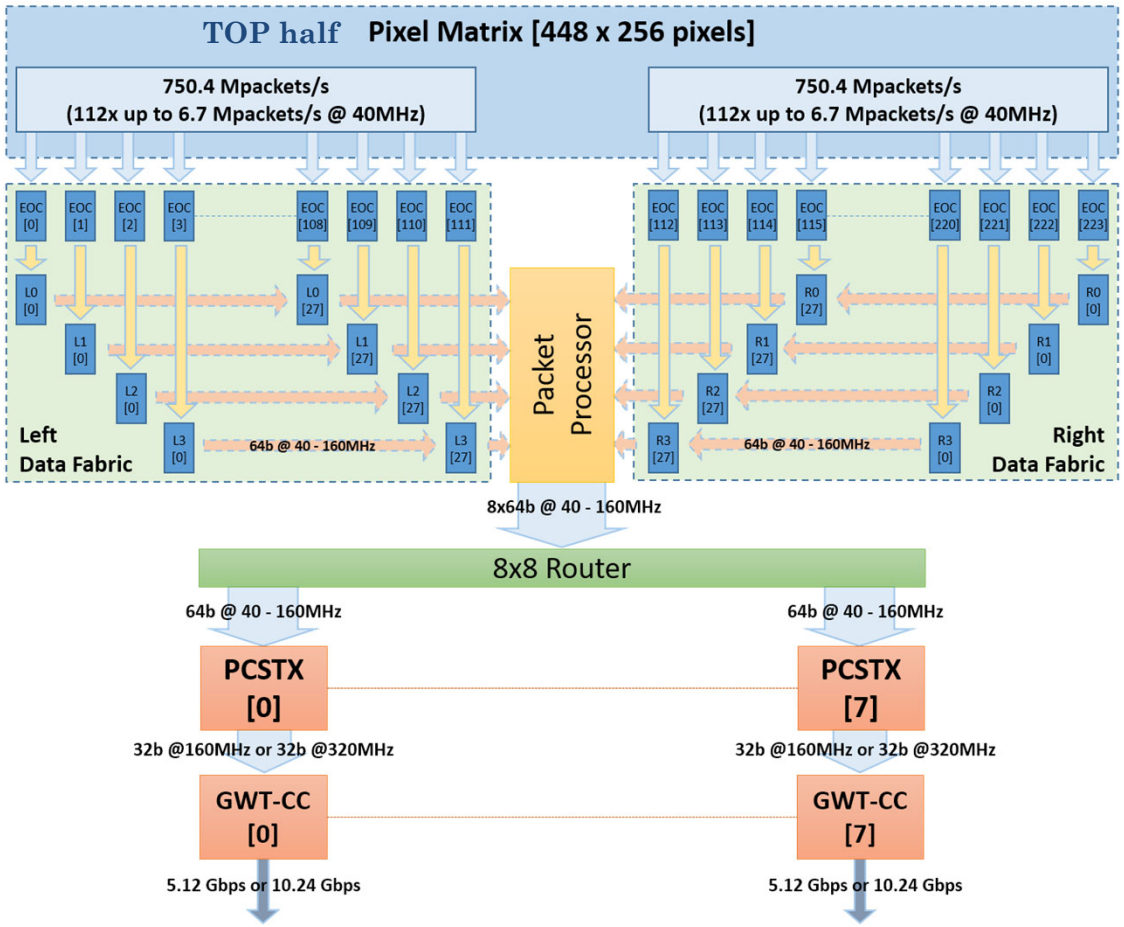
High-volume and high-speed data readout

Data transport architecture

Pixel Matrix → End-of-Column
max bandwidth **: 95.6 Gbps**

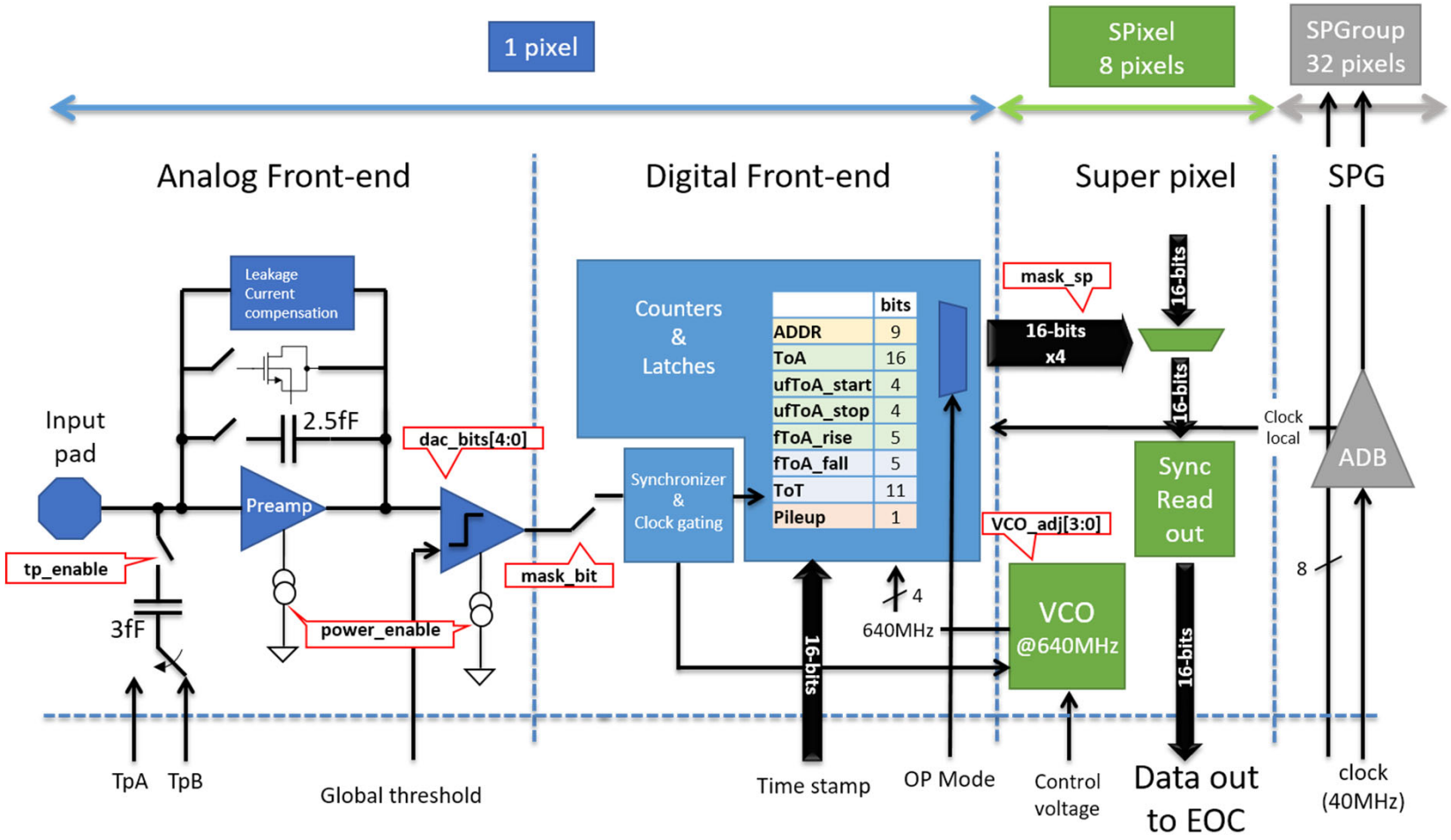
End-of-Column → End-of-Chip
max bandwidth **: 81.92 Gbps**

output Serializers
max bandwidth **: 81.92Gbps**



- **the bandwidth of the data readout is high up to 163.8 Gbps : 2.56×10^9 packets /sec**
  : 89×10^3 frames / sec
- **the bandwidth the data transport components match to each other**
- **multi-level FIFO architecture with the push-back overflow control**

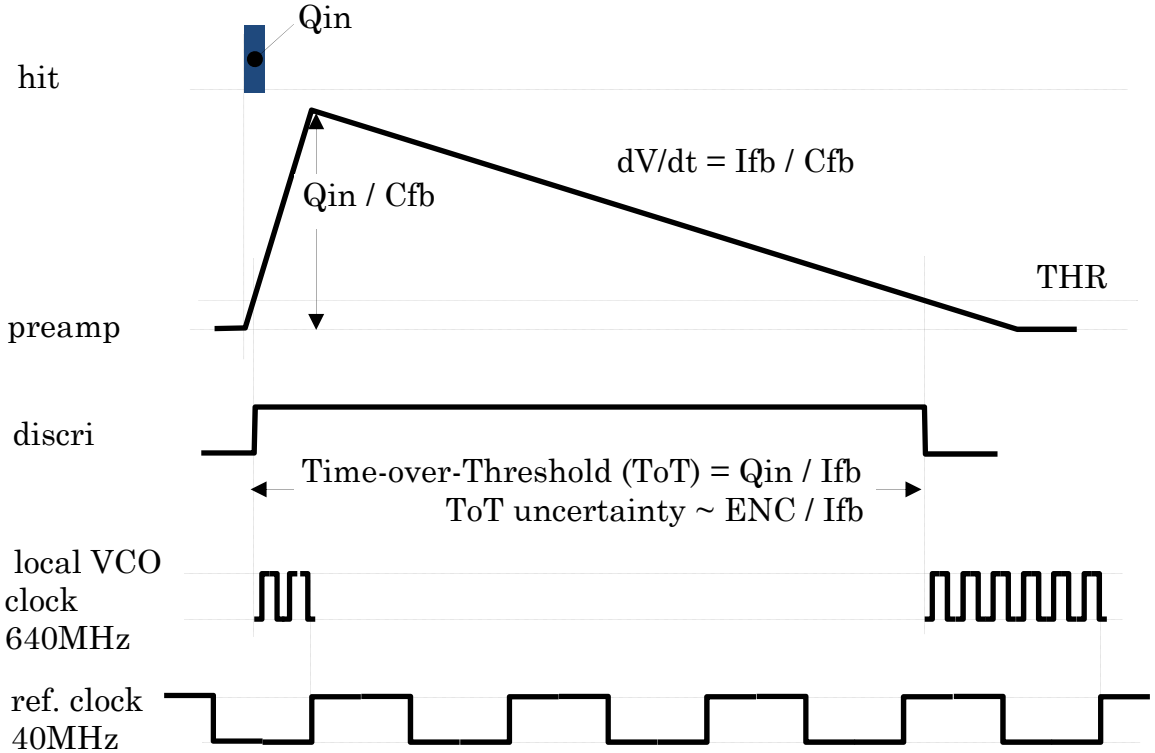
In-pixel signal processing



- **the pixel-level circuit : - digitizes all the information contained in the hits**
  - adds pixel coordinate information
  - sends the data packet to the periphery of the chip
- **the local oscillator (VCO) starts to generate a 640MHz clock when it is triggered by the hit. The VCO runtime is limited by the period of a 40MHz reference clock to 25ns**

Hit charge quantization : Time-over-Threshold method (ToT)

Charge sensitive amplifier (CSA) with a Krummenacher feedback network (I_{fb}= I_{KRUM} = const)



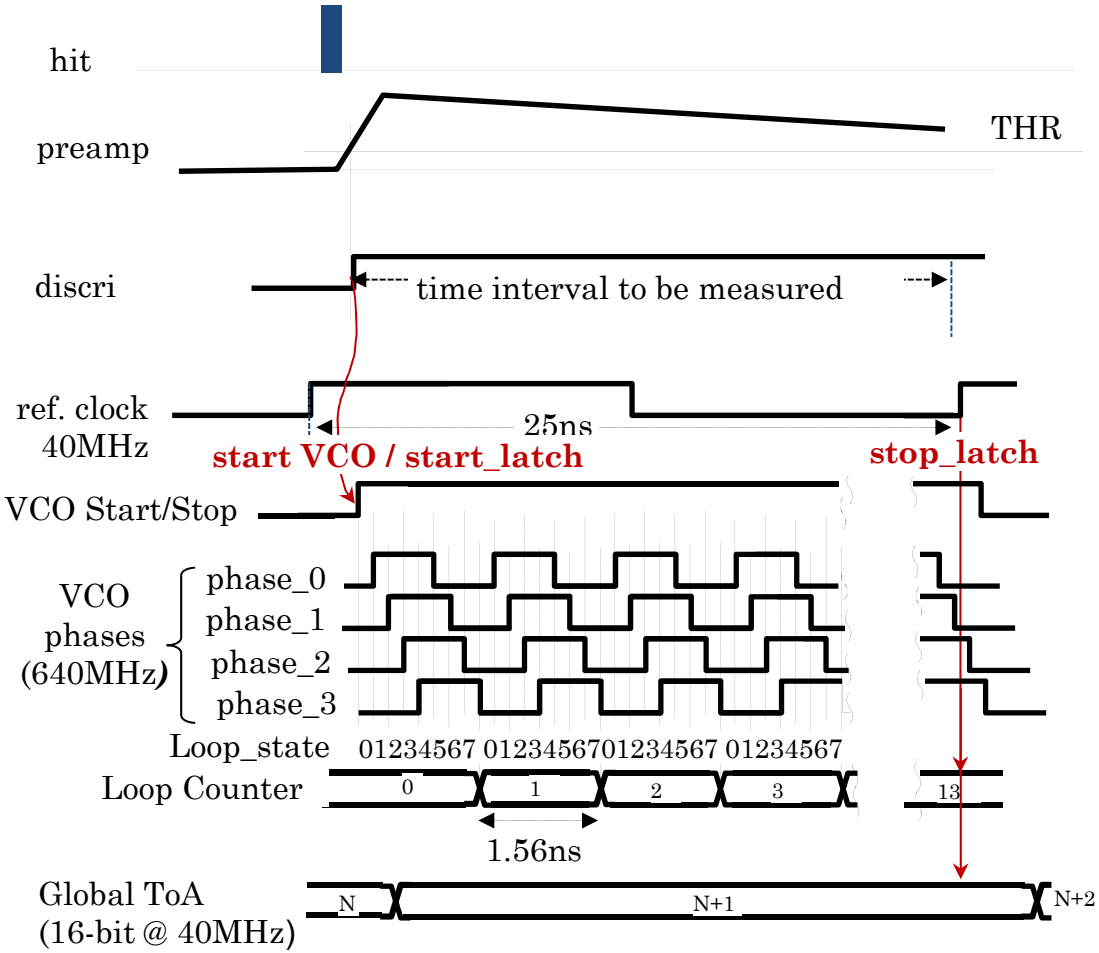
ToT quantization error: T^{640MHz} = 1.6ns /√ 12 = 0.5ns rms
ToT quantization range: 11 bit counter @ 40MHz clock = 51us

		e⁻ collection	h⁺ collection	h⁺ collection (log gain)
Gain=1/Cfb		40mV/ke⁻	40mV/ke⁻	25mV/ke⁻
ENC Cin=75fF		**80e⁻ rms**	**80e⁻ rms**	**90e⁻ rms**
THR (min)		500e⁻	500e⁻	600e⁻
ToT range		250ke⁻	200ke⁻	800ke⁻
I_{KRUM}= 18nA	ToT uncertainty	0.6ns rms ….. 0.7ns rms		
	ToT quantization error	0.5ns rms **~63e⁻ rms**		
I_{KRUM}= 1nA	ToT uncertainty	13ns rms	13ns rms	15ns rms
	ToT quantization error	0.5ns rms **~ 3e⁻ rms**		

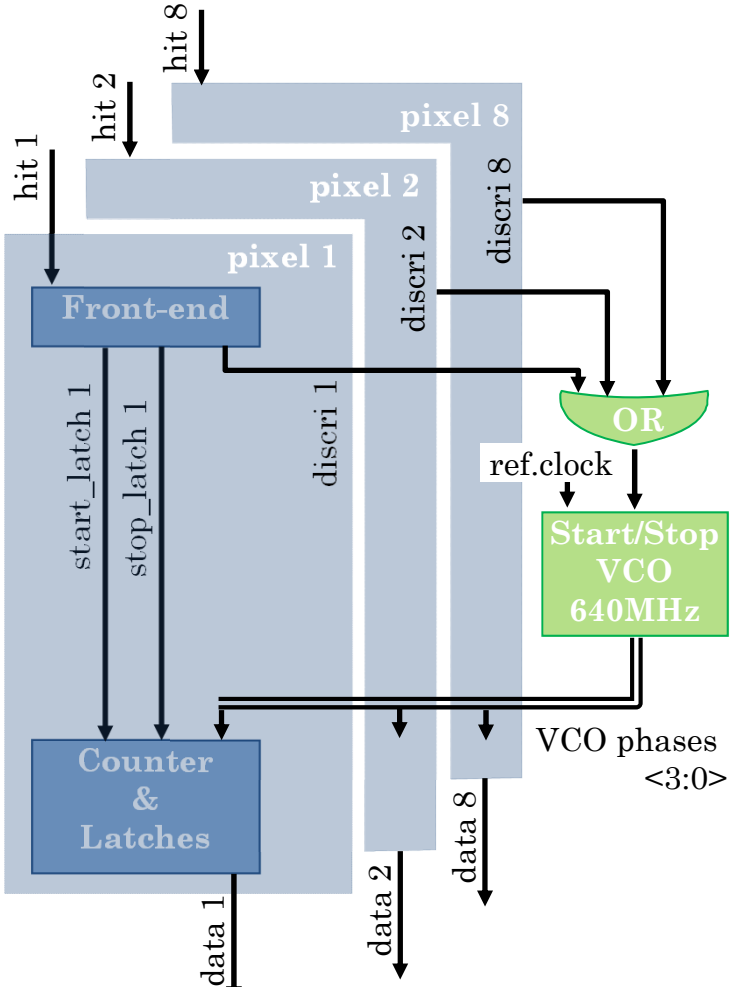
- **a 640MHz local VCO clock pulses and a 40MHz reference clock pulses pass through the clock gating block and are counted giving the digital representation of the measured charge Qin**
- **the range of the ToT method is limited by the value of the charge-storing capacitance Cin+Cfb**
- **the precision of the ToT method is limited by the noise (ENC = 80e⁻ rms)**
- **this corresponds to a 288eV rms energy resolution in silicon sensors (3.67eV/e⁻)**

Hit arrival time (ToA) quantization : a 195ps TDC per pixel

Time-to-digital conversion : the signals



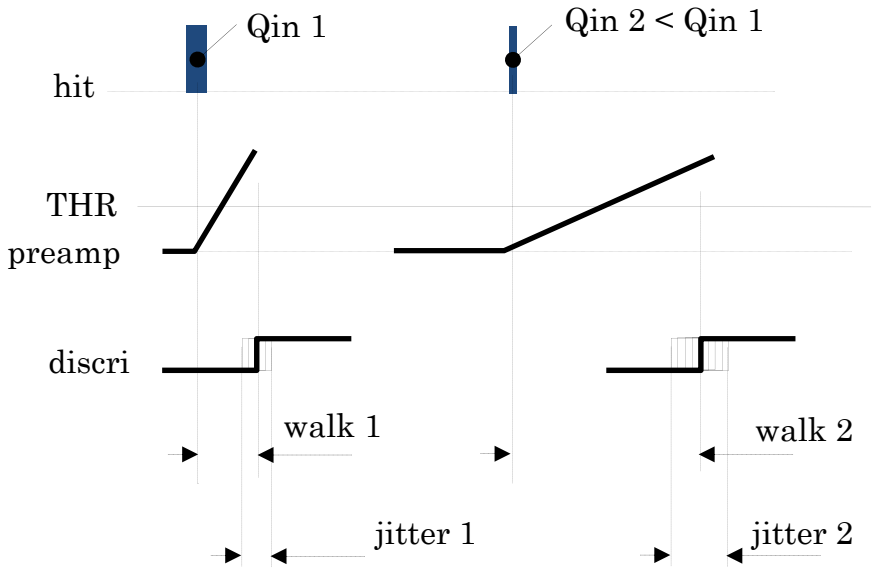
TDC block diagram



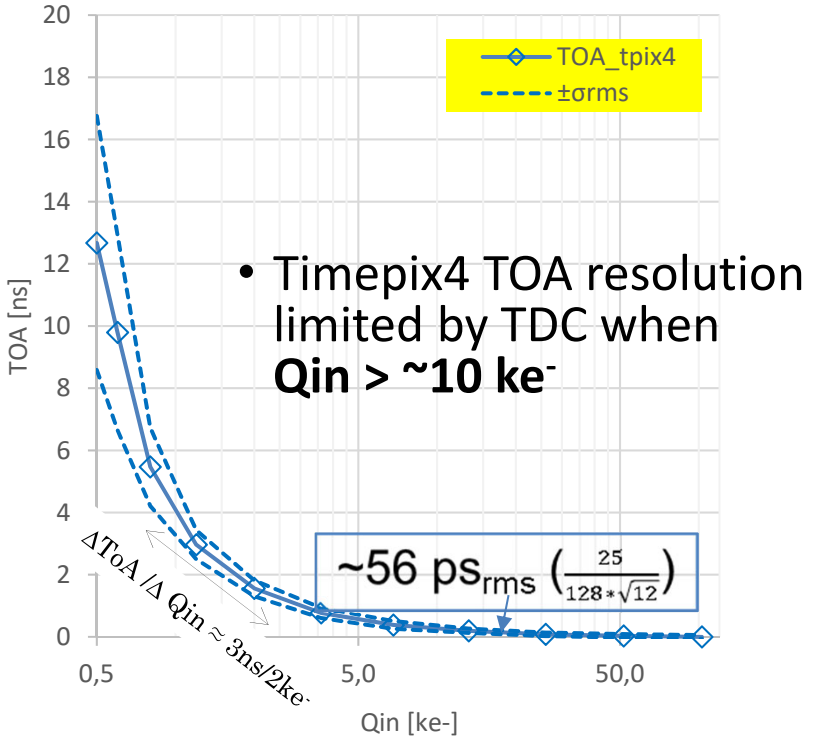
- the resolution of the TDC is limited by the size of the VCO loop state (195ps = 1/640MHz / 8)
- the dynamic range of the TDC is set by duration of the global timing orbit (1.638ms= 16bit@40MHz)
- the VCO consumes significant current (~500uA) when it is running
- the VCO power consumption is negligible due to a low running duty cycle (~10^{-3})

Hit arrival time (ToA) : accuracy limiting effects

Time-walk & noise time-jitter



ToA (Qin) @ THR=500e⁻, ENC=60e⁻rms
(simulated by R. Ballabriga)

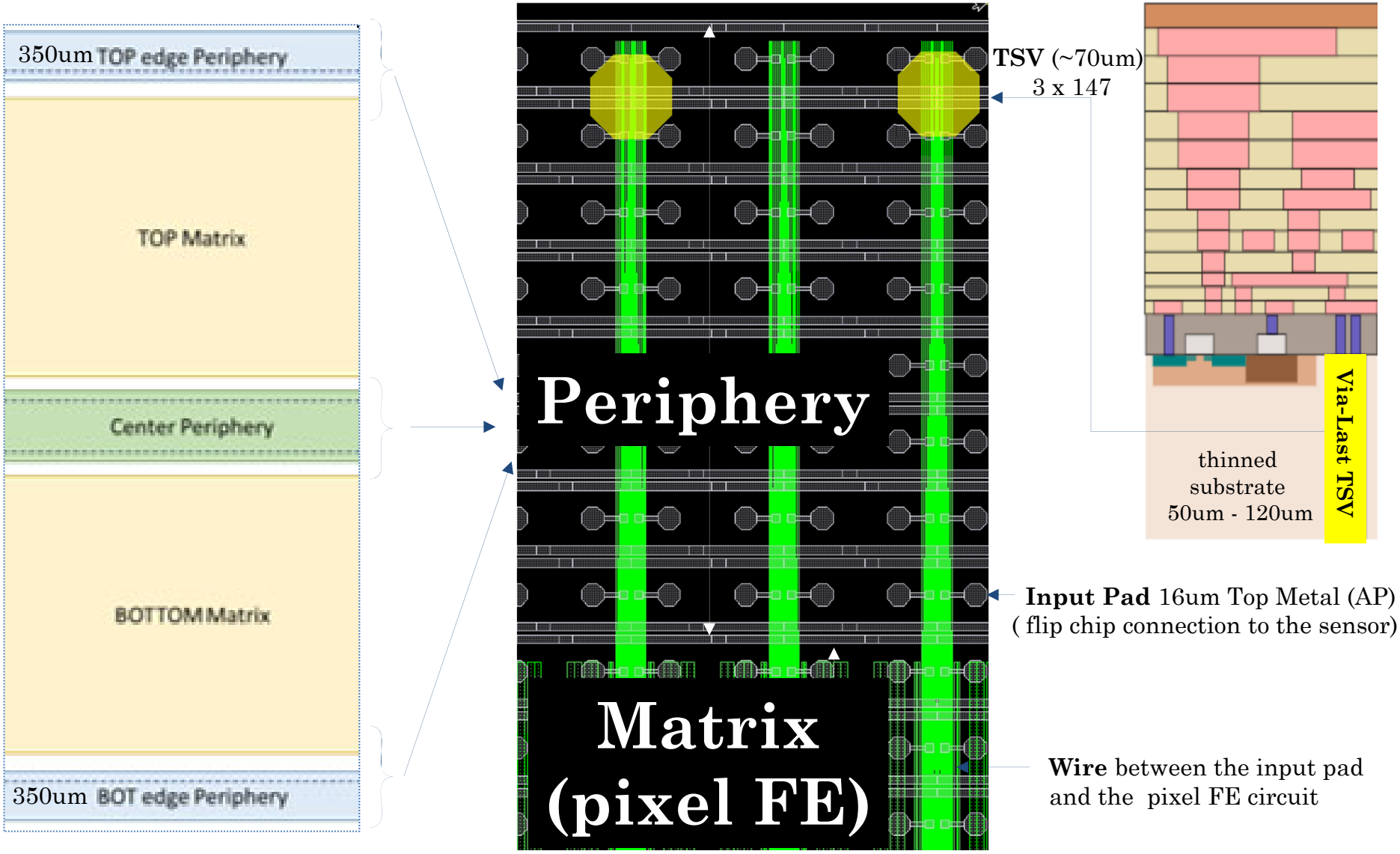


- **the performance of the Front-end circuit (preamplifier, discriminator) limits the accuracy of the timing measurements (time-walk, noise time-jitter)**
- **a 195ps ToA accuracy can be achieved only for the large-size hits with Qin > 10 ke⁻**
- **the ToT charge information will be used to identify the large-size hits**
- **for small-size hits (< 10ke⁻) : - the ToA @ ToT time-walk correction is feasible**

ToA rms = ToT rms • ΔToA/ΔQin = 80e⁻ rms • 3000ps/2000e⁻ = 120ps rms

- however the ToA noise jitter is still very high >> LSB (195ps)

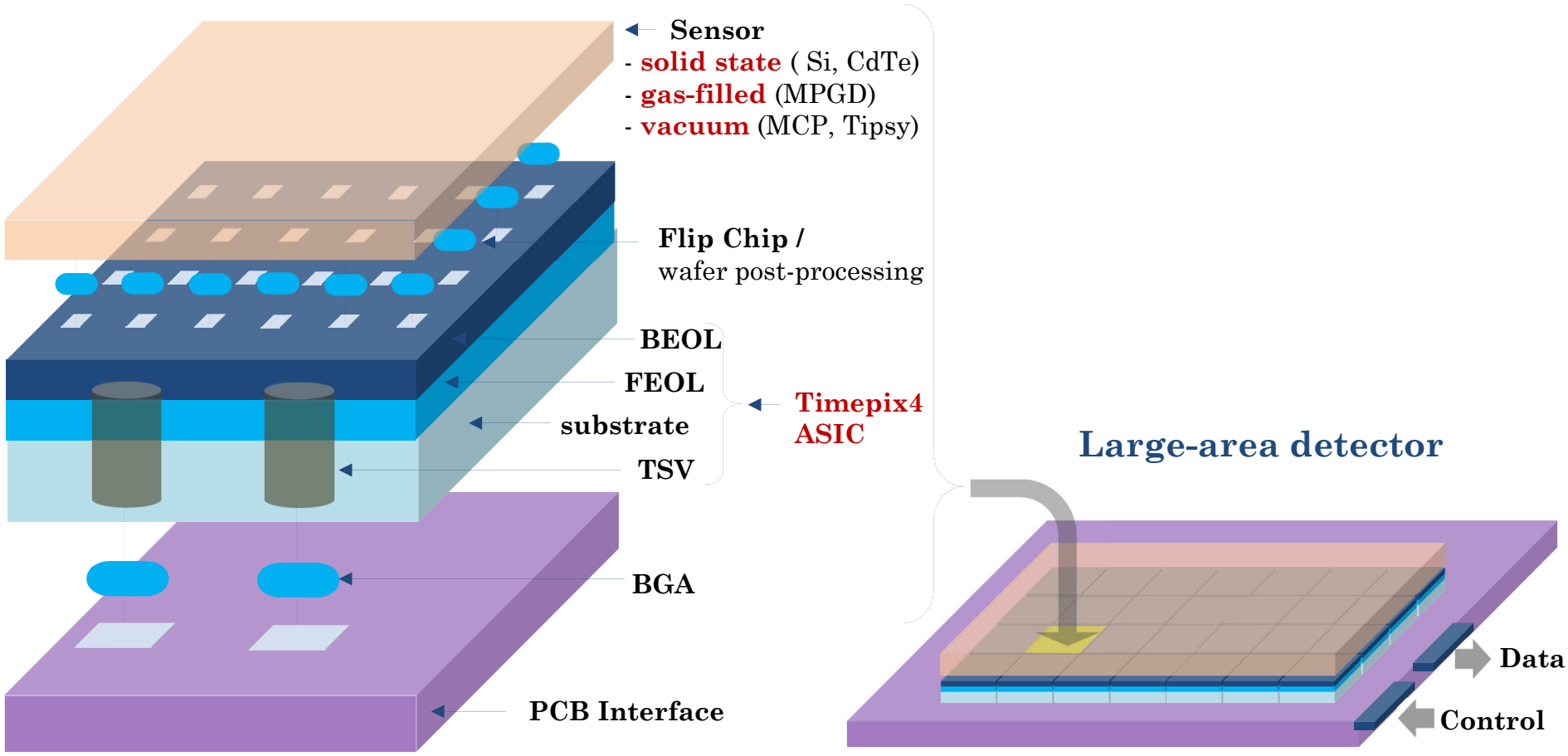
“Hidden” peripheries with TSV (Through-Silicon-Vias)



➢ **chip surface utilization is high > 99.5% active area**

4-sides stitching of the Timepix4 ASIC-level modules

Timepix4 ASIC-level Hybrid detector module



- the TSV technology allows for a 4-sides stitching of the ASIC-level modules to construct large-area detectors
- the large-area detector is almost-dead-area-free : > 99.5% active area

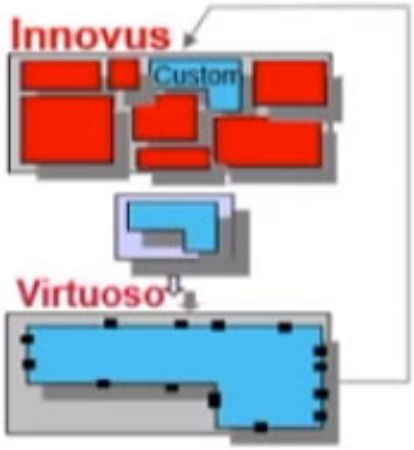
the circuit design aspects

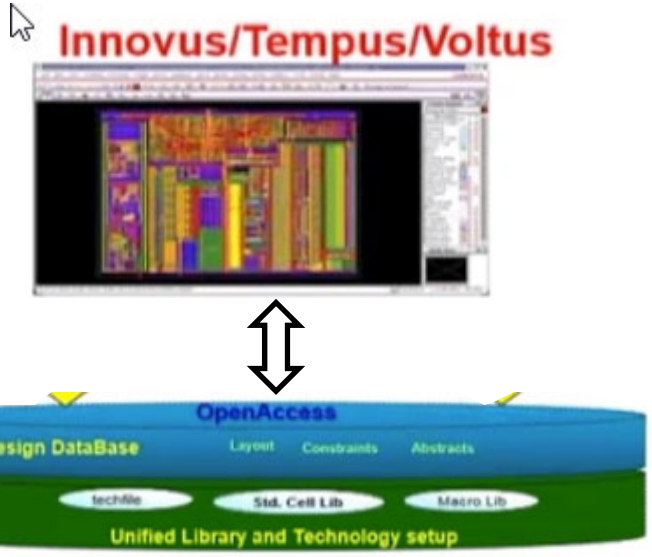
Timepix4: Digital-on-Top (DoT) design methodology

Design Strategy & Top Level Integration (X. Llopart)

- Design specifications closed 2 years ago
- Top level chip floorplan realized at a very early stage
- Use the digital on top flow
  - All analog blocks designed as “islands” inside digital flow
    - Required careful physical and functional characterization before integration
  - Digital logic is used as “glue” between analog blocks
- Use of UVM as system level functional verification
  - Allows full chip top level simulations → Impossible using analog simulators
- Extensive use of repositories (GitLab, ClioSoft) allowed versioning and save file sharing between the design team
- Total design time of ~3 years with 9 engineers → ~12.5 FTE
- ASIC designers:

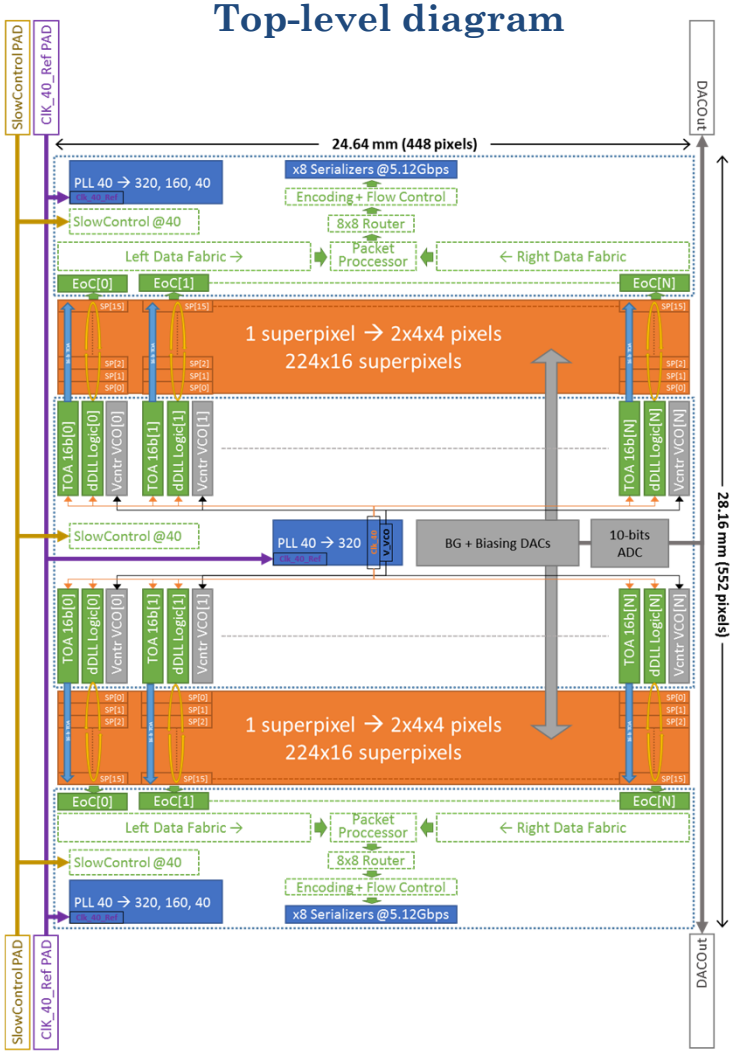
CERN (Gevene): R. Ballabriga, T. Poikela,
E. Santin, V. Sriskaran, N. Egidos, X. Llopart
Nikhef (Amsterdam): V. Gromov , A. Vitkovskiy
IFAE (Barcelona): R. Casanova





Timepix4: Floorplan and Interface

Top-level diagram



High-Speed data Readout :

- 16 x 5.12 Gbps /10.24 Gbps Serial links (±0.6V @ Rterm=100 Ω)

Custom Slow Control protocol:

- write / read configuration registers

pixel matrix configuration > 2 Mb (8-bit/pixel + 24-bit/SPGroup)
peripheral registers (DAC settings, operation modes, e-fuses, ….)

- readout pixel matrix in the test mode @ 40MHz
- point-to-point connection between the chip and the readout system

I2C control protocol:

- on-chip adapter from I2C slave to the Slow Control

Global control signals:

Data Acquisition time window (SHUTTER)
Synchronization of Global Time Stamp counter (TO_SYN)
External reset (RESET)

Resets procedure:

- periphery logic reset : concurrent
- pixel matrix reset : sequential

External clocks:

- Slow control clock (< 40MHz) (SC_CLOCK_IN)
- PLL Clock reference (40MHz / 320MHz) (CLK_REF_PLL)
- I2C Clock (SCL_I2C)

Internal clock generation:

- configurable PLL circuits (320MHz / 640MHz outputs)

Monitoring / debugging :

- internal-generated analog signals via an on-chip ADC (DAC_OUT)
- internal digital signals (TEST_OUT)

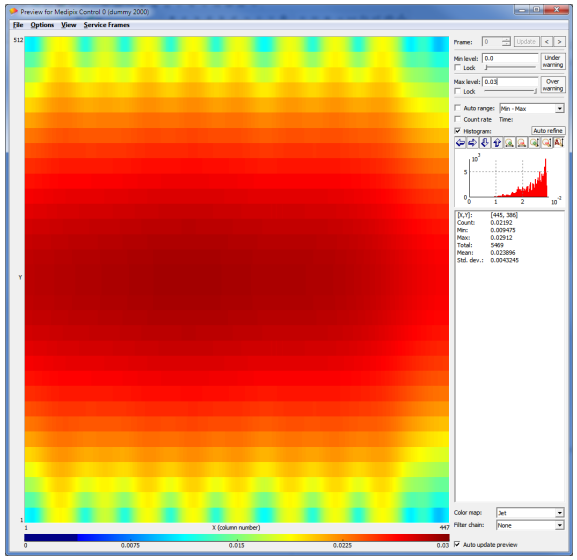
➢ **the chip can be controlled/readout in either single-periphery or multi-periphery configuration**

Uniformity of the power supply voltage across the chip

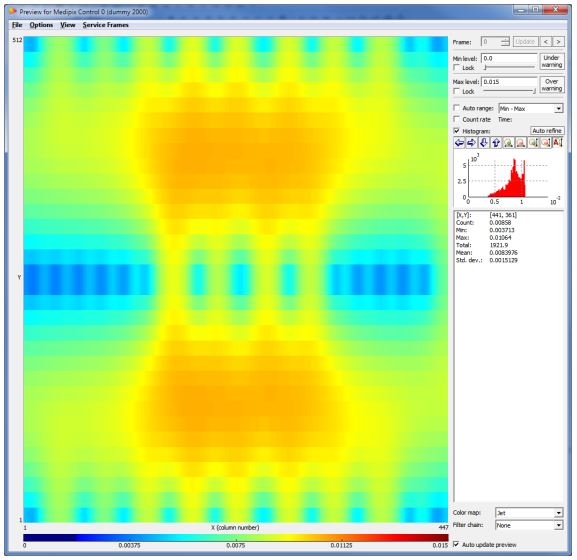
Analog (static) power supply distribution (simulated by X. Llopart)

		2WB	3TSV
Nominal Analog Power [10 µA/pixel]	V_{drop} [max-min]	19.6 mV	6.9 mV
	Imax pad	60 mA	57 mA
Low Analog Power [1 µA/pixel]	V_{drop} [max-min]	1.96mV	0.69mV
	Imax pad	6 mA	5.7 mA

double-side
Wire-Bond (WB) I/O pads



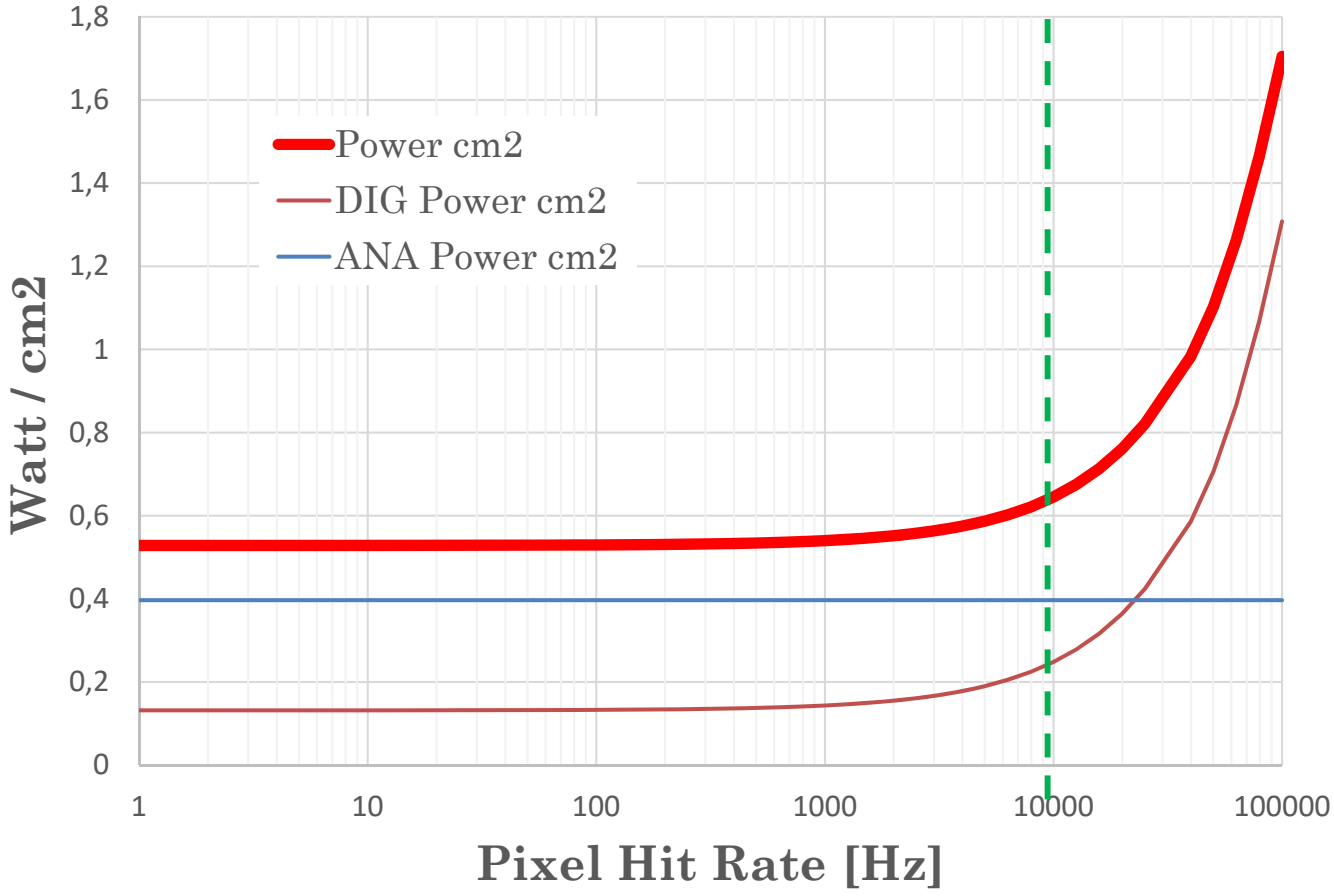
triple-side
Through-Silicon-Via (TSV) I/O pads



➢ **the power supply voltage IR drop across the pixel matrix is very low (6.9mV) when a 3-side bonding scheme is used**

Timepix4: Dynamic and Static Power Consumption

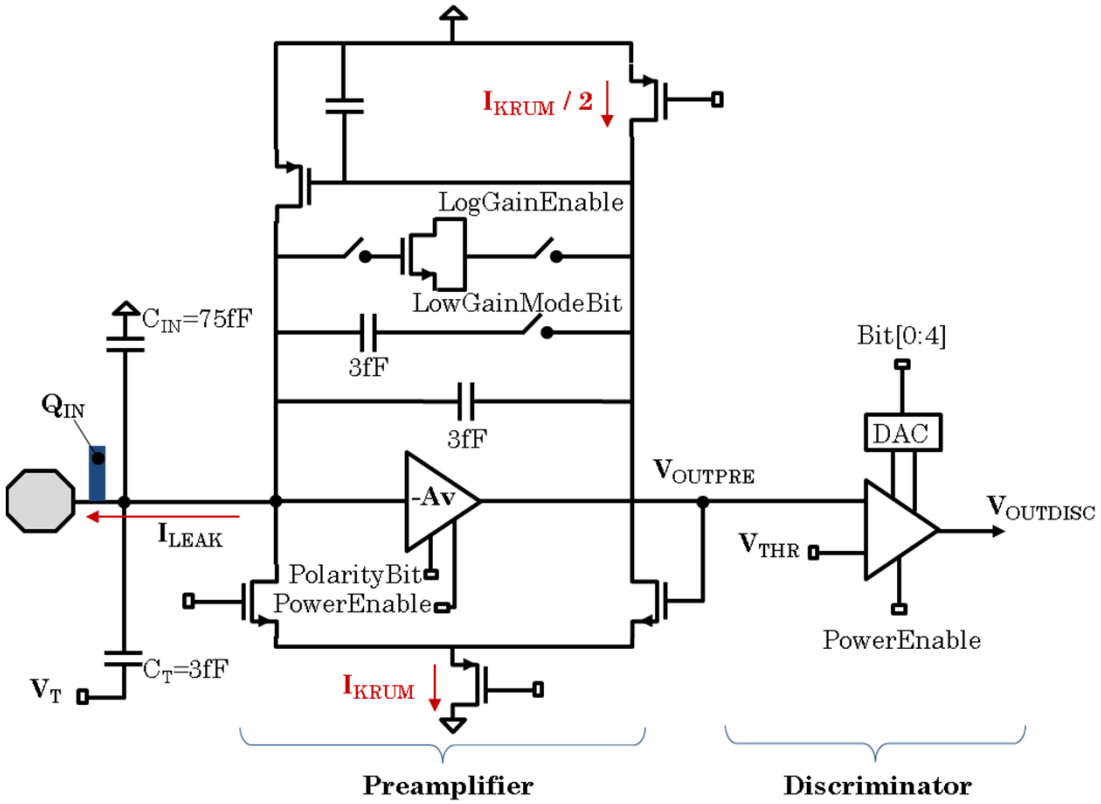
Dynamic and Static Power as a function of hit rate in the Tracking (data driven) readout mode (simulated by X. Llopart)



➢ **the on-pixel analog front-end circuit is the largest contributor to the power budget (9uA/pixel @ 1.2V = 10.8uW/pixel)**

Timepix4: Krummenacher Charge-sensitive Front-end circuit

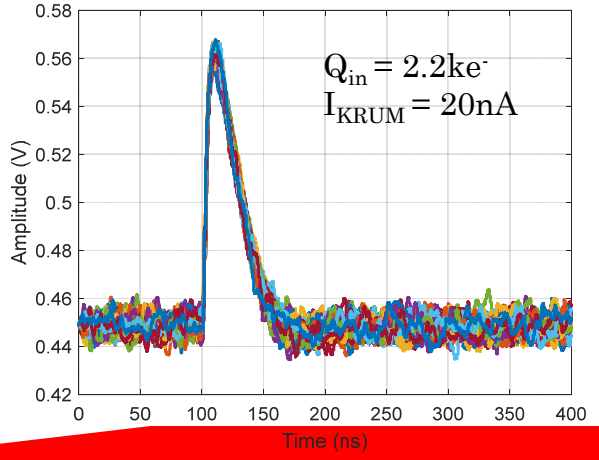
Simplified schematic (designer R. Ballabriga)



Some specifications

Q_{IN} polarity	bipolar
Sensor leakage current compensation	< 10nA
Feedback current (Ikrum)	1nA - 20nA
Hit processing time	~ Q_{IN} / Ikrum
Gain=1/ Cfb	adjustable
Input capacitance (C_{IN})	20fF: input pad 45fF: pixel-pad routing (RDL)
ENC @ Cin=75fF	**80e⁻ rms**
ΔENC / ΔI_{LEAK}	4e⁻ / nA
Hit arrival time uncertainty	<60ps rms @ Q_{IN}> 10 ke⁻
Power consumption	preamp: 4uA @1.2V discri: 5uA @1.2V

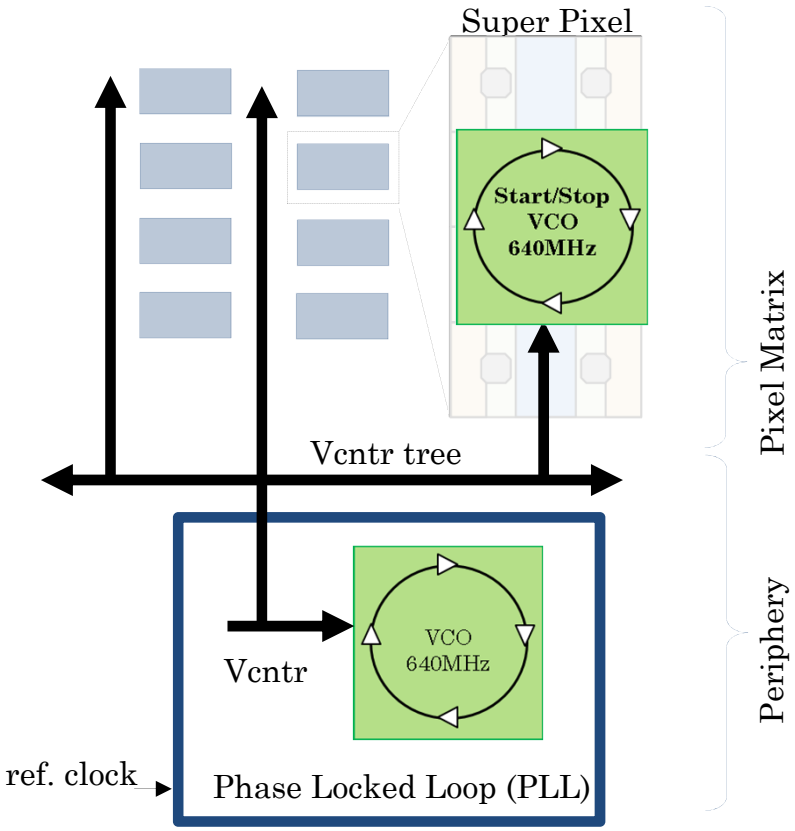
Preamplifier output



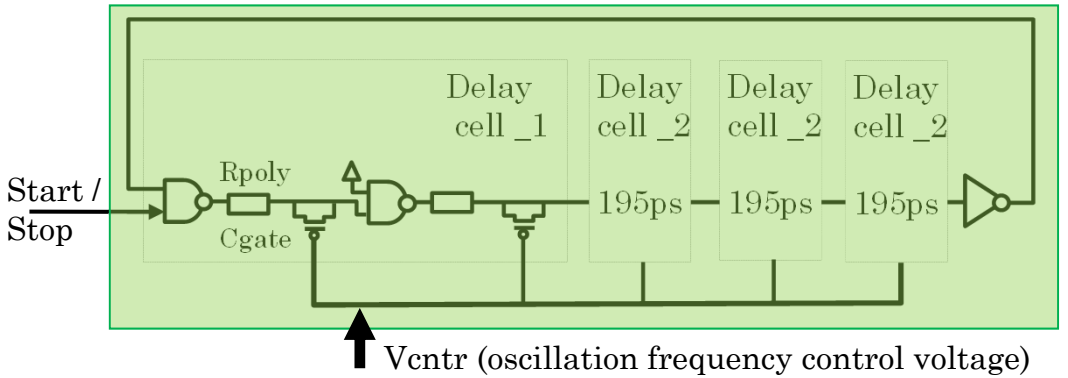
- **the versatile front-end :**
  - **is compatible with various sensors (solid-state, gas-filled …)**
  - **optimized for high hit rate operation (dead time < 200ns)**
  - **optimized a 195ps hit arrival time accuracy**

Voltage-Controlled Oscillator (VCO)

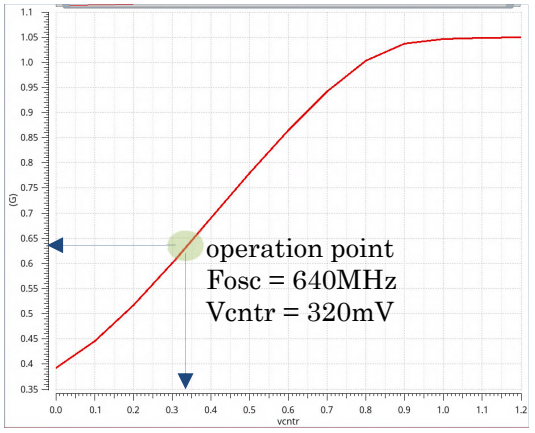
VCO control schema



VCO schematic



VCO control characteristic: Fosc (Vcntr)

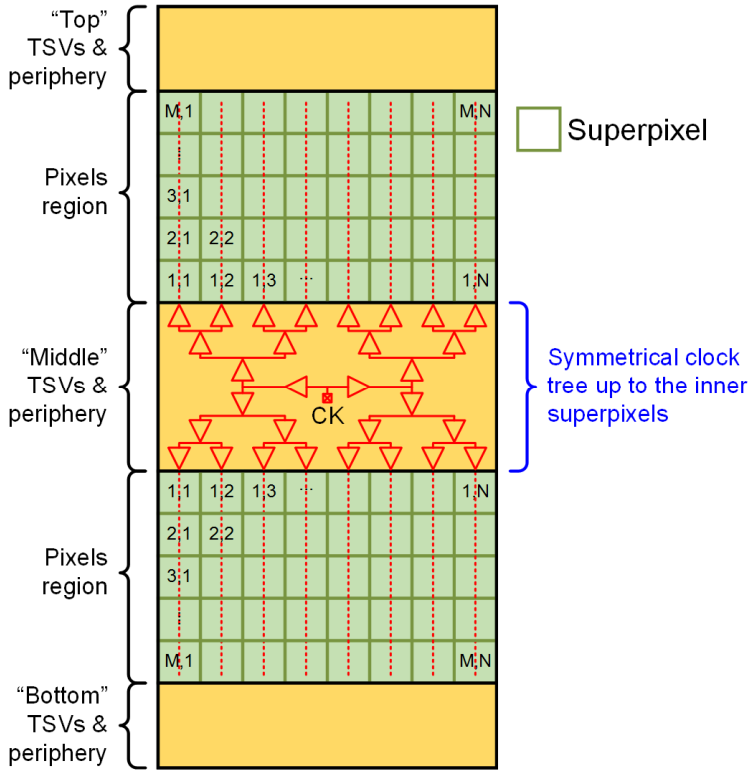


- the VCO consists of 4 RC-delay cells taking only 1% area in the layout of the pixel matrix
- the VCO control voltage is generated in the common PLL, locked to the target oscillation frequency (640MHz)
- in this schema the VCO oscillation frequency is immune to the process corner and the temperature variation
- the VCO can also be tuned individually to compensate for the fabrication mismatch in the range 2.5%
- a ±1mV dynamic voltage drop on the power supply busses will not causes an error more than 1/2 LSB

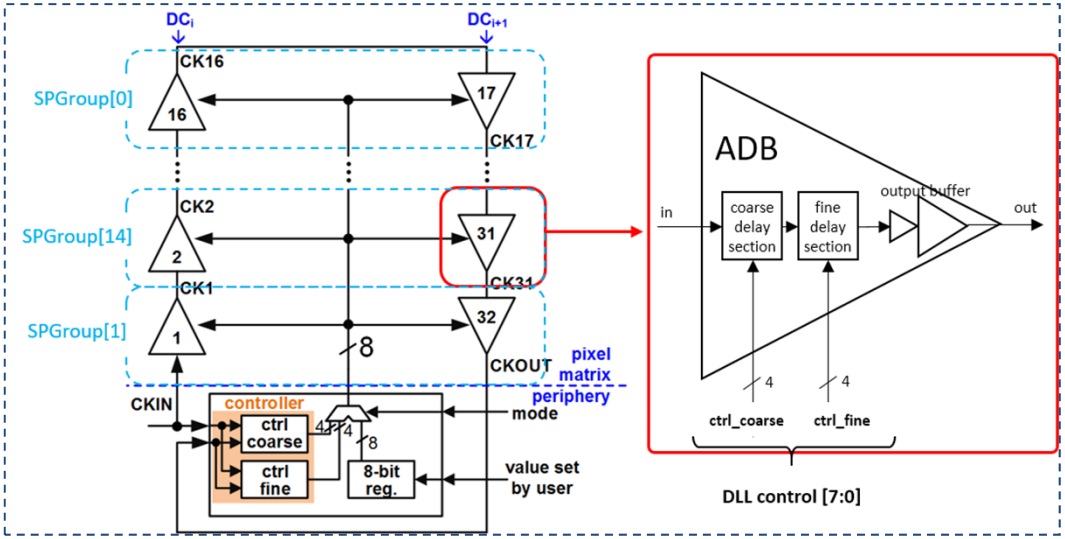
Reference time clock delivery to the on-pixel TDC

https://iopscience.iop.org/article/10.1088/1748-0221/14/01/C01024/pdf

Chip-level ref. clock tree



digital DLL per Double Column (designer E. Santin)

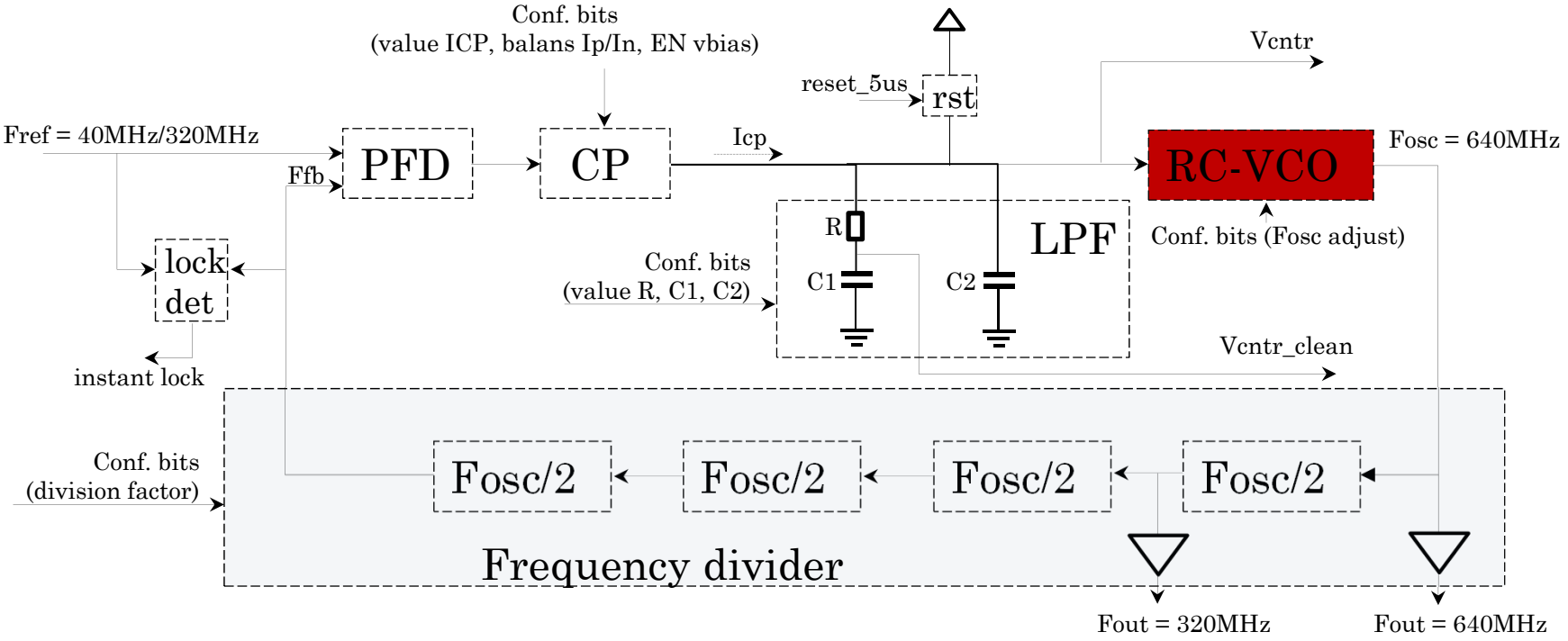


Specifications

reference time clock frequency	40MHz
number of the dDDL blocks per chip	448
SPGroup – to – SPGroup delay	780ps
delay skew uncertainty	< 100ps
total power per chip (dDLL contribution)	157mW

➢ **the reference time clock is delivered to each on-pixel TDC with an uncertainty less than 100ps**

Timepix4: Generic PLL

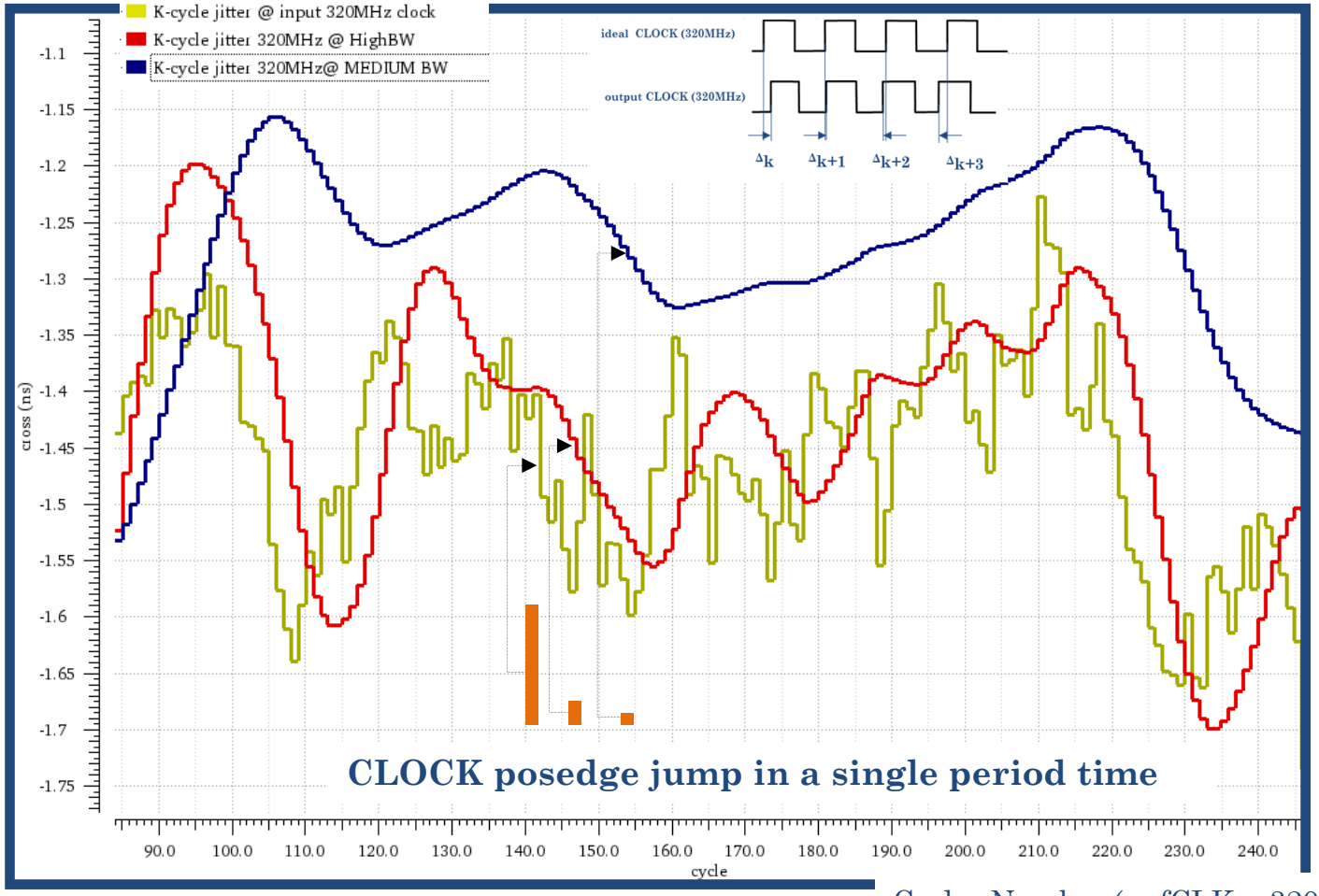


- **used as :**
  - **reference PLL to generate Vcntr for the on-pixel VCOs**
  - **a 320MHz/640MHz clock generator for the periphery logic**
  - **a 320MHz clock-cleaning PLL in the high-speed (5/12/10.24Gbps) data serializer block**

  internal time jitter : < 50ps p-p
- **MOSCAP_rf25 thick gate oxide capacitance (low leakage)**
- **DNW for better substrate isolation**
- **separate power supply voltage domain**

Clock-cleaning PLL configuration

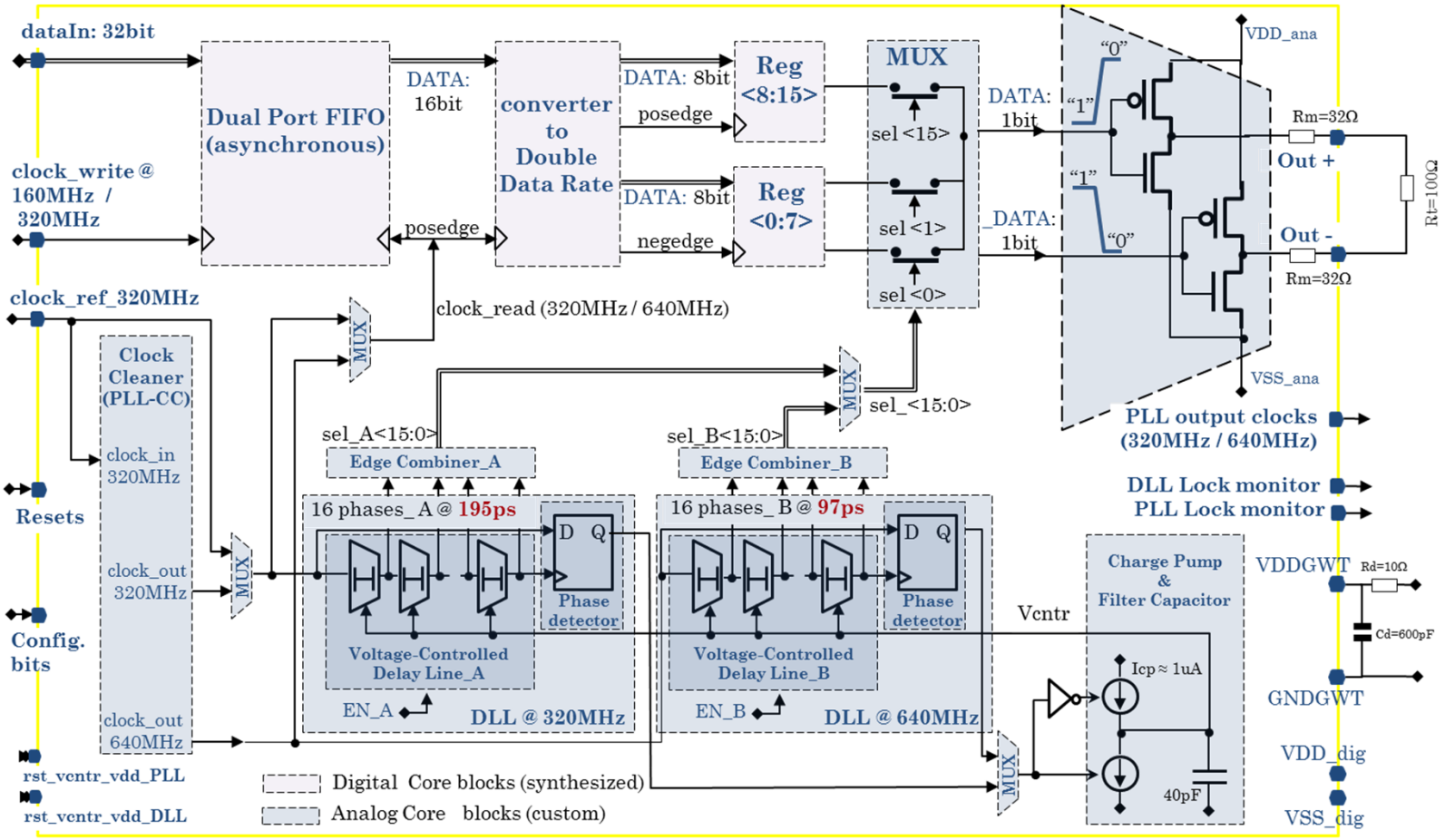
Suppression of the jitter of the reference clock



Cycles Number (refCLK = 320MHz)

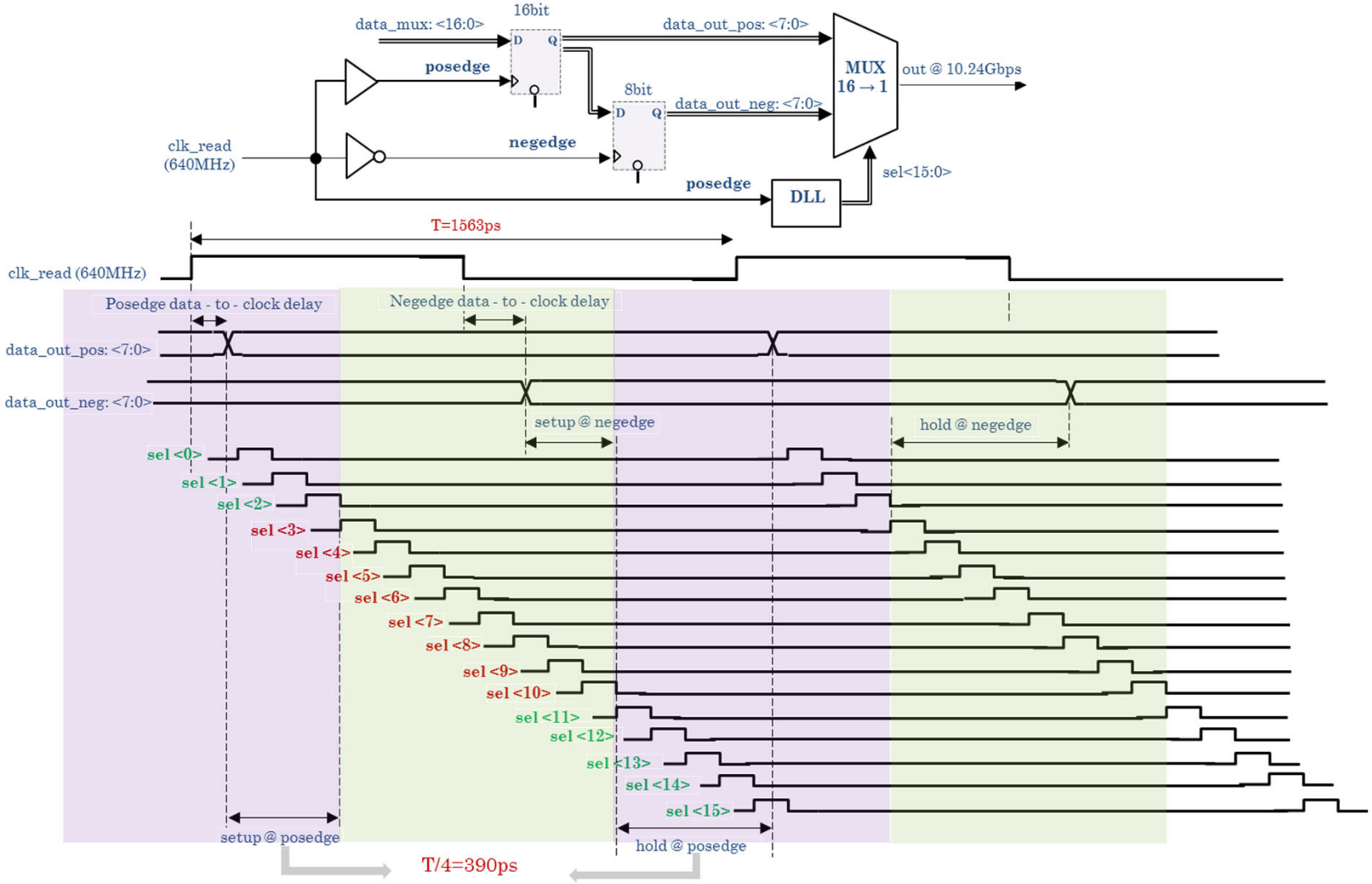
- **high-frequency jitter = sudden jumps of the clock edges will be suppressed by the PLL-CC circuit**
- **low-frequency jitter = long-term (accumulated) shift of the clock edges will be suppressed by the off-chip in the clock-and-data recovery circuit (CDRPLL)**

GWT-CC :5.12/10.24Gbps Data Serializer and Wireline Transmitter



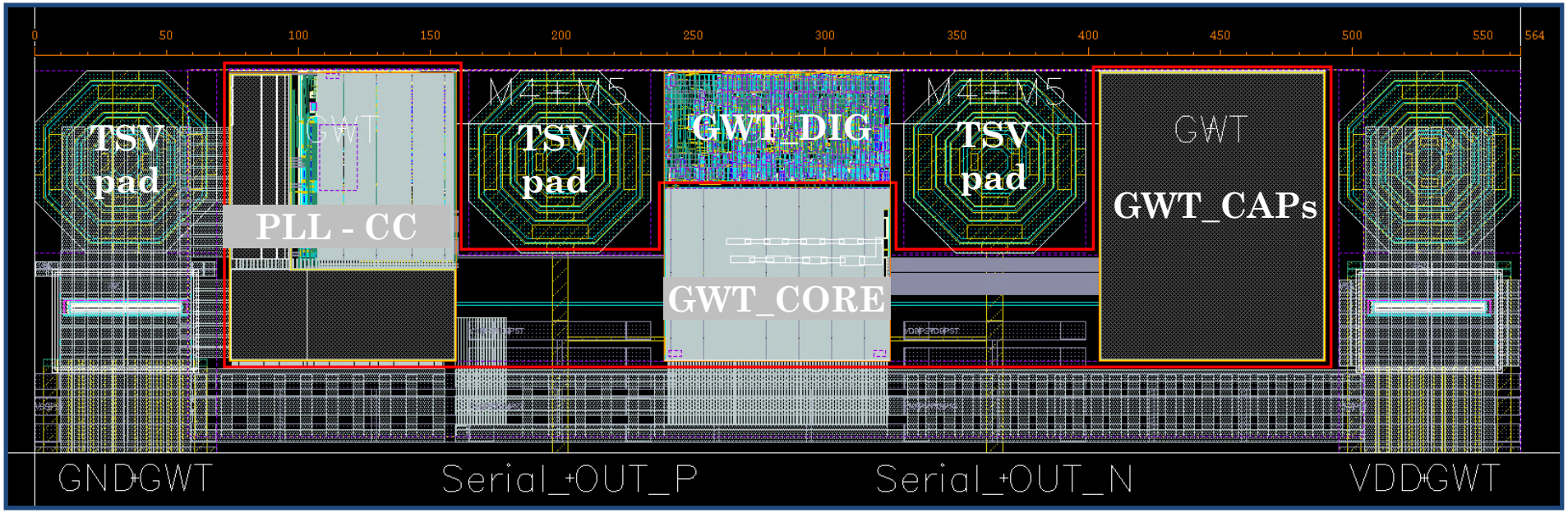
- successor of block used in the VeloPix
- selective data rate: 5.12Gbps/10.24Gbps
- bypassable clock-cleaning PLL (ring-oscillator) : internal jitter < 30ps p-p
- NO high-frequency external clocks: ≤ 320MHz
- voltage-mode transmitter: output swing = ±0.6V @ Rterm=100Ω
- low power : 24mW

GWT-CC: 1/16-Rate Multiplexer-based architecture



- **16-bit input data: byte-interleaved internally (both-edge-clocked)**
- **internal DLL used to generate 16 phases controlling the Multiplexer**

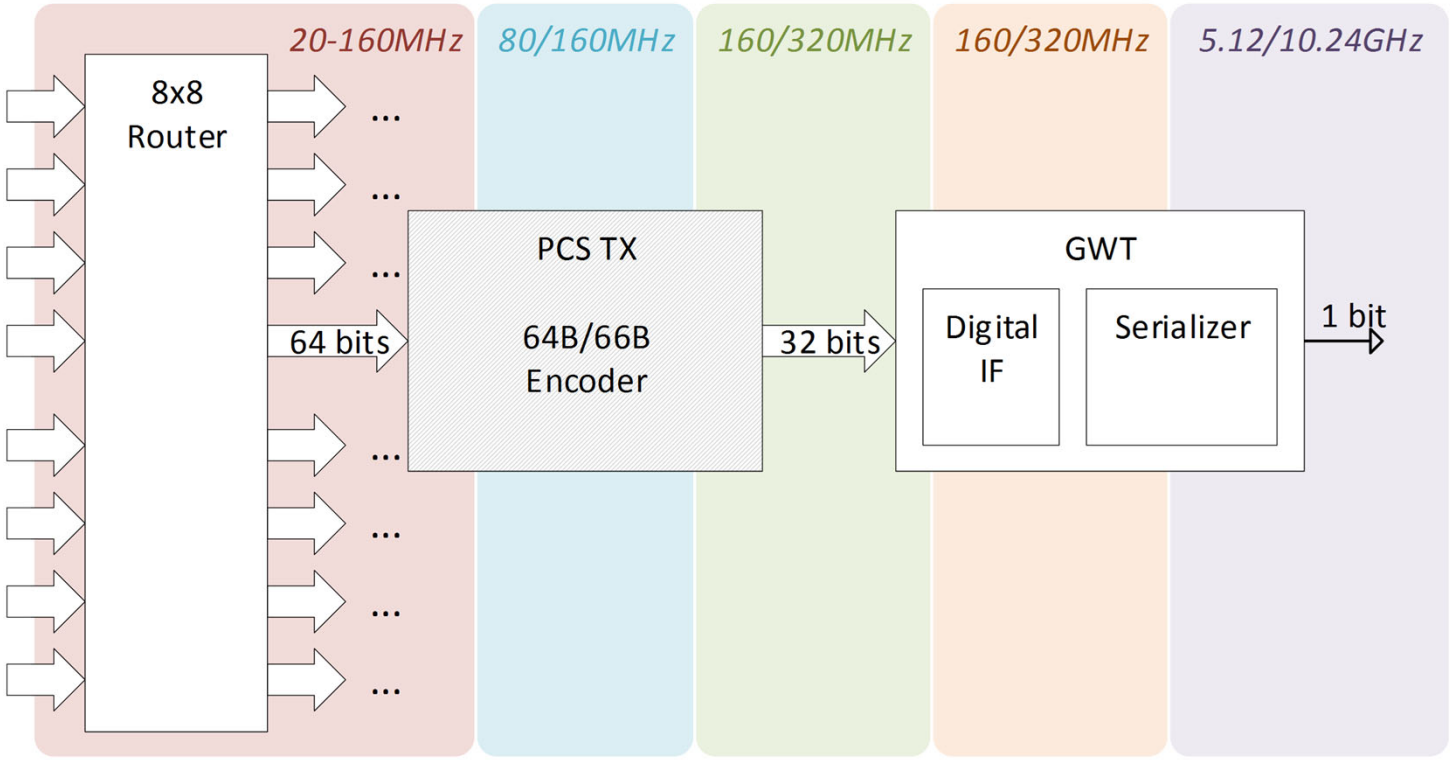
GWT-CC: layout



- **area: 4 x 10^4 µm^2**
- **local (dedicated) power supply connections : TSV / Wirebond pads**
- **deep N-well (DNW) substrate isolation of the analog cores**
- **current-leakage-free large-area capacitances: thick gate-oxide varactor**
- **local power supply grid M4/M5**

Timepix4: Physical Coding Sublayer Transmitter (PCS TX)

Top-level diagram (designer A. Vitkovskiy)



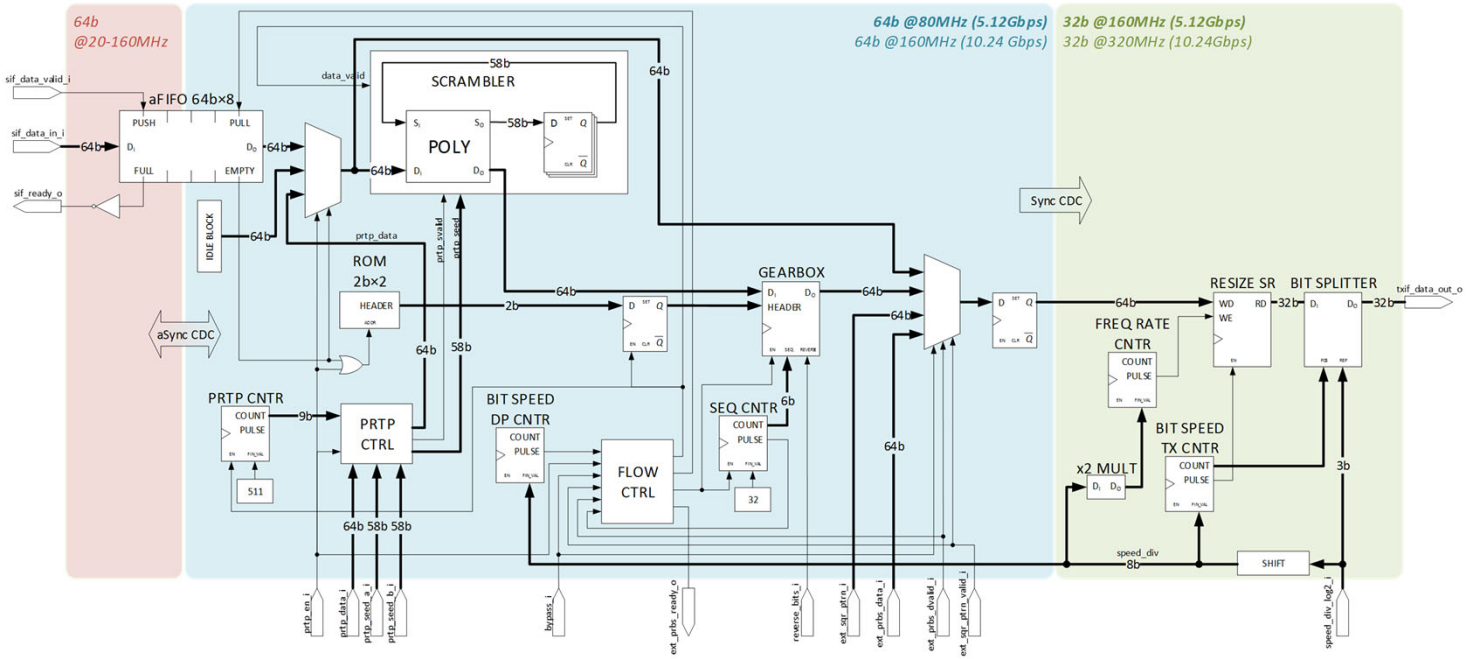
Features

- 64B/66B data Encoder
  - IEEE802.3ae standard
  - packet starts with LSB / MSB
  - 3.125% data overhead
  - data packet alignment
- Encoder bypass mode
- Data scrambling
  - initial value is a zero-vector
- Serial data speed control
  - by multiplying data stream bits
  - 5.12/10.24Gbps → 40/80Mbps
- Test pattern generation
  - square wave
  - pseudo-random
  - PRBS-31, PRBS-23, PRBS-15, PRBS-7

➢ **provides an interface between the Packet Router block and the GWT-CC block**

Timepix4: implementation of the PCS TX block

Block diagram (designer A. Vitkovskiy)



Features

- ❑ Input Asyncronous FIFO :
  - clock-domain-crossing
  - data backpressure compensation
- ❑ Scrambler:
  - randomizes the bit stream for disparity correction between 1's and 0's
- ❑ Pseudo-Random Pattern Controller :
  - enables test mode
- ❑ Gearbox:
  - add 2 bits synch header
  - transmits 32 data blocks in 33 clock cycles to keep a 64b input/output data stream
- ❑ Bit Splitter :
  - serial speed control by repeating of the bits in the data stream

➢ **this highly-configurable and multi-functional topology makes the readout of the chip compatible with various telecommunication standards and computer networking technologies (10 Gigabit Ethernet)**

➢ **the bandwidth of the data transfer is fully digitally-controlled**

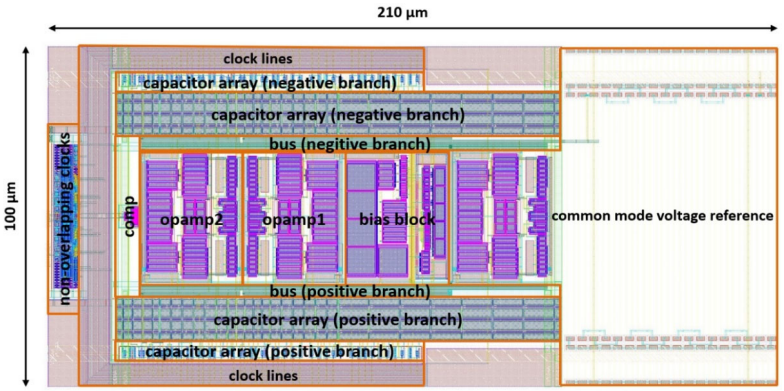
Timepix4: Analog blocks (periphery)

- 12-bit ΣΔ ADC (designer R. Casanova)

Monitoring 12-bits Fully Differential Second Order
Incremental Delta Sigma Converter ADC for Timepix4" – TWEPP 2019
spec: conversion rate up to 1190 samples / sec , power: 8uW

monitors internal signals:

- internal power supply drop (analog and digital core supply)
- BG and temperature monitor
- DAC Biasing voltages



- BandGap reference circuit (designer S. Michelis)

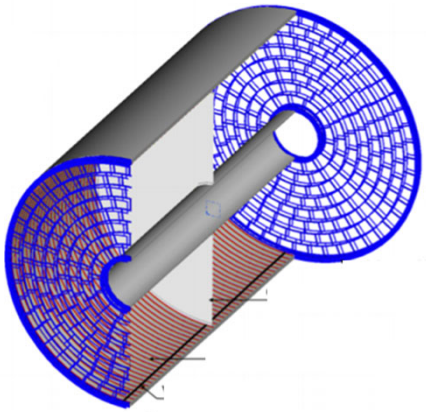
https://ieeexplore.ieee.org/abstract/document/6872688
spec: Vout = 330mV,
maximum output deviation in absolute value: ±1.1% (process) & ±1.6% (mismatch)
gradient=6.2uV / °C , noise =180uV @ BW=100MHz ,
power =240uW , Enclosed Layout diode

➢ **the Timepix4 chip in fully digitally controlled and monitored (NO analog input/output signals)**

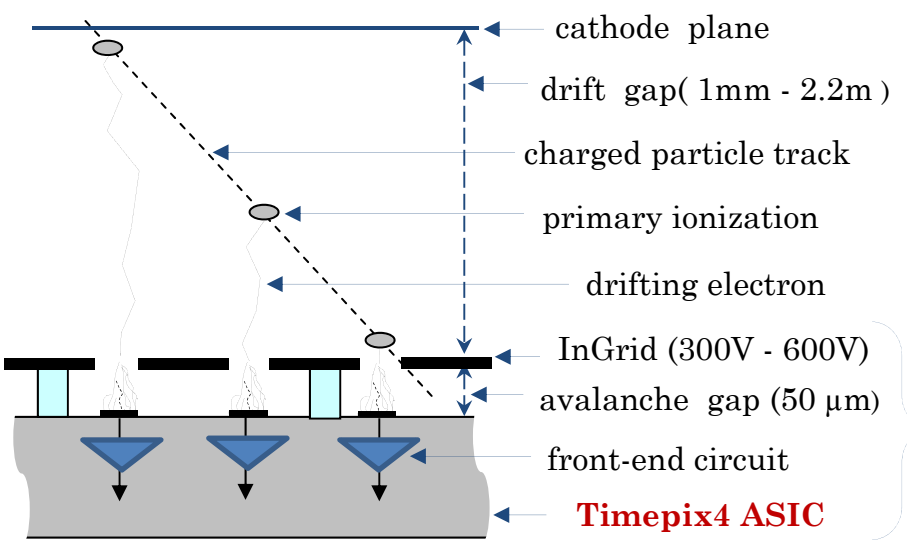
application opportunities

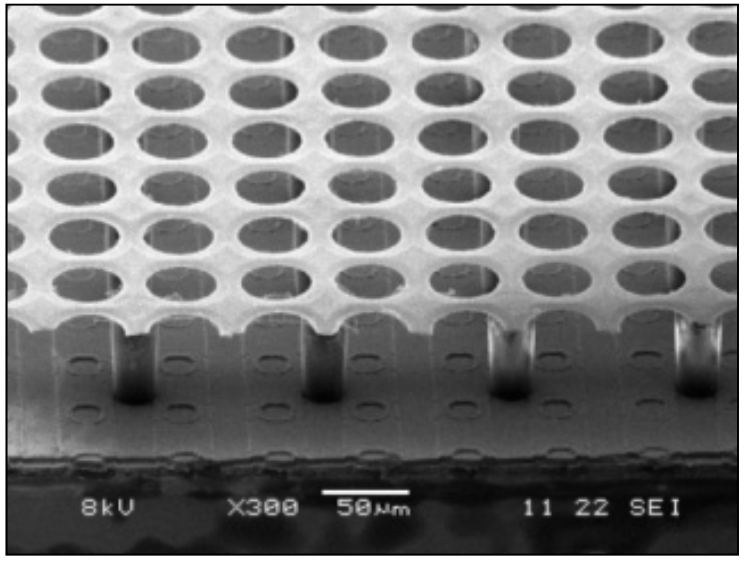
Large-area Time Projection Chamber (TPC) detector for ILC

2 x 8.7 m² TPC : International Large Detector (ILD)



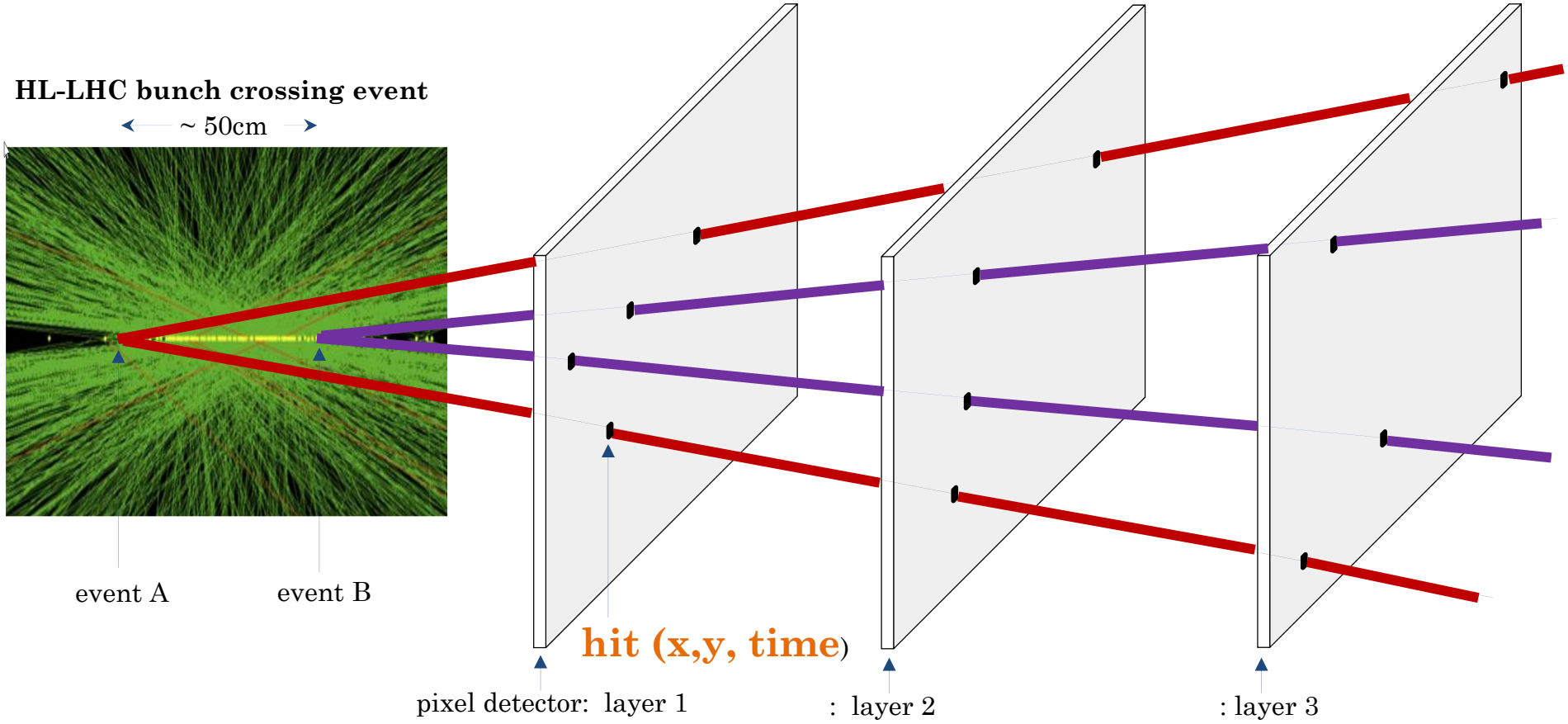
GridPix gas-filled detector : high-resolution 3D track reconstruction





- the Timepix4 ASIC can be used to build large-area TPC detectors
- its small pixel size (55µm) & high time resolution (195ps) are useful for 3D tracking

Tracks reconstruction in High-Luminosity environment

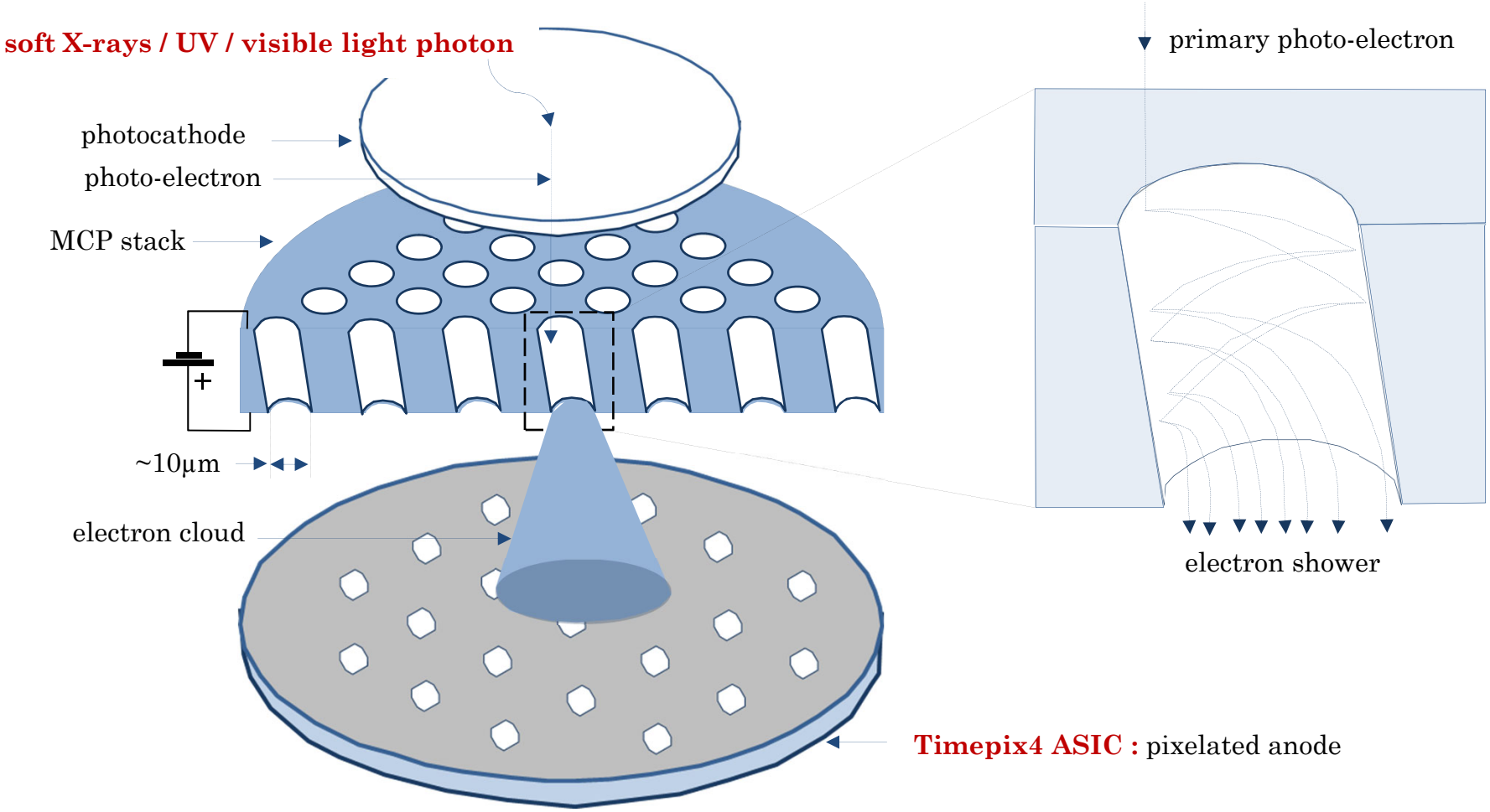


- **hit time stamp gives an extra dimension in the track reconstraction**
- **a < 50ps time resolution is required for efficient 4D tracking in the HL-LHC environment**
- **the Timepix4 ASIC (195ps time of arrival bin size) will be used as a test vehicle**

Microchannel Plate (MCP) vacuum detectors with the Timepix4 readout

Single-photon imaging detector with sub-100 ps and < 10µm resolutions

https://doi.org/10.1016/j.radmeas.2019.106228

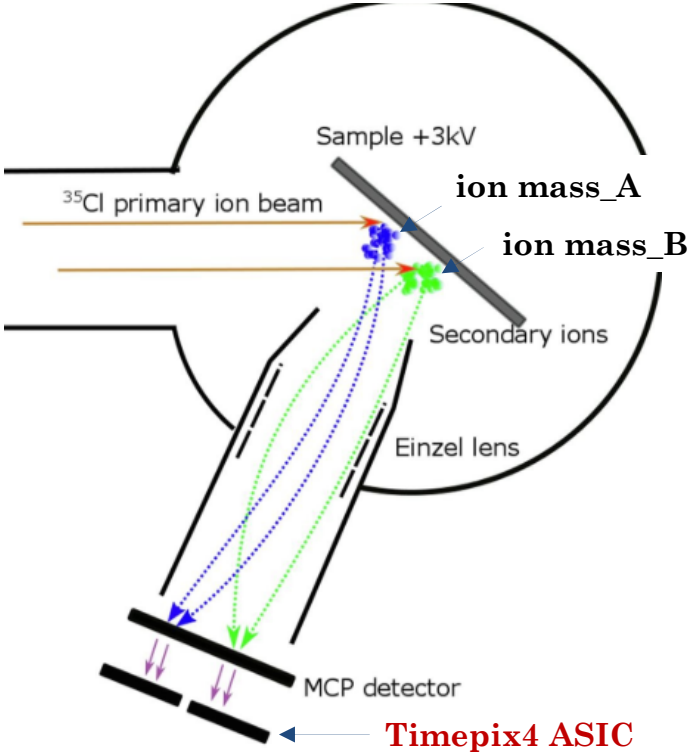


- the MCP detector internally has high spatial (<20um) and temporal (<100ps) resolutions
- it can fully exploit high position (55um) and time resolution (195ps) of the Timepix4 chip

Molecular imaging with the Timepix4 readout

https://www.sciencedirect.com/science/article/pii/S0168583X19303611?via%3Dihub

Time-of-Flight (ToF) mass spectrometer



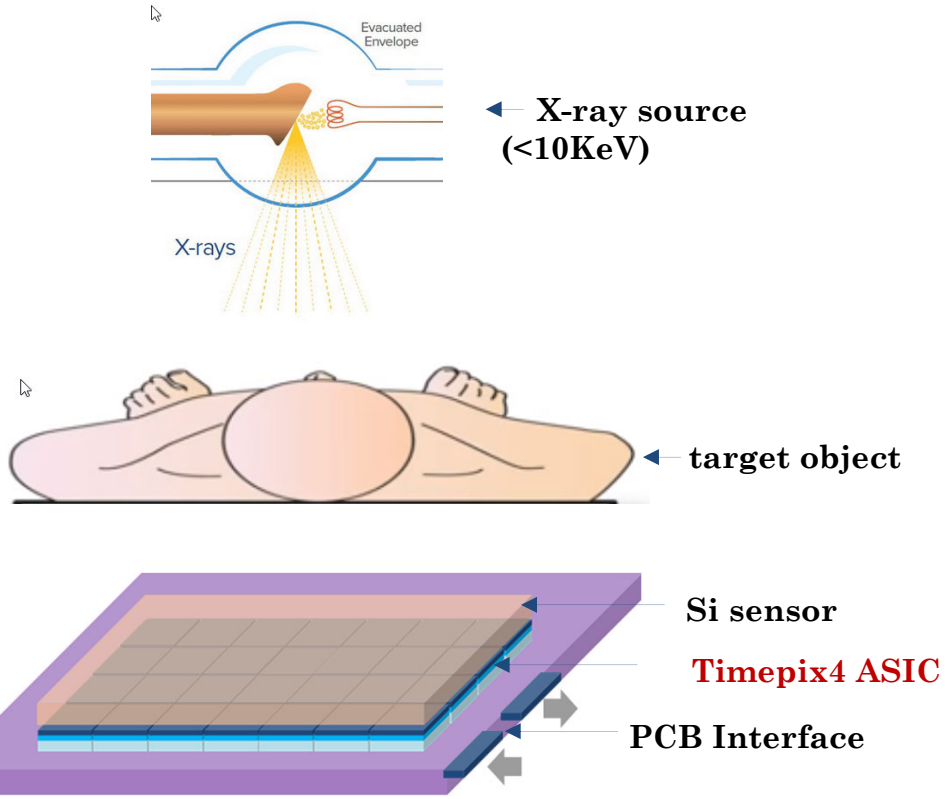
Timepix4 : Tracking (event-based) readout mode

Dead-time free operation	Continuous Data driven readout
Time-of-arrival (ToA) accuracy	**195ps**
Mass resolution (feasible)	**m/dm → 30000**
Max Hit rate	3.58 x 10^6 hits/mm^2/s
Spatial resolution (pixel size)	55µm x 55µm

- **the time-of-flight (ToF) is used to calculate mass-to-charge value of the secondary ions**
- **with a 195ps event time-tag in the Timepix4 chip very high mass resolution is feasible**

X-ray imaging with the Timepix4 readout

Medical imaging systems



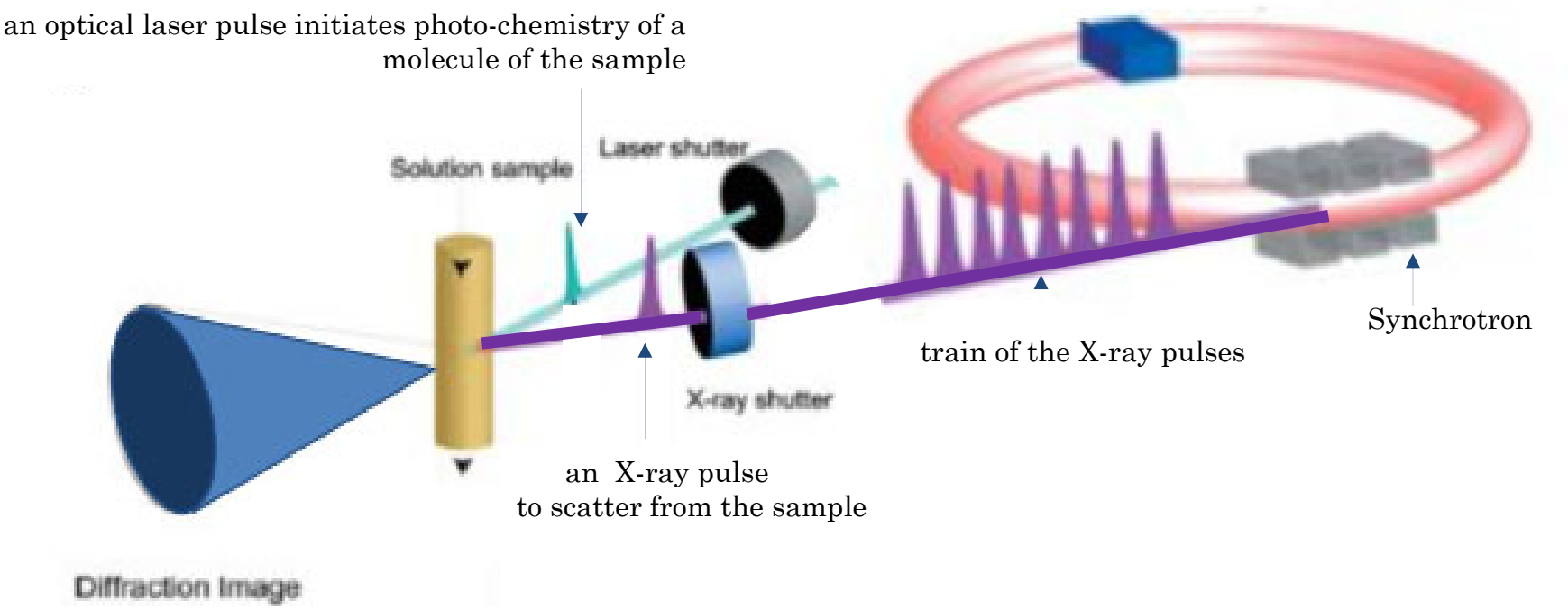
Timepix4 : frame-based readout mode

Dead-time free operation	Continuous Read/Write (CRW)	
On-pixel counter	8 bit	16bit
Max Frame rate	89kFPS	44kFPS
Max Hit rate	~ 5 x 10^9 hits/mm^2/s	
Spatial resolution (pixel size)	55µm x 55µm	

➢ the maximum hit rate is limited by the pulse shaping time in the analog front-end (~200ns) and not by the bandwidth of the readout system

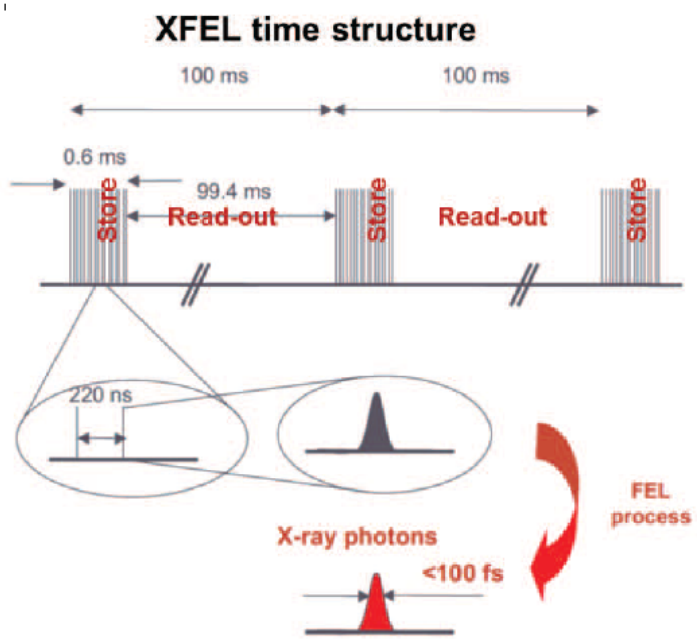
https://www.researchgate.net/publication/320651688_Timepix3_readout_system_for_time_resolved_experiments_at_synchrotron_radiation_facilities
https://www.intechopen.com/books/advances-in-lasers-and-electro-optics/synchrotron-based-time-resolved-x-ray-solution-scattering-liquidography-

X-ray liquidography:
the time evolution of the induced structural changes in molecules



- **the Timepix4 ASIC is very much suitable for a time-resolved diffraction image readout system**
- **in Tracking readout mode there will be good time resolution between the diffraction images for each X-ray pulse in the train**

Timepix4 and the European XFEL facilities



https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7581819&tag=1

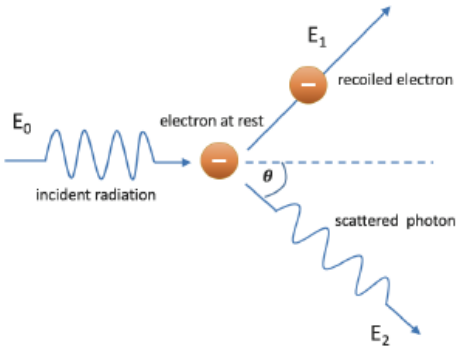
	XFEL	Timepix4
Single pulse size / Dynamic range	**1 – 1000 photons** (12.4keV) per pixel (55um x 55um) **3ke$^-$ … 3000ke$^-$**	**500e$^-$ … 800ke$^-$** (@ log gain mode)
Single pulse processing time	**< 200ns**	**< 200ns** (@ Ikrum>10nA)
On-pixel memory depth	**2700** X-ray pulses every 200ns in a 600usec train	1-2

- **the European XFEL has an extremely irregular time structure of the X-ray flux**
- **the Timepix4 ASIC is NOT optimized for such operation conditions**

Timepix4 : Compton imaging camera

Compton scattering effect

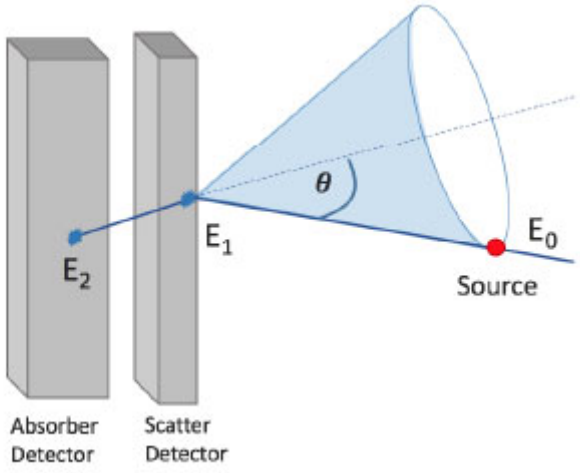
https://iopscience.iop.org/article/10.1088/1748-0221/13/11/C11022/pdf



$$\cos\theta = 1 - m_e c^2 \frac{E_1}{E_0 (E_0 - E_1)}$$

$$E_0 = E_1 + E_2$$

Schema of the Compton camera

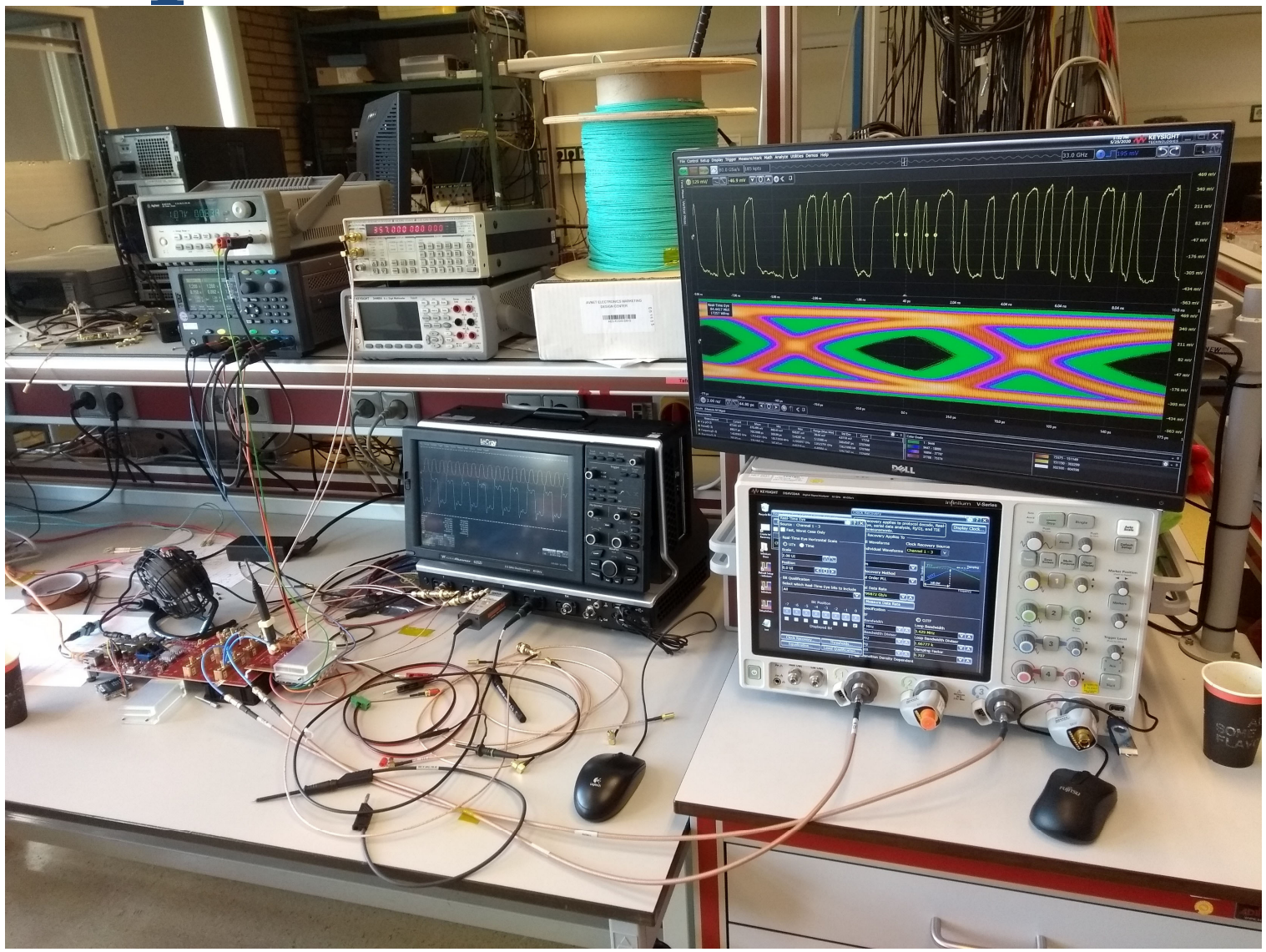


Timepix4: 2D coordinate, energy and time for each single hit

Dead-time free operation	Continuous Data driven readout
Time-of-arrival (ToA) accuracy	**195ps**
Energy measurement accuracy	**300eV rms**
Spacial resolution (pixel size)	**55µm x 55µm**
Max Hit rate	3.58 x 10^6 hits/mm^2/s

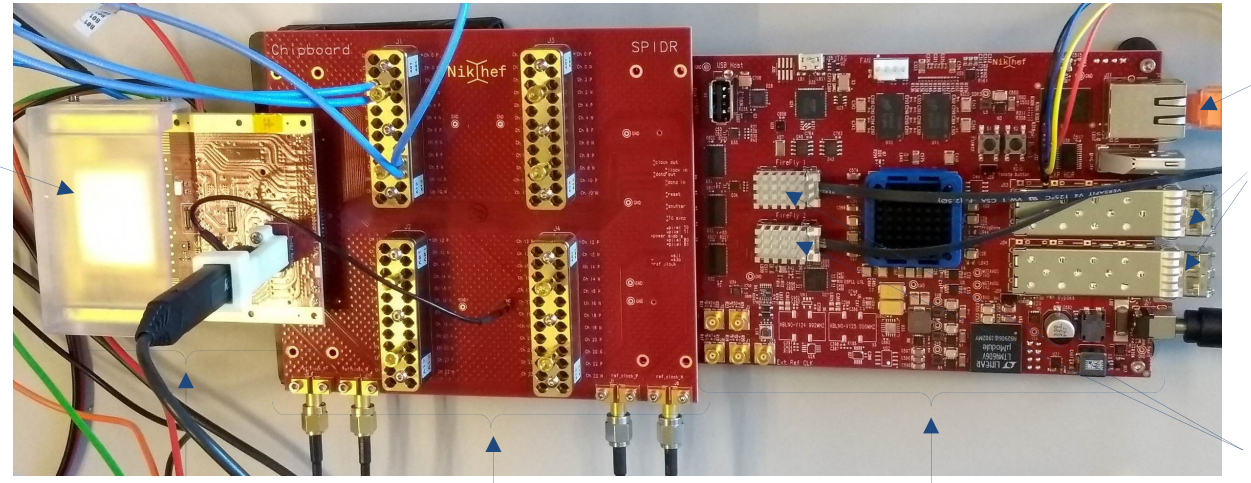
- **the Timepix4 ASIC can be combined with different sensors (1mm Si or 2mm CdTe) to build both the Scatter detector and the Absorber detector**
- **the Timepix4 ASIC delivers a full set of data for each single event needed to estimate the possible direction of the original gamma**

experimental results



Timepix4: test system

SPIDR4 control and readout system (designer Bas van der Heijden, basvdh@nikhef.nl)

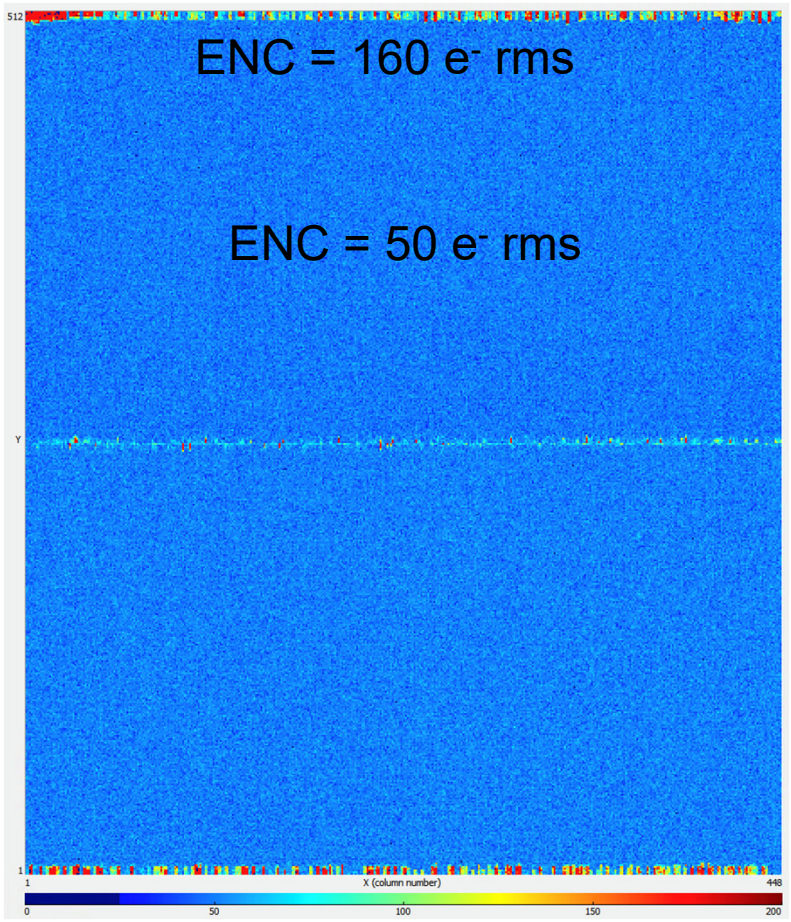


- SPIDR4 readout system from Nikhef
- SPIDR4 Chipboard + Timepix4
- Timepix4 is wirebonded from TOP and BOT periphery WB pads
- Timepix4 accessed (slow control) through TOP periphery
  - Bottom periphery IO is not fully connected due to PCB design error

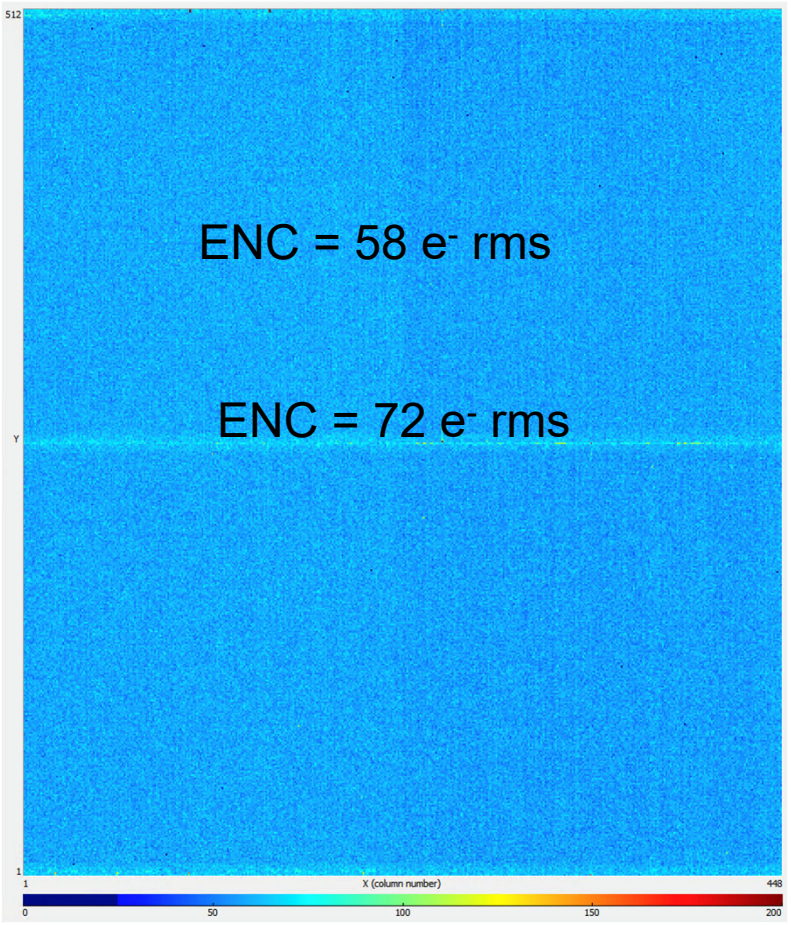
ENC full matrix (X.Llopart)

Timepix4v0

- Excess ENC noise on top of peripheries (x2-4):
  - ~26 rows: [0:7] [250:260] [504:511]

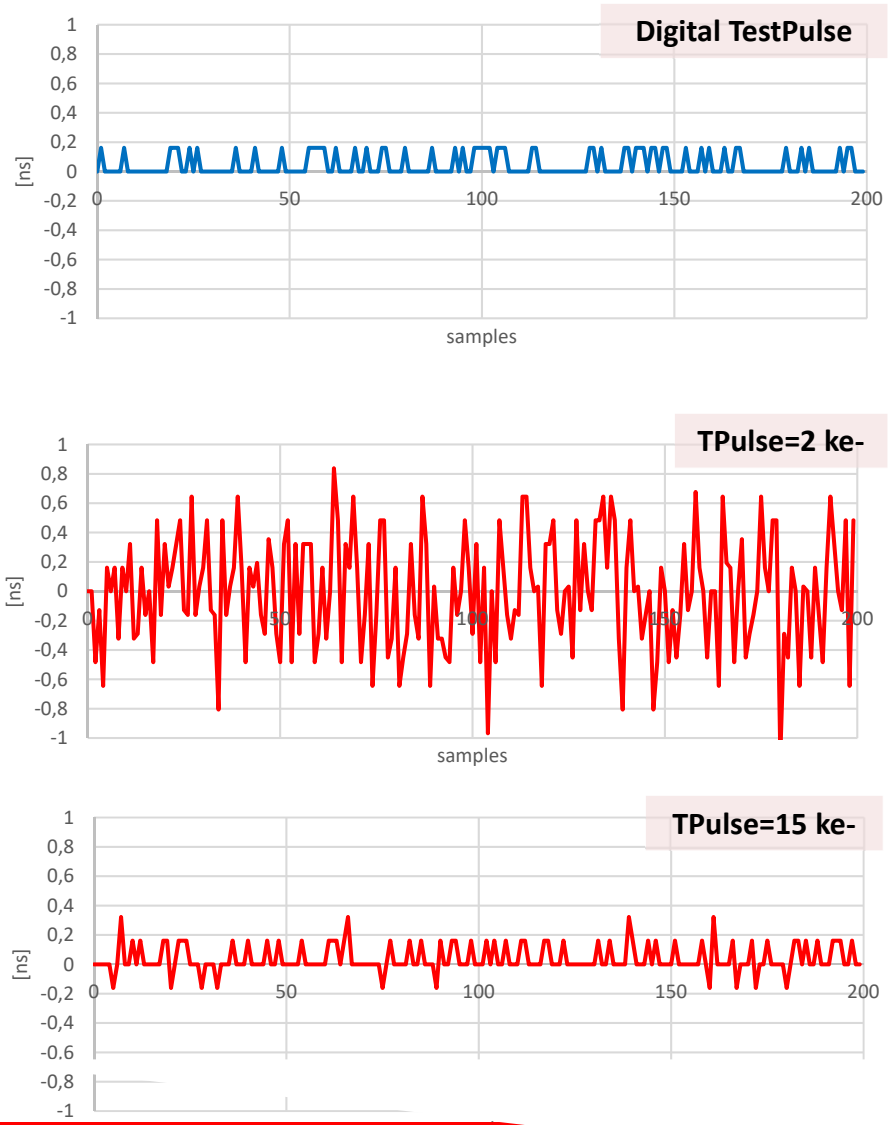


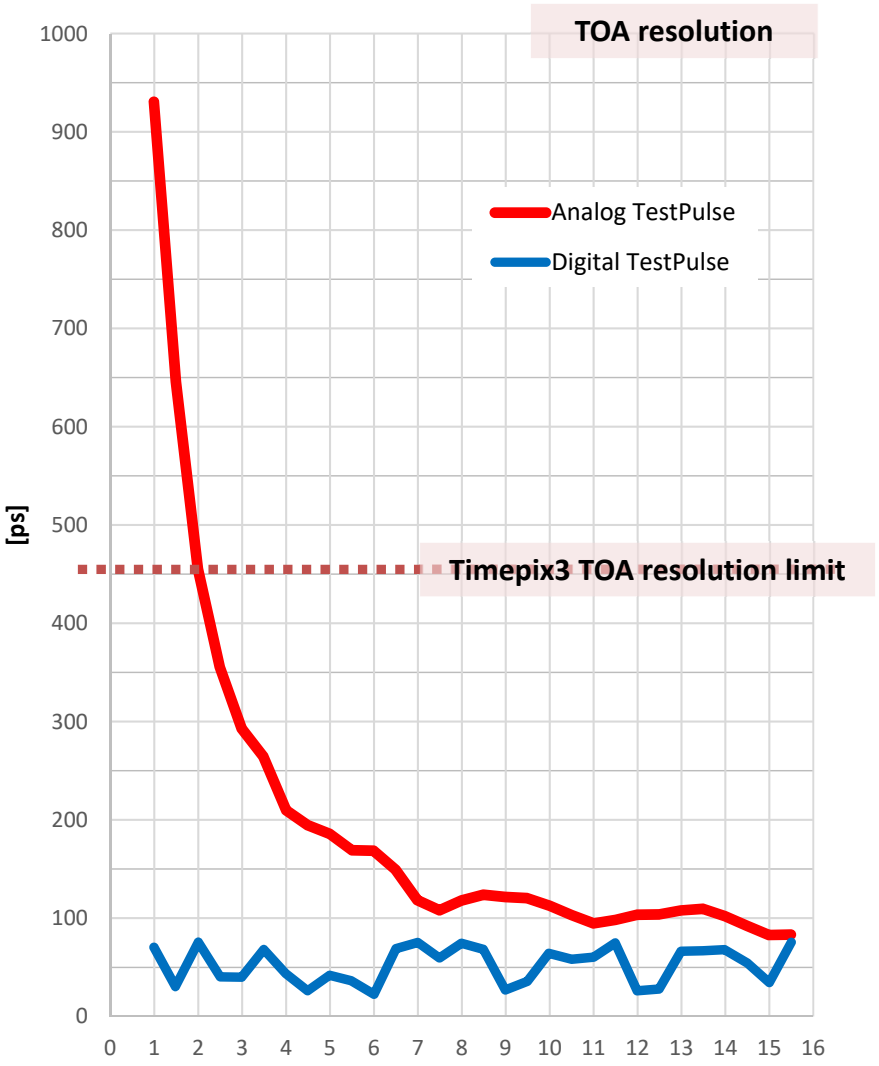
Timepix4v1



TOA Resolution (X. Llopart)

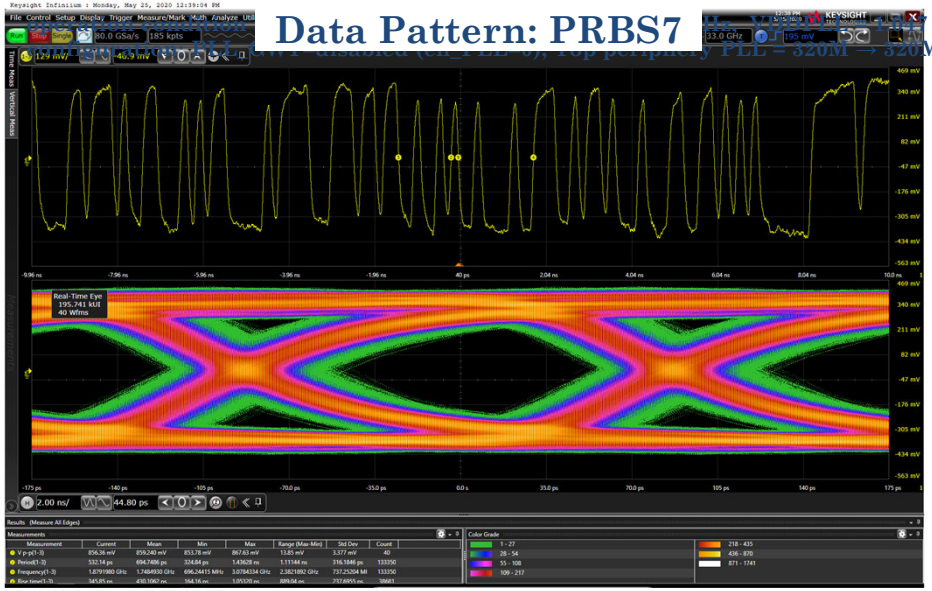
[TOA-TOT, 1 pixel, 10000 samples, HG e-]



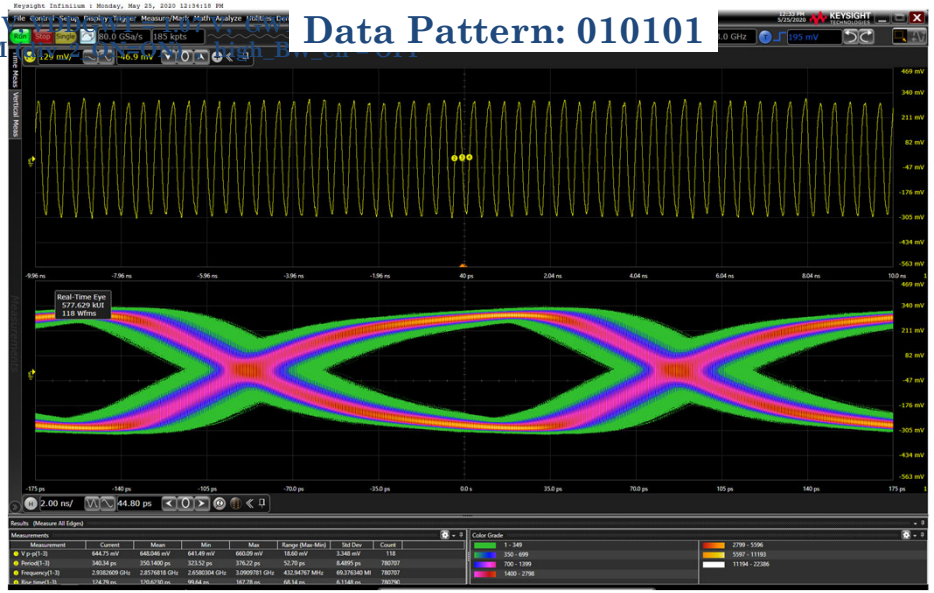


GWT-CC : 5.12Gbps Data Serializer and Wireline Transmitter

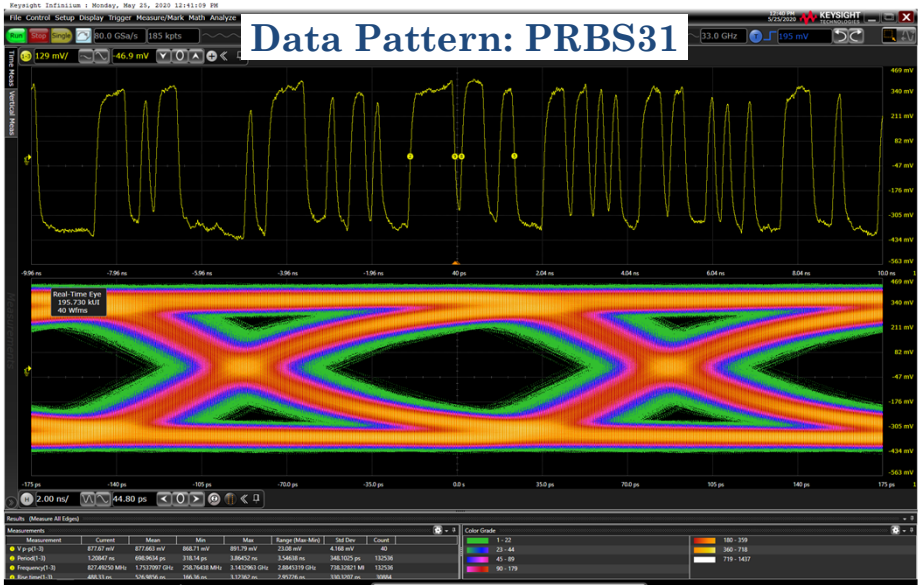
Data Pattern: PRBS7



Data Pattern: 010101

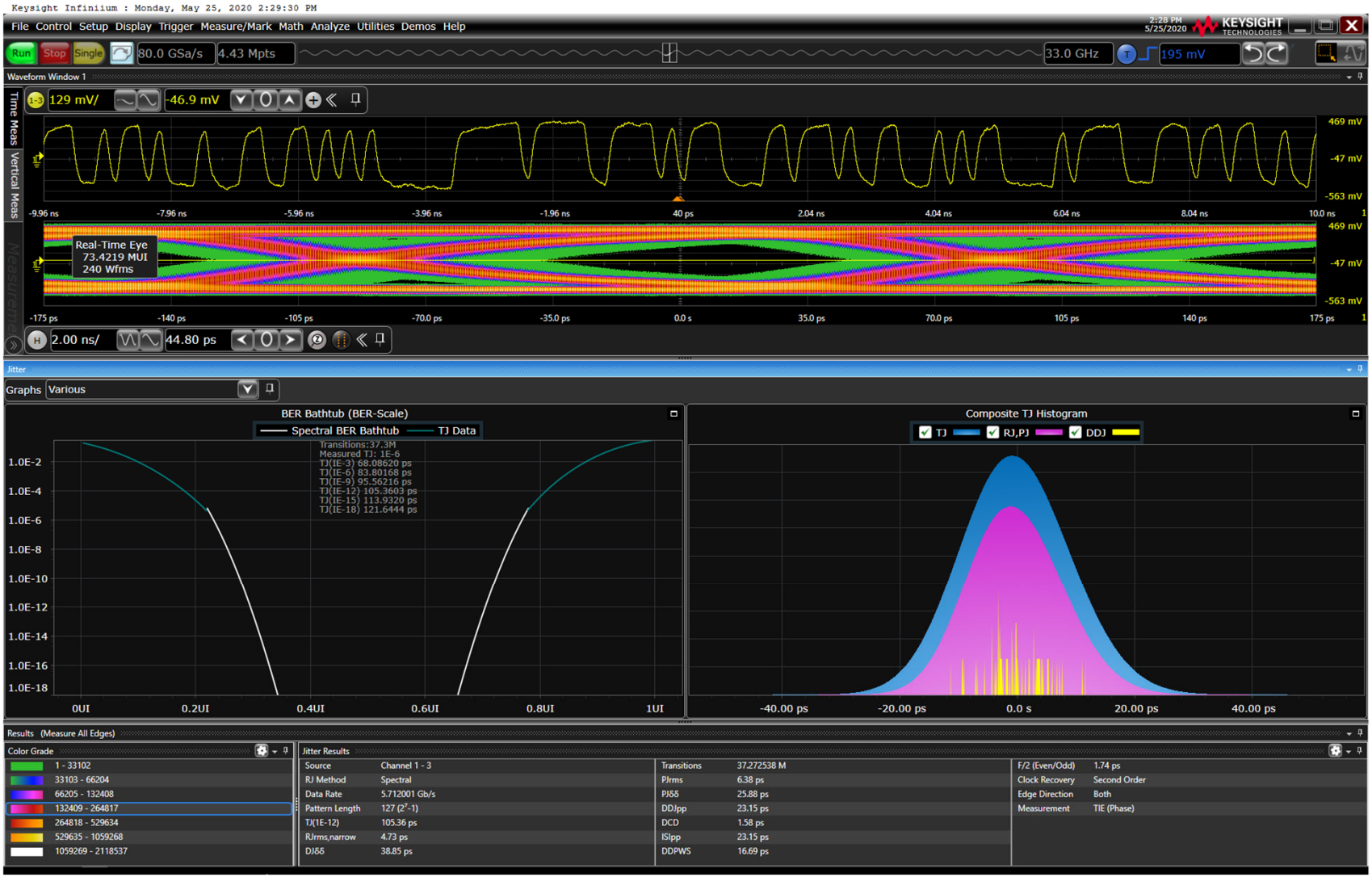


Data Pattern: PRBS31



➢ **the GWT demonstrates good eye diagrams for various data patterns**

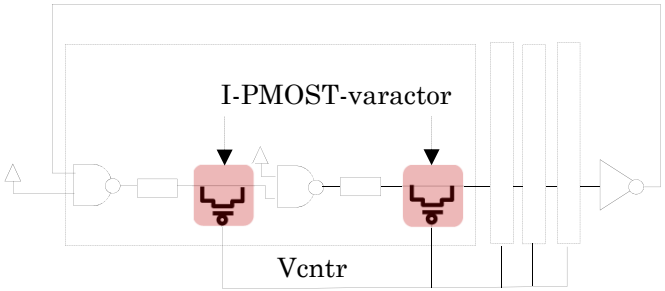
GWT-CC: Bathtub curves and jitter histogram



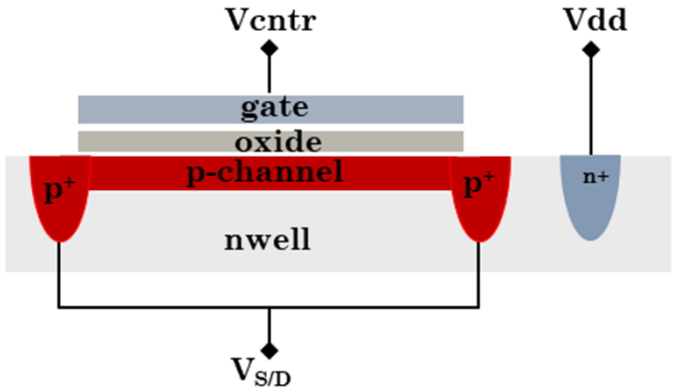
- **the scope locks on the PRBS7 orbit**
- **the shape of the jitter spectrum looks fine**
- **the sampling clock tolerance @ BER=10^{-12} is ±0.2UI = ±35ps**

PLL locking issue

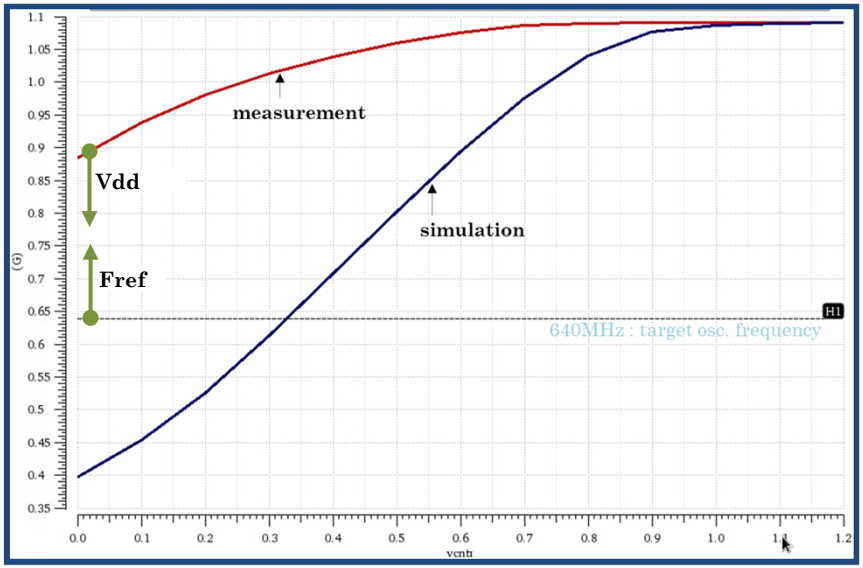
Voltage-Controlled Oscillator

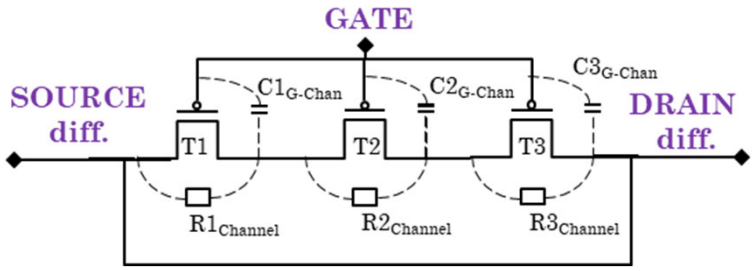


I-PMOST-varactor



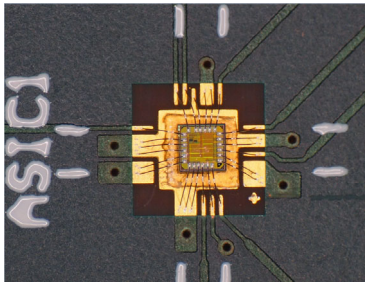
VCO control characteristic : Fosc (Vcntr)



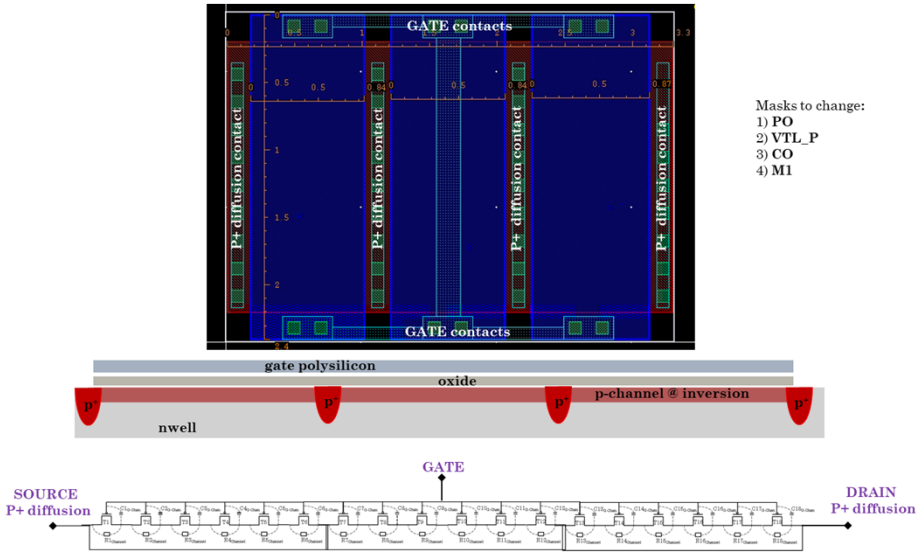


- **the VCO control characteristic is critically dependent on the modeling of the varactor capacitance**
- **a single–device model does NOT take into account the internal channel resistance in the inversion**

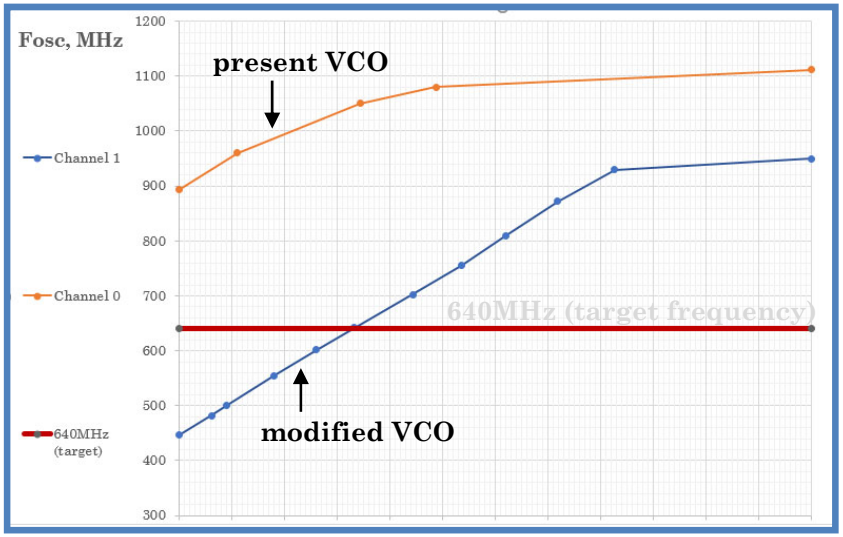
VCO modification : test chip results



New varactor:
(short-channel I-PMOST_LVT-based)



Measurements: Fosc (Vcntr)



- by changing the type of the varactor device and re-arranging the layout to use only short-channel devices it is possible to mitigate the effect of internal channel resistance
- with the new varactor the VCO will reliably lock on the target frequency

Take-home messages

➢ **Timepix4 is a new readout chip for the hybrid pixel detectors** to be used in both **the photon science and particle physics fields**

➢ the chip is developed in the frame of the **Medipix4 collaboration** , has configurable architecture to accommodate a large number of different applications

➢ the chip has the following specification:

- a **large sensitive area** (6.93 cm^2) with almost no dead area (<0.5%)
- a **4-side buttable** and therefore suitable for large-area detectors assemblies
  - **in Tracking (data driven) readout mode** :

❖ time measurement ToA: 23-bit dynamic range (1.6ms) @ **195 ps LSB**

❖ charge measurement ToT : 15-bit dynamic range @ **80e^- LSB**

❖ maximum hit rate : **3.58 x 10^6 hits/mm^2/s**

  - in **Imaging (frame-based) readout mode** :

❖ Photon Counting per pixel: **8-bit or 16-bit Continuous Read-Write (CRW)**

❖ maximum hit rate : **5 x 10^9 hits/mm^2/s**