Development of the Timepix4 chip

on behalf of the Medipix4 collaboration (https://medipix.web.cern.ch/)

Vladimir Gromov
National Institute for Subatomic Physics (Nikhef), Amsterdam, the Netherlands
- introduction and main features of the Timepix4 chip
- the circuit design aspects
- applications opportunities
- experimental results
- summary
introduction
Timepix4: Readout ASIC for hybrid pixel detectors

- **Single hit (electrical signal) pixel-level processor**
- **Features of the Timepix4 chip**

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>TSMC 65nm - 10 metal</td>
</tr>
<tr>
<td>Pixel size</td>
<td>55 x 55 µm</td>
</tr>
<tr>
<td>Chip arrangement</td>
<td>4-side buttable</td>
</tr>
<tr>
<td>3x “hidden” periphery TSV I/O</td>
<td></td>
</tr>
<tr>
<td>Pixel matrix</td>
<td>512 x 448</td>
</tr>
<tr>
<td>Sensitive area</td>
<td>6.94 cm²</td>
</tr>
<tr>
<td>Interface</td>
<td>3x 147 I/O TSV / Wirebond</td>
</tr>
<tr>
<td><strong>Tracking (data driven)</strong></td>
<td></td>
</tr>
<tr>
<td>Mode</td>
<td>ToT &amp; ToA</td>
</tr>
<tr>
<td>Data data</td>
<td>64-bit per hit</td>
</tr>
<tr>
<td>Max hit rate</td>
<td>3.58x10⁶ hits/mm²/s (10.8 KHz / pixel)</td>
</tr>
<tr>
<td><strong>Imaging (frame-based)</strong></td>
<td></td>
</tr>
<tr>
<td>Mode</td>
<td>CRW: Pixel Counter (8 /16-bit)</td>
</tr>
<tr>
<td>Frame rate</td>
<td>up to 89kFPS</td>
</tr>
<tr>
<td>Max hit rate</td>
<td>~ 5 x 10⁹ hits/mm²/s</td>
</tr>
<tr>
<td>Energy resolution @ Si sensor</td>
<td>~ 1keV FWHM</td>
</tr>
<tr>
<td>ENC @ Cin = 75fF</td>
<td>80e⁻ rms</td>
</tr>
<tr>
<td>Minimum threshold</td>
<td>~ 500 e⁻</td>
</tr>
<tr>
<td>Hit arrival timing (ToA)</td>
<td>LSB=195ps, range: 1.638ms</td>
</tr>
<tr>
<td>Charge measurement (ToT)</td>
<td>Accuracy: 80e⁻ rms, range: 200ke⁻</td>
</tr>
<tr>
<td>Data readout bandwidth</td>
<td>≤163.84 Gbps (16x @ 10.24 Gbps)</td>
</tr>
<tr>
<td>Power Supply Voltage</td>
<td>1.2V</td>
</tr>
<tr>
<td>Power</td>
<td>~3.5W</td>
</tr>
</tbody>
</table>

- Timepix4 is a fully digitally-controlled, 4-side tillable large-area, single threshold pixel readout chip with improved energy and time resolution and with high-rate imaging capabilities
Multi-purpose pixel readout chip for Medipix4 collaboration

Particle identification and tracking
Photon (hit) detection time-resolved & energy-resolved:

- High-Energy Physics (HEP):
  - very high rate pixel telescope
  - ultra-fast sensor studies for HL-LHC
  - beam gas interaction (PS SPS/LHC)
  - ATLAS background rad monitor and TRD detector
  - large area gas-filled TPC for ILC

- Time-of-flight mass spectrometry
- Neutron time-of-flight imaging
- Radiation monitors
- Electron microscopy
- X-ray and powder diffraction
- Compton camera for medical diagnostics
- Gamma and neutron imaging for nuclear industry and Homeland Security

Imaging applications:
- X-ray imaging in synchrotrons with extreme high rates > 10^8 particles/mm^2/s

20th Anniversary Symposium on Medipix and Timepix
https://indico.cern.ch/event/782801/

- Timepix4 a multi-application device is not fully optimized for a particular application
main features
Tracking readout mode: particle track detection / energy-resolved and time-resolved photon (hit) detection

- the data packet is created and read out immediately after the hit occurred
- the bandwidth of the data readout system can be adjusted to match the hit rate
- the hit charge info (ToT) can also be used for the correction of the time info (ToA)

<table>
<thead>
<tr>
<th>output bandwidth max / min</th>
<th>hit rate</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>per pixel</td>
</tr>
<tr>
<td>163 Gbps</td>
<td>10.8 KHz</td>
</tr>
<tr>
<td>40 Mbps</td>
<td>2.6 Hz</td>
</tr>
</tbody>
</table>

Sparsely distributed hits: zero data-suppressed, continuous, Data-Driven readout
Imaging readout mode: on-pixel hit counting

- Continuous data taking and pixel matrix readout with two hit counters per pixel
- The on-pixel hit counter is read out regularly once per frame

<table>
<thead>
<tr>
<th>Output bandwidth max / min</th>
<th>Frame rate</th>
<th>Hit rate per mm²</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>8-bit</td>
<td>16-bit</td>
</tr>
<tr>
<td>163 Gbps</td>
<td>89 KHz</td>
<td>45 KHz</td>
</tr>
<tr>
<td>40 Mbps</td>
<td>21 Hz</td>
<td>11 Hz</td>
</tr>
</tbody>
</table>

- NO zero data suppression
- 8-bit or 16-bit pixel counter depth

packet A <63:0> = pixel counter 7_1 <63:56>, pixel counter 6_1 <55:48>, ... , pixel counter 0_1<7:0>
High-volume and high-speed data readout

- the bandwidth of the data readout is high up to 163.8 Gbps: \(2.56 \times 10^9\) packets/sec
- the bandwidth the data transport components match to each other
- multi-level FIFO architecture with the push-back overflow control

Output Serializers
max bandwidth: 81.92 Gbps

Pixel Matrix → End-of-Column
max bandwidth: 95.6 Gbps

End-of-Column → End-of-Chip
max bandwidth: 81.92 Gbps

Data transport architecture

TOP half

Pixel Matrix [448 x 256 pixels]

750.4 Mpackets/s
(112x up to 6.7 Mpackets/s @ 40MHz)

End-of-Column

End-of-Chip

max bandwidth: 81.92 Gbps

8x64b @ 40 - 160MHz

8x8 Router

5.12 Gbps or 10.24 Gbps

32b @160MHz or 32b @320MHz

32b @160MHz or 32b @320MHz

5.12 Gbps or 10.24 Gbps

PCSTX [0]

GWT-CC [0]

PCSTX [7]

GWT-CC [7]

The bandwidth of the data readout is high up to 163.8 Gbps: \(2.56 \times 10^9\) packets/sec

The bandwidth the data transport components match to each other

Multi-level FIFO architecture with the push-back overflow control
the pixel-level circuit:
- digitizes all the information contained in the hits
- adds pixel coordinate information
- sends the data packet to the periphery of the chip

the local oscillator (VCO) starts to generate a 640MHz clock when it is triggered by the hit. The VCO runtime is limited by the period of a 40MHz reference clock to 25ns
Hit charge quantization: Time-over-Threshold method (ToT)

Charge sensitive amplifier (CSA) with a Krummenacher feedback network ($I_{fb} = I_{KRUM} = const$)

- a 640MHz local VCO clock pulses and a 40MHz reference clock pulses pass through the clock gating block and are counted giving the digital representation of the measured charge $Q_{in}$
- the range of the ToT method is limited by the value of the charge-storing capacitance $C_{in} + C_{fb}$
- the precision of the ToT method is limited by the noise ($ENC = 80e^{-}$ rms)
- this corresponds to a 288eV rms energy resolution in silicon sensors ($3.67eV/e^{-}$)

<table>
<thead>
<tr>
<th>$I_{KRUM} = 18nA$</th>
<th>ToT uncertainty</th>
<th>0.6ns rms .. 0.7ns rms</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{KRUM} = 1nA$</td>
<td>ToT quantization error</td>
<td>0.5ns rms ~$63e^{-}$ rms</td>
</tr>
<tr>
<td>$I_{KRUM} = 1nA$</td>
<td>ToT uncertainty</td>
<td>13ns rms 13ns rms 15ns rms</td>
</tr>
<tr>
<td>$I_{KRUM} = 1nA$</td>
<td>ToT quantization error</td>
<td>0.5ns rms ~$3e^{-}$ rms</td>
</tr>
</tbody>
</table>
Hit arrival time (ToA) quantization: a 195ps TDC per pixel

Time-to-digital conversion: the signals

- Hit
- Preamplifier
- Discriminator
- Reference clock (40MHz)
- VCO Start/Stop
- VCO phases (640MHz)
- Loop state
- Loop Counter
- Global ToA (16-bit @ 40MHz)

TDC block diagram

- Front-end
- Counter & Latches
- Pixel

- Start/Stop VCO 640MHz
- OR
- Ref. clock
- Data

- The resolution of the TDC is limited by the size of the VCO loop state (195ps = 1/640MHz / 8)
- The dynamic range of the TDC is set by the duration of the global timing orbit (1.638ms = 16bit@40MHz)
- The VCO consumes significant current (~500uA) when it is running
- The VCO power consumption is negligible due to a low running duty cycle (~10^-3)
Hit arrival time (ToA) : accuracy limiting effects

- the performance of the Front-end circuit (preamplifier, discriminator) limits the accuracy of the timing measurements (time-walk, noise time-jitter)
- a 195ps ToA accuracy can be achieved only for the large-size hits with Qin > 10 ke-
- the ToT charge information will be used to identify the large-size hits
- for small-size hits (< 10ke-) : the ToA @ ToT time-walk correction is feasible
  
  \[
  \text{ToA rms} = \text{ToT rms} \cdot \frac{\Delta \text{ToA}/\Delta \text{Qin}}{2000} = 80 \text{ e- rms} \cdot \frac{3000 \text{ ps}}{2000 \text{ e-}} = 120 \text{ ps rms}
  \]
  
  - however the ToA noise jitter is still very high >> LSB (195ps)
“Hidden” peripheries with TSV (Through-Silicon-Vias)

- Chip surface utilization is high > 99.5% active area

- Timepix4

- V.Gromov

- 12/06/20
4-sides stitching of the Timepix4 ASIC-level modules

- the TSV technology allows for a 4-sides stitching of the ASIC-level modules to construct large-area detectors
- the large-area detector is almost-dead-area-free: > 99.5% active area
the circuit design aspects
**Timepix4: Digital-on-Top (DoT) design methodology**

**Design Strategy & Top Level Integration (X. Llopart)**

- Design specifications closed 2 years ago
- Top level chip floorplan realized at a very early stage
- Use the digital on top flow
  - All analog blocks designed as “islands” inside digital flow
    - Required careful physical and functional characterization before integration
  - Digital logic is used as “glue” between analog blocks
- Use of UVM as system level functional verification
  - Allows full chip top level simulations \(\rightarrow\) Impossible using analog simulators
- Extensive use of repositories (GitLab, ClioSoft) allowed versioning and save file sharing between the design team
- Total design time of \(~3\) years with 9 engineers \(\rightarrow\) \(~12.5\) FTE

- ASIC designers:
  - CERN (Geneve): R. Ballabriga, T. Poikela, E. Santin, V. Sriskaran, N. Egidos, X. Llopart
  - Nikhef (Amsterdam): V. Gromov, A. Vitkovskiy
  - IFAE (Barcelona): R. Casanova
The chip can be controlled/readout in either single-periphery or multi-periphery configuration.

**High-Speed data Readout:**
- 16 x 5.12 Gbps /10.24 Gbps Serial links (±0.6V @ Rterm=100 Ω)

**Custom Slow Control protocol:**
- write / read configuration registers
- pixel matrix configuration > 2 Mb (8-bit/pixel + 24-bit/SPGroup)
- peripheral registers (DAC settings, operation modes, e-fuses, ...)
- readout pixel matrix in the test mode @ 40MHz
- point-to-point connection between the chip and the readout system

**I2C control protocol:**
- on-chip adapter from I2C slave to the Slow Control

**Global control signals:**
- Data Acquisition time window (SHUTTER)
- Synchronization of Global Time Stamp counter (TO_SYN)
- External reset (RESET)

**Resets procedure:**
- periphery logic reset: concurrent
- pixel matrix reset: sequential

**External clocks:**
- Slow control clock (< 40MHz) (SC_CLOCK_IN)
- PLL Clock reference (40MHz / 320MHz) (CLK_REF_PLL)
- I2C Clock (SCL_I2C)

**Internal clock generation:**
- configurable PLL circuits (320MHz / 640MHz outputs)

**Monitoring / debugging:**
- internal-generated analog signals via an on-chip ADC (DAC_OUT)
- internal digital signals (TEST_OUT)
Uniformity of the power supply voltage across the chip

Analog (static) power supply distribution (simulated by X. Llopart)

<table>
<thead>
<tr>
<th></th>
<th>2WB</th>
<th>3TSV</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Nominal Analog Power</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[10 µA/pixel]</td>
<td>$V_{\text{drop}}$ [max-min]</td>
<td>19.6 mV</td>
</tr>
<tr>
<td></td>
<td>$I_{\text{max pad}}$</td>
<td>60 mA</td>
</tr>
<tr>
<td><strong>Low Analog Power</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[1 µA/pixel]</td>
<td>$V_{\text{drop}}$ [max-min]</td>
<td>1.96mV</td>
</tr>
<tr>
<td></td>
<td>$I_{\text{max pad}}$</td>
<td>6 mA</td>
</tr>
</tbody>
</table>

- the power supply voltage IR drop across the pixel matrix is very low (6.9mV) when a 3-side bonding scheme is used
Dynamic and Static Power as a function of hit rate in the Tracking (data driven) readout mode (simulated by X. Llopart)

- the on-pixel analog front-end circuit is the largest contributor to the power budget (9uA/pixel @ 1.2V = 10.8uW/pixel)
The versatile front-end:
- is compatible with various sensors (solid-state, gas-filled ...)
- optimized for high hit rate operation (dead time < 200ns)
- optimized a 195ps hit arrival time accuracy
the VCO consists of 4 RC-delay cells taking only 1% area in the layout of the pixel matrix
the VCO control voltage is generated in the common PLL, locked to the target oscillation frequency (640MHz)
in this schema the VCO oscillation frequency is immune to the process corner and the temperature variation
the VCO can also be tuned individually to compensate for the fabrication mismatch in the range 2.5%
a ±1mV dynamic voltage drop on the power supply busses will not cause an error more than 1/2 LSB
Reference time clock delivery to the on-pixel TDC

Chip-level ref. clock tree

- **“Top” TSVs & periphery**
- **“Middle” TSVs & periphery**
- **“Bottom” TSVs & periphery**

Symmetrical clock tree up to the inner superpixels

**Specifications**

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>reference time clock frequency</td>
<td>40MHz</td>
</tr>
<tr>
<td>number of the dDDL blocks per chip</td>
<td>448</td>
</tr>
<tr>
<td>SPGroup – to – SPGroup delay</td>
<td>780ps</td>
</tr>
<tr>
<td>delay skew uncertainty</td>
<td>&lt; 100ps</td>
</tr>
<tr>
<td>total power per chip (dDLL contribution)</td>
<td>157mW</td>
</tr>
</tbody>
</table>

- The reference time clock is delivered to each on-pixel TDC with an uncertainty less than 100ps

**digital DLL per Double Column**

(Designer E. Santin)

[Diagram of digital DLL per Double Column]

**Specifications**

- reference time clock frequency: 40MHz
- number of the dDDL blocks per chip: 448
- SPGroup – to – SPGroup delay: 780ps
- delay skew uncertainty: < 100ps
- total power per chip (dDLL contribution): 157mW

Reference time clock delivery to the on-pixel TDC

https://iopscience.iop.org/article/10.1088/1748-0221/14/01/C01024/pdf
Timepix4: Generic PLL

- reference PLL to generate Vcntr for the on-pixel VCOs
- a 320MHz/640MHz clock generator for the periphery logic
- a 320MHz clock-cleaning PLL in the high-speed (5/12/10.24Gbps) data serializer block

internal time jitter : < 50ps p-p

- MOSCAP_rf25 thick gate oxide capacitance (low leakage )
- DNW for better substrate isolation
- separate power supply voltage domain

used as:

- reference PLL to generate Vcntr for the on-pixel VCOs
- a 320MHz/640MHz clock generator for the periphery logic
- a 320MHz clock-cleaning PLL in the high-speed (5/12/10.24Gbps) data serializer block

internal time jitter : < 50ps p-p

- MOSCAP_rf25 thick gate oxide capacitance (low leakage )
- DNW for better substrate isolation
- separate power supply voltage domain
Clock-cleaning PLL configuration

Suppression of the jitter of the reference clock

- high-frequency jitter = sudden jumps of the clock edges will be suppressed by the PLL-CC circuit
- low-frequency jitter = long-term (accumulated) shift of the clock edges will be suppressed by the off-chip in the clock-and-data recovery circuit (CDRPLL)
GWT-CC : 5.12/10.24Gbps Data Serializer and Wireline Transmitter

- successor of block used in the VeloPix
- selective data rate: 5.12Gbps/10.24Gbps
- bypassable clock-cleaning PLL (ring-oscillator): internal jitter < 30ps p-p
- NO high-frequency external clocks: ≤ 320MHz
- voltage-mode transmitter: output swing = ±0.6V @ Rterm=100Ω
- low power : 24mW
GWT-CC: 1/16-Rate Multiplexer-based architecture

- 16-bit input data: byte-interleaved internally (both-edge-clocked)
- Internal DLL used to generate 16 phases controlling the Multiplexer
- **area**: $4 \times 10^4 \, \mu\text{m}^2$
- **local (dedicated) power supply connections**: TSV / Wirebond pads
- **deep N-well (DNW) substrate isolation of the analog cores**
- **current-leakage-free large-area capacitances**: thick gate-oxide varactor
- **local power supply grid M4/M5**
Timepix4: Physical Coding Sublayer Transmitter (PCS TX)

Top-level diagram (designer A. Vitkovskiy)

- **8x8 Router**
  - 20-160MHz
  - 80/160MHz
  - 160/320MHz
  - 160/320MHz
  - 5.12/10.24GHz

- **64B/66B Encoder**
  - 64B/66B data Encoder
  - IEEE802.3ae standard
  - packet starts with LSB / MSB
  - 3.125% data overhead
  - data packet alignment

- **Encoder bypass mode**

- **Data scrambling**
  - initial value is a zero-vector

- **Serial data speed control**
  - by multiplying data stream bits
  - 5.12/10.24Gbps → 40/80Mbps

- **Test pattern generation**
  - square wave
  - pseudo-random
  - PRBS-31, PRBS-23, PRBS-15, PRBS-7

- **GWT**
  - Digital IF
  - Serializer
  - 1 bit

- **Digital IF**

- **Serializer**

- **Features**

  - provides an interface between the Packet Router block and the GWT-CC block

  - 64B/66B data Encoder
    - IEEE802.3ae standard
    - packet starts with LSB / MSB
    - 3.125% data overhead
    - data packet alignment

  - Encoder bypass mode

  - Data scrambling
    - initial value is a zero-vector

  - Serial data speed control
    - by multiplying data stream bits
    - 5.12/10.24Gbps → 40/80Mbps

  - Test pattern generation
    - square wave
    - pseudo-random
    - PRBS-31, PRBS-23, PRBS-15, PRBS-7
Timepix4: implementation of the PCS TX block

Block diagram (designer A. Vitkovskiy)

- Input Asynchronous FIFO:
  - clock-domain-crossing
  - data backpressure compensation

- Scrambler:
  - randomizes the bit stream for disparity correction between 1’s and 0’s

- Pseudo-Random Pattern Controller:
  - enables test mode

- Gearbox:
  - add 2 bits synch header
  - transmits 32 data blocks in 33 clock cycles to keep a 64b input/output data stream

- Bit Splitter:
  - serial speed control by repeating of the bits in the data stream

- this highly-configurable and multi-functional topology makes the readout of the chip compatible with various telecommunication standards and computer networking technologies (10 Gigabit Ethernet)

- the bandwidth of the data transfer is fully digitally-controlled
- 12-bit $\Sigma\Delta$ ADC (designer R. Casanova)
Monitoring 12-bits Fully Differential Second Order Incremental Delta Sigma Converter ADC for Timepix4” – TWEPP 2019
spec: conversion rate up to 1190 samples / sec , power: 8uW
monitors internal signals:
- internal power supply drop (analog and digital core supply)
- BG and temperature monitor
- DAC Biasing voltages
- BandGap reference circuit (designer S. Michelis)
spec: Vout = 330mV,
maximum output deviation in absolute value: ±1.1% (process) & ±1.6% (mismatch)
gradient=6.2uV / °C , noise =180uV @ BW=100MHz ,
power =240uW , Enclosed Layout diode

➢ the Timepix4 chip in fully digitally controlled and monitored (NO analog input/output signals)
application opportunities
The Timepix4 ASIC can be used to build large-area TPC detectors. Its small pixel size (55µm) & high time resolution (195ps) are useful for 3D tracking.
A 4D real-time tracking in VELO sub-detector for the LHCb Upgrade II

Tracks reconstruction in High-Luminosity environment

- hit time stamp gives an extra dimension in the track reconstruction
- a < 50ps time resolution is required for efficient 4D tracking in the HL-LHC environment
- the Timepix4 ASIC (195ps time of arrival bin size) will be used as a test vehicle
Single-photon imaging detector with sub-100 ps and < 10µm resolutions

- the MCP detector internally has high spatial (<20µm) and temporal (<100ps) resolutions
- it can fully exploit high position (55µm) and time resolution (195ps) of the Timepix4 chip

https://doi.org/10.1016/j.radmeas.2019.106228
Molecular imaging with the Timepix4 readout

- The time-of-flight (ToF) is used to calculate mass-to-charge value of the secondary ions
- With a 195ps event time-tag in the Timepix4 chip, very high mass resolution is feasible

### Time-of-Flight (ToF) mass spectrometer

![Diagram of Time-of-Flight (ToF) mass spectrometer]

**Timepix4 :**

- Tracking (event-based) readout mode
- Dead-time free operation
- Continuous Data driven readout

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time-of-arrival (ToA) accuracy</td>
<td>195ps</td>
</tr>
<tr>
<td>Mass resolution (feasible)</td>
<td>m/dm → 30000</td>
</tr>
<tr>
<td>Max Hit rate</td>
<td>3.58 x 10^6 hits/mm^2/s</td>
</tr>
<tr>
<td>Spatial resolution (pixel size)</td>
<td>55µm x 55µm</td>
</tr>
</tbody>
</table>

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X-ray imaging with the Timepix4 readout

**Medical imaging systems**

- X-ray source (<10KeV)
- Target object
- Si sensor
- Timepix4 ASIC
- PCB Interface

**Timepix4**: frame-based readout mode

<table>
<thead>
<tr>
<th>Feature</th>
<th>Dead-time free operation</th>
<th>Continuous Read/Write (CRW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>On-pixel counter</td>
<td>8 bit</td>
<td>16 bit</td>
</tr>
<tr>
<td>Max Frame rate</td>
<td>89kFPS</td>
<td>44kFPS</td>
</tr>
<tr>
<td>Max Hit rate</td>
<td>~ 5 x 10^9 hits/mm²/s</td>
<td></td>
</tr>
<tr>
<td>Spatial resolution (pixel size)</td>
<td>55µm x 55µm</td>
<td></td>
</tr>
</tbody>
</table>

- the maximum hit rate is limited by the pulse shaping time in the analog front-end (~200ns) and not by the bandwidth of the readout system
X-ray liquidography: the time evolution of the induced structural changes in molecules

an optical laser pulse initiates photo-chemistry of a molecule of the sample

an X-ray pulse to scatter from the sample

train of the X-ray pulses

Synchrotron

➢ the Timepix4 ASIC is very much suitable for a time-resolved diffraction image readout system
➢ in Tracking readout mode there will be good time resolution between the diffraction images for each X-ray pulse in the train
### Timepix4 and the European XFEL facilities

<table>
<thead>
<tr>
<th></th>
<th>XFEL</th>
<th>Timepix4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single pulse size /</td>
<td><strong>1 – 1000 photons</strong> (12.4keV) per pixel (55um x 55um)</td>
<td><strong>500e⁻ ... 800ke⁻</strong> (@ log gain mode)</td>
</tr>
<tr>
<td>Dynamic range</td>
<td><strong>3ke⁻ ... 3000ke⁻</strong></td>
<td></td>
</tr>
<tr>
<td>Single pulse processing</td>
<td>&lt; 200ns</td>
<td>&lt; 200ns (@ Ikrum&gt;10nA)</td>
</tr>
<tr>
<td>time</td>
<td></td>
<td></td>
</tr>
<tr>
<td>On-pixel memory depth</td>
<td><strong>2700 X-ray pulses every 200ns in a 600usec train</strong></td>
<td>1-2</td>
</tr>
</tbody>
</table>

- the European XFEL has an extremely irregular time structure of the X-ray flux
- the Timepix4 ASIC is NOT optimized for such operation conditions
the Timepix4 ASIC can be combined with different sensors (1mm Si or 2mm CdTe) to build both the Scatter detector and the Absorber detector

the Timepix4 ASIC delivers a full set of data for each single event needed to estimate the possible direction of the original gamma

Compton scattering effect

\[ \cos \theta = 1 - \frac{m_ec^2}{E_0 (E_0 - E_1)} \]

\[ E_0 = E_1 + E_2 \]

Schema of the Compton camera

<table>
<thead>
<tr>
<th></th>
<th>Dead-time free operation</th>
<th>Continuous Data driven readout</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time-of-arrival (ToA) accuracy</td>
<td>195ps</td>
<td></td>
</tr>
<tr>
<td>Energy measurement accuracy</td>
<td>300eV rms</td>
<td></td>
</tr>
<tr>
<td>Spacial resolution (pixel size)</td>
<td>55µm x 55µm</td>
<td></td>
</tr>
<tr>
<td>Max Hit rate</td>
<td>3.58 x 10^6 hits/mm²/s</td>
<td></td>
</tr>
</tbody>
</table>
experimental results
Timepix4: test system

SPIDR4 control and readout system (designer Bas van der Heijden, basvdh@nikhef.nl)

- SPIDR4 readout system from Nikhef
- SPIDR4 Chipboard + Timepix4
- Timepix4 is wirebonded from TOP and BOT periphery WB pads
- Timepix4 accessed (slow control) through TOP periphery
  - Bottom periphery IO is not fully connected due to PCB design error

Interface: 1Gbps Internet
Data optical readout: 2 x 10Gbps Internet (Timepix4 readout @ 2x 5.12Gbps)
2x Firefly 12TX E-O module (BW=16x10.24Gbps)
ENC full matrix (X.Llopart)

**Timepix4v0**

- Excess ENC noise on top of peripheries (x2-4):
  - ~26 rows: [0:7] [250:260] [504:511]

  ![ENC 160 e⁻ rms](image1)

  ![ENC 50 e⁻ rms](image2)

**Timepix4v1**

  ![ENC 58 e⁻ rms](image3)

  ![ENC 72 e⁻ rms](image4)
TOA Resolution (X. Llopart)

[TOA-TOT, 1 pixel, 10000 samples, HG e-]

Digital TestPulse

TOA resolution

Analog TestPulse
Digital TestPulse

Timepix3 TOA resolution limit

12/06/20


GWT-CC: 5.12Gbps Data Serializer and Wireline Transmitter

- Operation condition: external clock (CLK_REF_PLL) = 357 MHz, VDDPLL = 1.047 V, VDDGWT = 1.07 V, GWT bit rate = 5.71Gbps

- Configuration: PLL_GWT=disabled (en_PLL=0), Top periphery PLL = 320M (div_2_ON=ON), high_BW_en = OFF

- Data Pattern: PRBS7, Data Pattern: PRBS31, Data Pattern: 010101

- The GWT demonstrates good eye diagrams for various data patterns

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Nikhef Timepix4 V.Gromov 12/06/20
GWT-CC: Bathtub curves and jitter histogram

- The scope locks on the PRBS7 orbit.
- The shape of the jitter spectrum looks fine.
- The sampling clock tolerance @ BER=10^{-12} is ±0.2UI = ±35ps.
PLL locking issue

Voltage-Controlled Oscillator

I-PMOST-varactor

VCO control characteristic: $F_{osc}$ ($V_{cntr}$)

- the VCO control characteristic is critically dependent on the modeling of the varactor capacitance
- a single–device model does NOT take into account the internal channel resistance in the inversion
by changing the type of the varactor device and re-arranging the layout to use only short-channel devices it is possible to mitigate the effect of internal channel resistance

- with the new varactor the VCO will reliably lock on the target frequency
Take-home messages

- **Timepix4** is a new readout chip for the hybrid pixel detectors to be used in both the photon science and particle physics fields.
- The chip is developed in the frame of the **Medipix4 collaboration**, has configurable architecture to accommodate a large number of different applications.
- The chip has the following specification:
  - **A large sensitive area** (6.93 cm²) with almost no dead area (<0.5%).
  - **4-side buttable** and therefore suitable for large-area detectors assemblies.
  - **In Tracking (data driven) readout mode:**
    - Time measurement ToA: 23-bit dynamic range (1.6 ms) @ **195 ps LSB**
    - Charge measurement ToT: 15-bit dynamic range @ **80 e⁻ LSB**
    - Maximum hit rate: **3.58 x 10⁶ hits/mm²/s**
  - **In Imaging (frame-based) readout mode:**
    - Photon Counting per pixel: **8-bit or 16-bit Continuous Read-Write (CRW)**
    - Maximum hit rate: **5 x 10⁹ hits/mm²/s**