The Upgrade of the Inner Tracker of the ATLAS experiment for the High-Luminosity LHC

Joint Instrumentation Seminar
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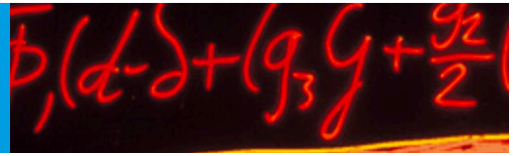
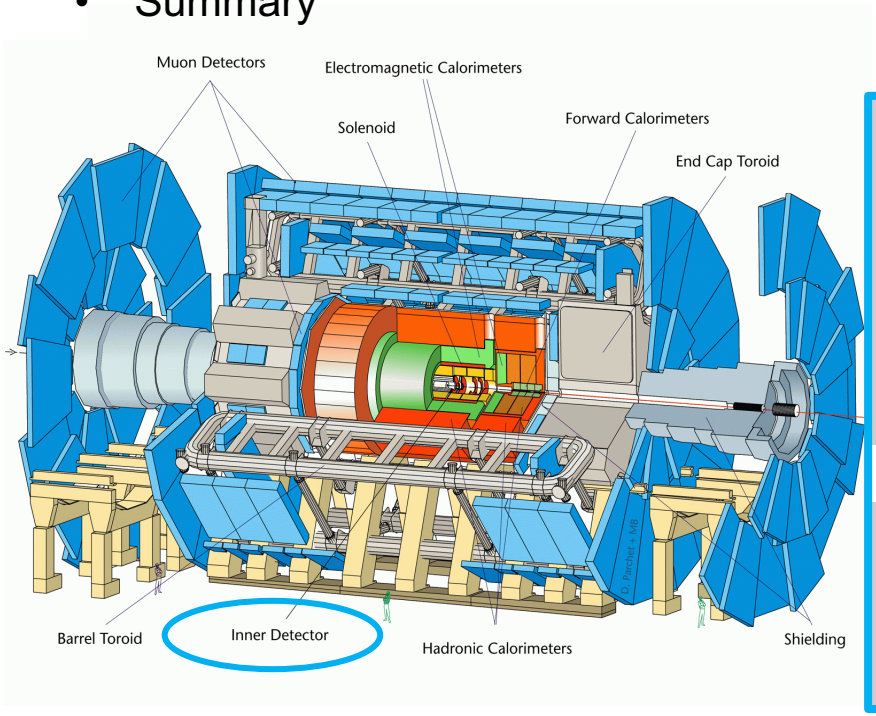
Susanne Kuehn, CERN

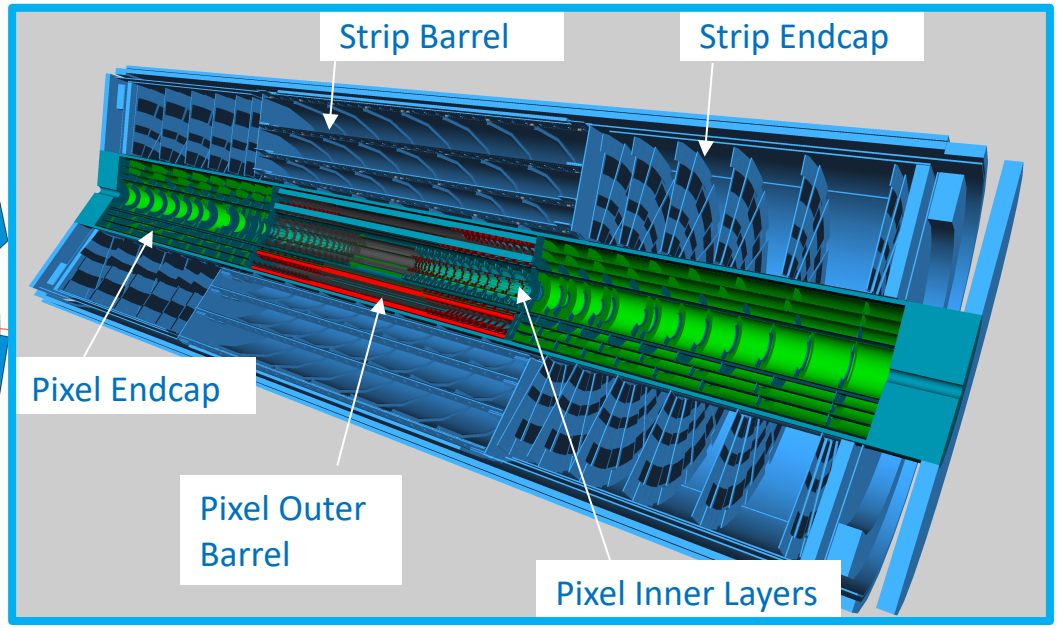
INSTRUMENTATION SEMINAR
Joint Instrumentation Seminar



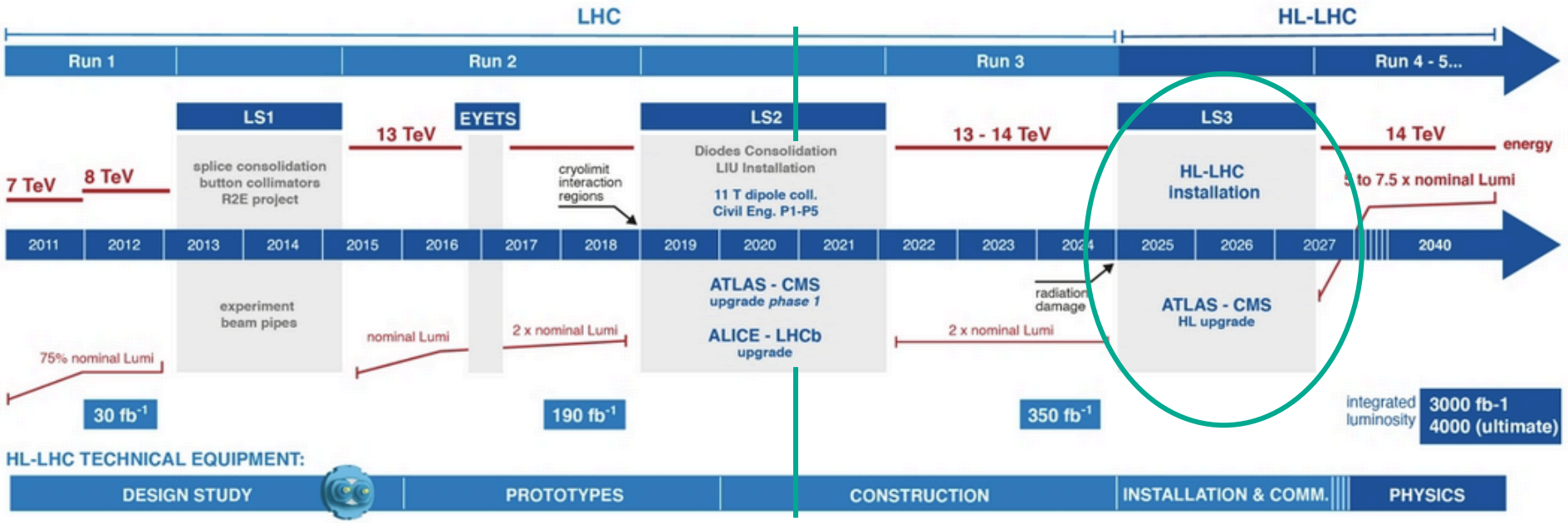
Overview

- The Phase-II Upgrade of the Large Hadron Collider and of the inner tracking detector of the ATLAS experiment
- Motivation and layout of the Inner Tracker (ITk) detector
- Concept, technology choices and results of prototyping of
  - the strip detector
  - the pixel detector
- Summary





Phase-II Upgrade of the Large Hadron Collider



https://hilumilhc.web.cern.ch/

From LHC to HL-LHC

Proton-proton collisions with up to 14 TeV at higher intensity:

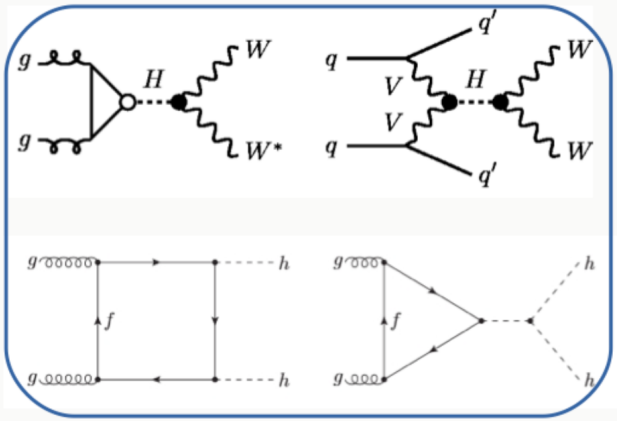
Instantaneous nominal luminosity x5-7.5 → Increased particle densities
Integrated luminosity x10 → Increased radiation damage
→ Increase of overlapping proton-proton events (pile-up) from <μ> ~ 50 now to <μ> ~ 200

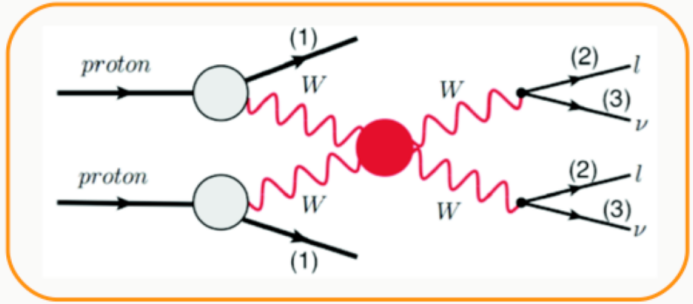
Upgrade Physics Goals

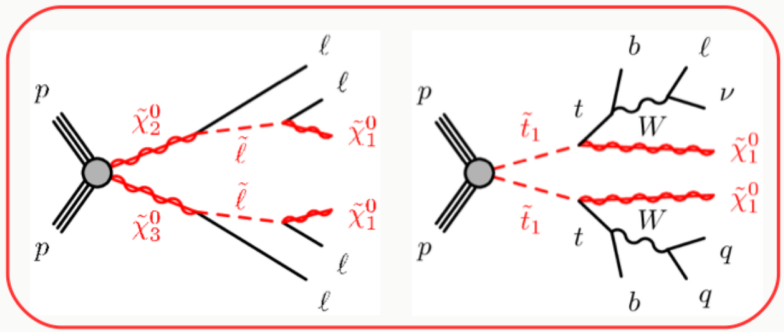
- **Improve Higgs boson precision measurements**
  - More precise measurements of Higgs boson couplings
  - Di-Higgs boson production
  - Study of Higgs boson self coupling

- **Vector Boson Scattering** and other precision SM measurements
  - VBS cross section

- **Search for New Physics**
  - Mass reach for new particle searches extends significantly, e.g. for stops to 1.2 TeV
  - Direct production of staus, stops, EW gauginos







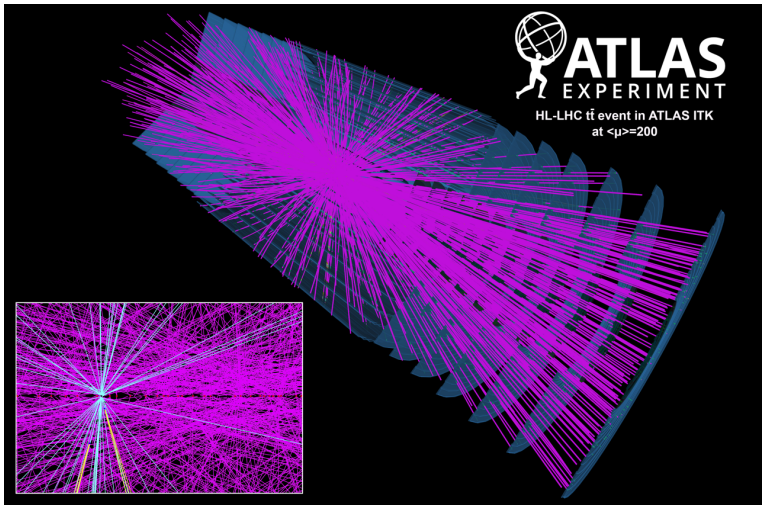
Many challenges for reconstruction:

- High multiplicity events and highly boosted jets require improved granularity and resolution
- VBS/VBF forward jets: forward tracker for pile-up rejection by jet-vertex association
- Rare events: improve in coverage and reconstruction efficiency

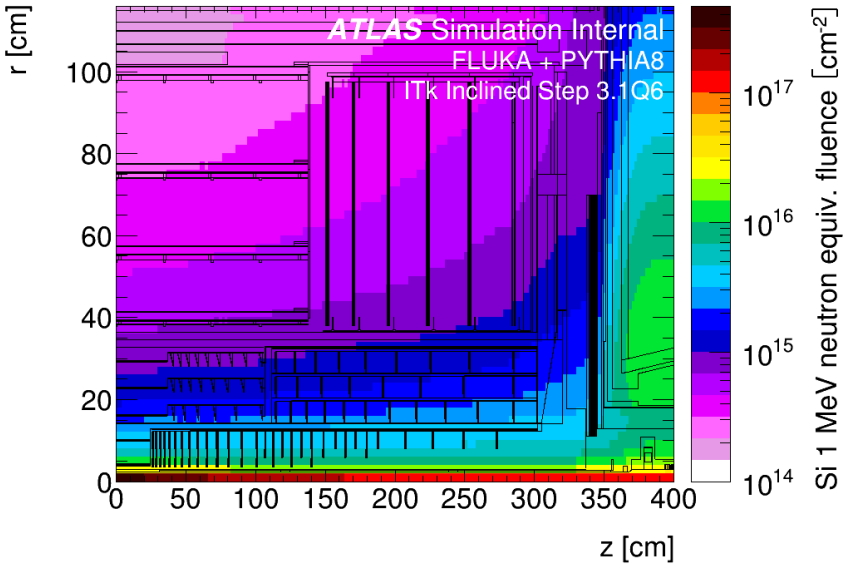
Tracking detector for the ATLAS experiment

Requirements for the tracking detector

- Luminosity of up to $7.5*10^{34}$ $cm^{-2}s^{-1}$
- On average 200 interactions per bunch crossing: keep occupancy at 1% level with highly granular detector
- High particle fluences
  - up to $1.3*10^{16}$ n_{eq}/cm^2 and 900 MRad for the pixel detector
  - up to $1.6*10^{15}$ n_{eq}/cm^2 and 70 MRad for the strip detector
- Low material budget
- Fast and reliable readout
- High charge collection efficiency
- High vertex and track position resolution



Simulated event with ttbar events and average pile-up of 200 collisions per bunch crossing



→ For Phase-II upgrade: new all-silicon tracker for the ATLAS experiment

Layout of the new Inner Tracker (ITk)

Silicon strip and pixel detector in 2 T magnetic field:

- 4 central strip layers and two endcaps with 6 disks each
  - n-in-p float zone sensors
  - ~18 k modules and ~234 k ASICs
  - ~ 60 million channels
  - Up to 640 Mbps per module
  - Total area about 165 m^2
- 5 pixel layers in the central and forward sections
  - 3D and planar sensors
  - ~8.5 k hybrid pixel modules and ~34 k front-end chips
  - ~5 billion pixels
  - Up to 4x 1.28 Gbps per front-end chip
  - Total area about 13 m^2
  - Inner two layers replaceable

Cooling with CO_2

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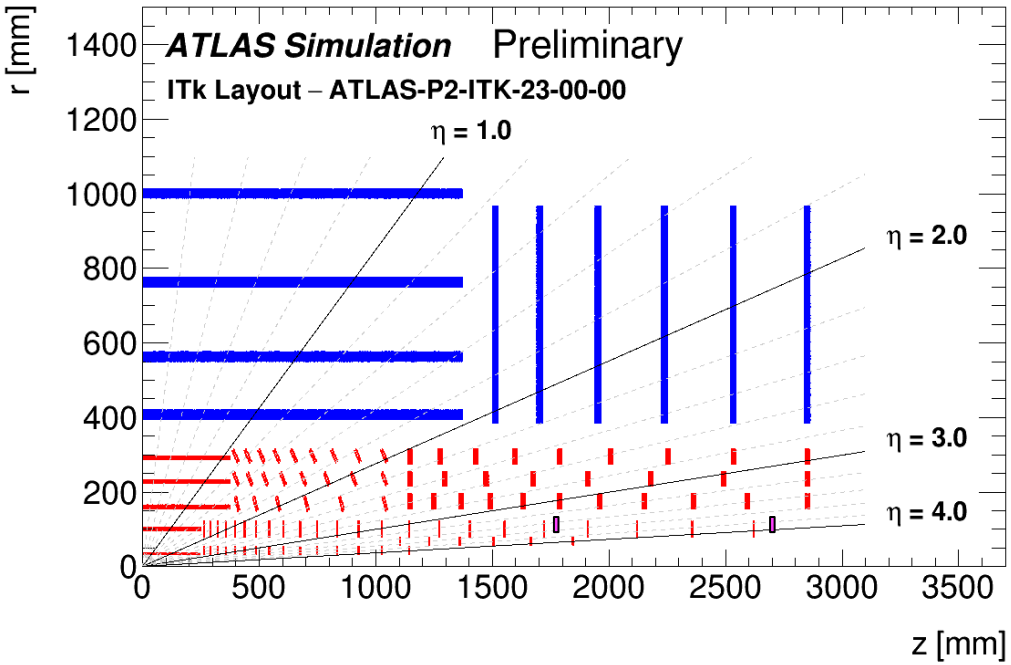
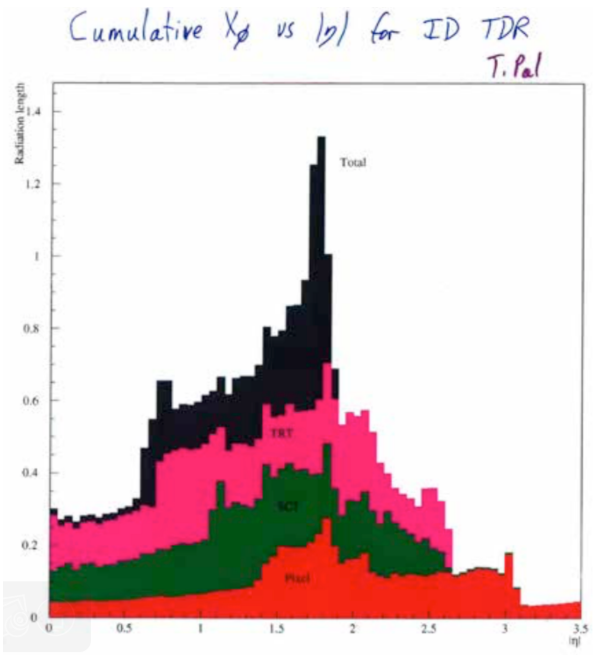


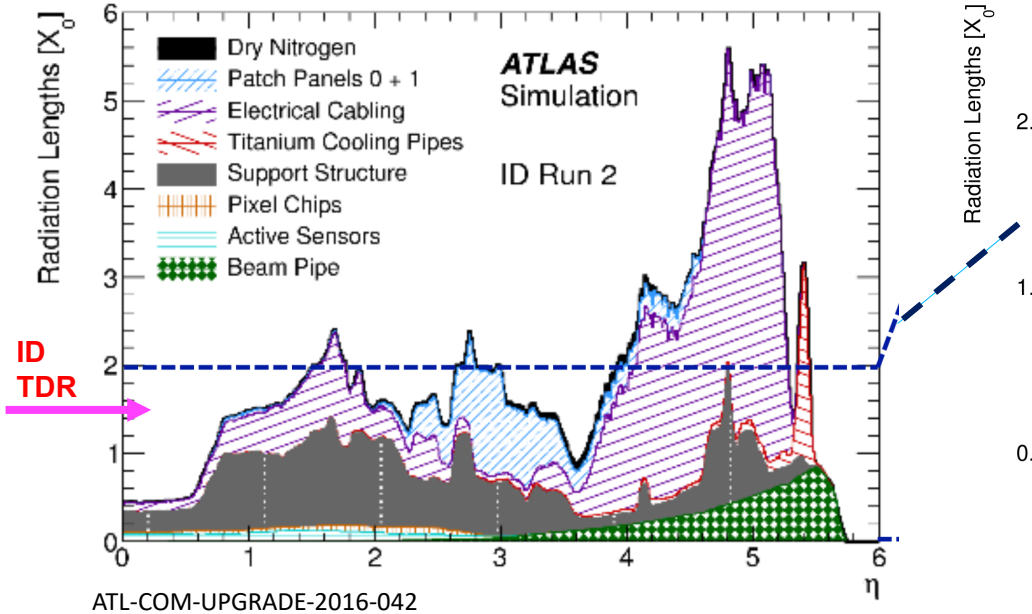
Technical Design Reports:
Strip detector CERN-LHCC-2017-005
Pixel detector CERN-LHCC-2017-021

Material estimate for ITk

Reduction of material by usage of

- CO_2 cooling with thin titanium pipes
- Thin silicon sensors
- Advanced powering: serial powering for pixels, DC-DC converters for strips
- Carbon structures for mechanical stability and mounting





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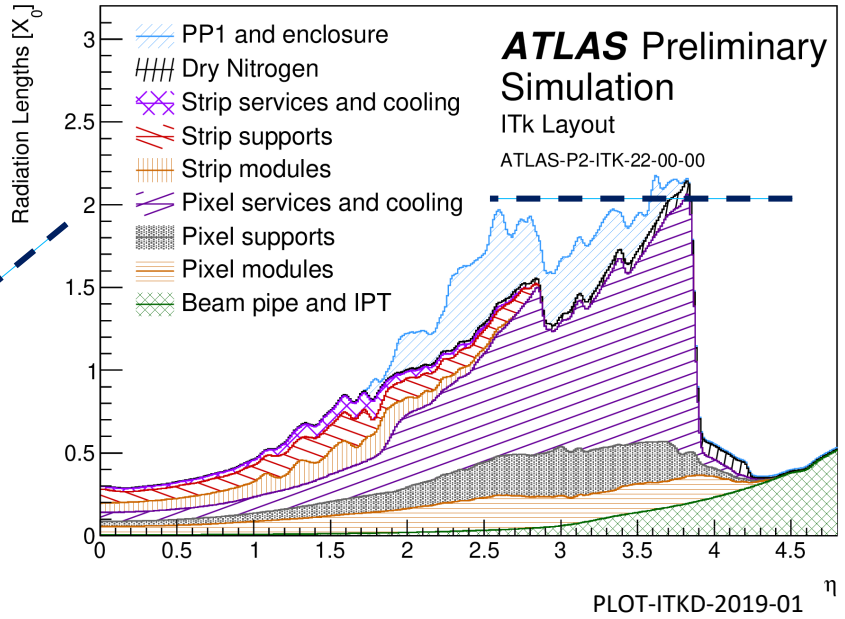

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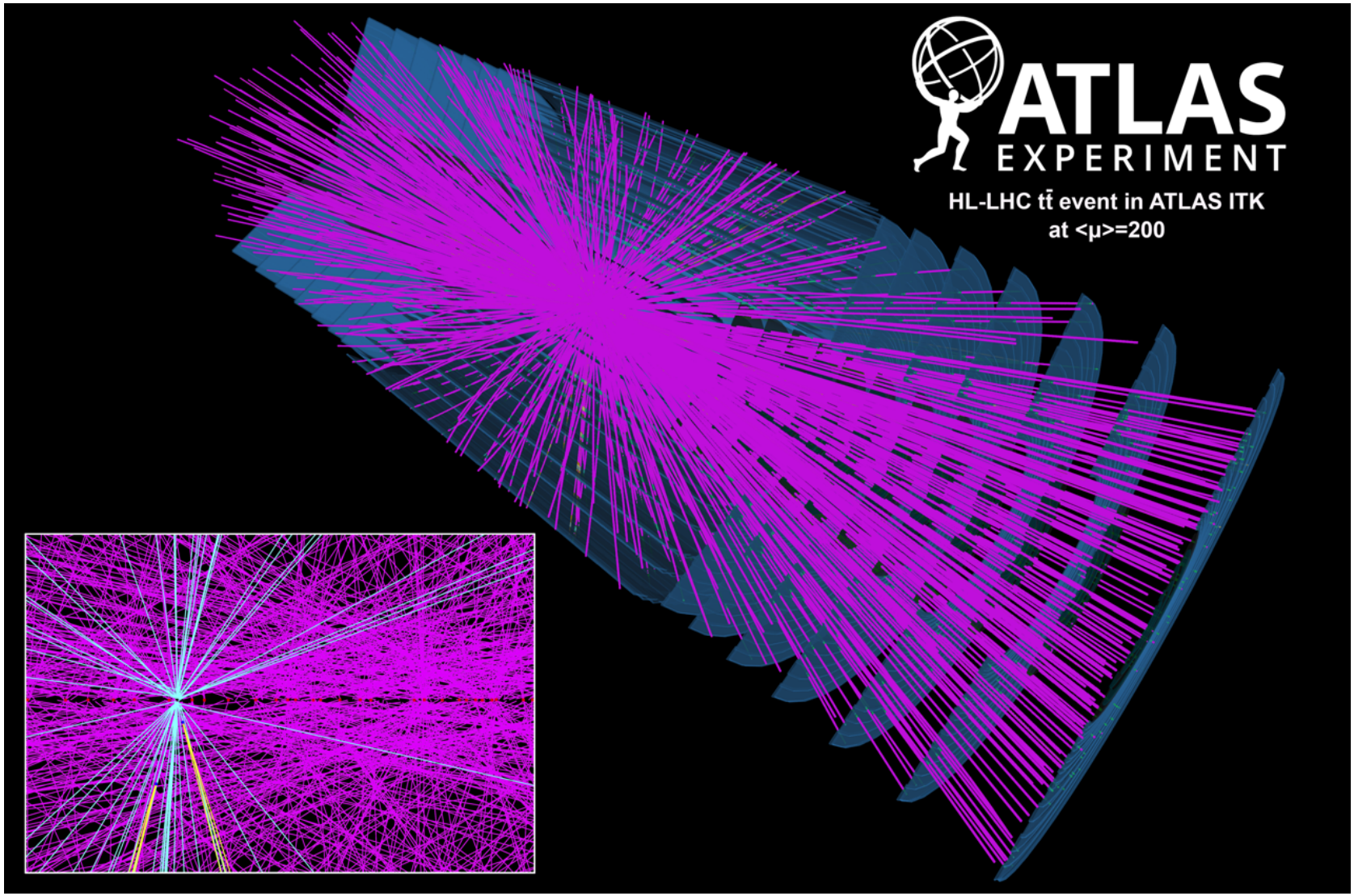
Towards the realisation of the system

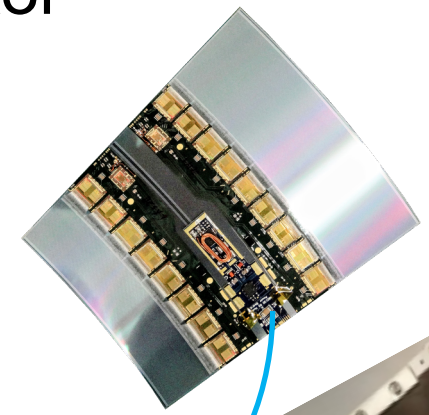


The concept of the ITk Strip Detector

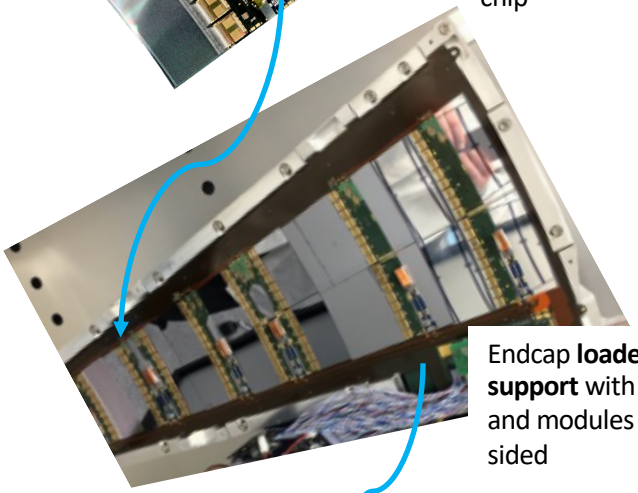
- 4 barrel cylinders and 2 endcaps with 6 disks each
- **Large strip system compared to current Inner Detector**
  - ~10x channels
  - ~3x size
  - ~5x modules

- **Concept of modularity of components** which are designed for manufacturability and mass production from the beginning (industry standard design rules, simplified construction,…)
  - Assembly and testing at multiple sites
  - Simplifies final assembly
  - Earlier test of full system

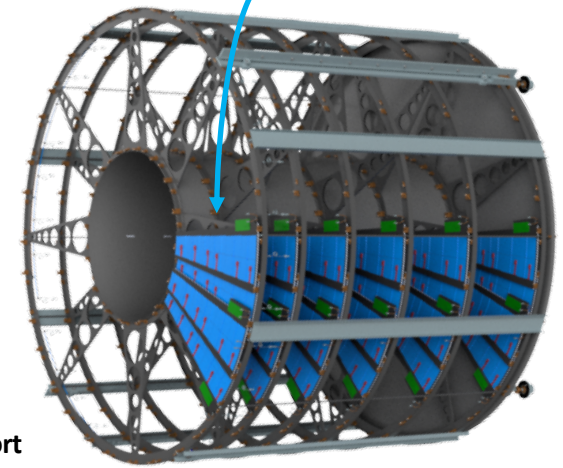
Not to scale



Module (endcap R0)
With FE chips, sensor and hybrid, power board with DC-DC converter and HCC chip



Endcap **loaded local support** with carbon core and modules glued double-sided



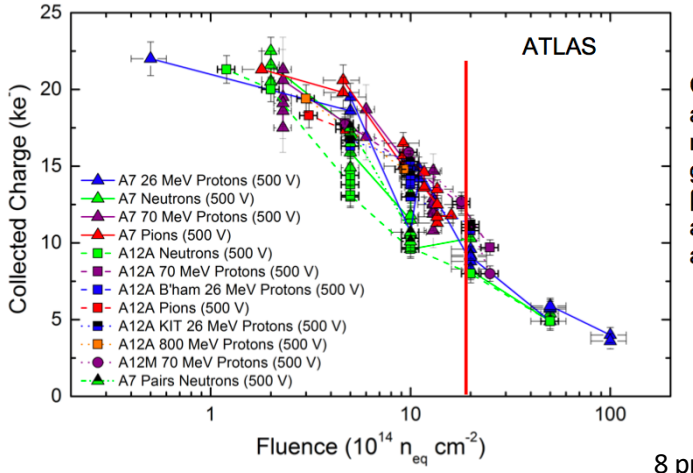
Endcap global support

One endcap will be assembled at DESY
Team heavily involved in described strip activities

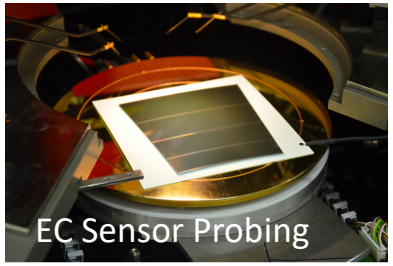
Strip sensors and readout electronics

- **n-in-p float-zone sensors with p-stop isolation and ~320 µm thickness**
- Strip length 8-50 mm depending on region
- **All sensors received from HPK for pre-production**
- QA and QC methods exercised at production sites, e.g. bow verified and for prototypes within specifications
- Few sites already qualified for production

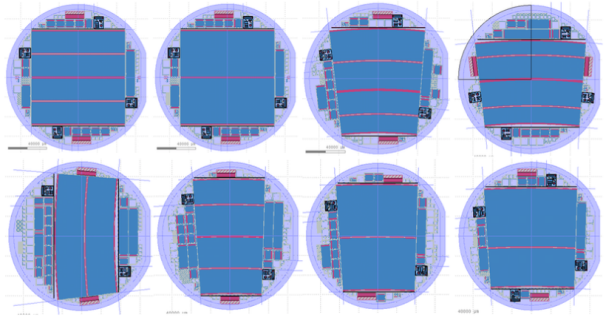
- **Binary readout chip (130 nm CMOS)** ABCStar with 256 channels, operated at 1.5 V
- Pre-production of ABCStar chips being tested with better single-event effects (SEE) tolerance
- Design of hybrid controller chip (HCC) technically challenging, optimization ongoing to resolve unexpected SEEs

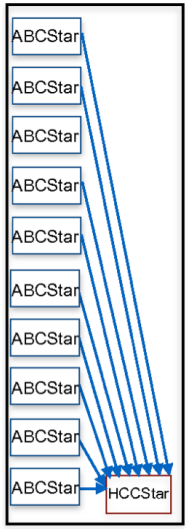


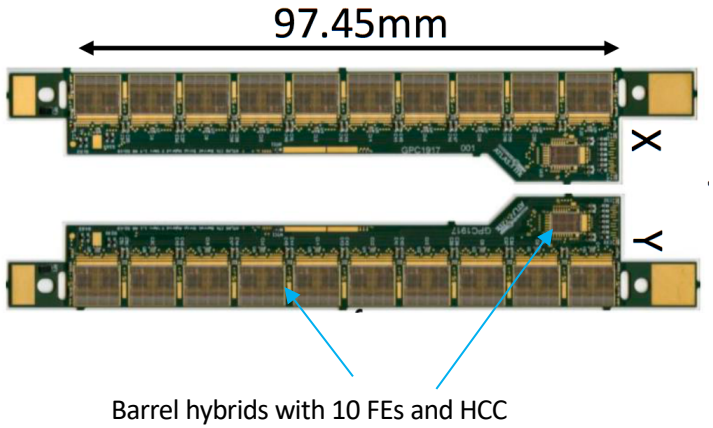
Collected charge after proton, neutron and gamma irradiation, β-source tests after 80 min annealing at 60°C



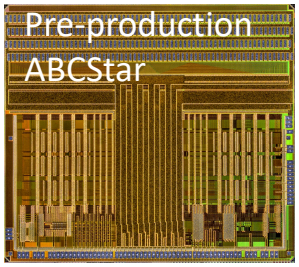
8 pre-production masks





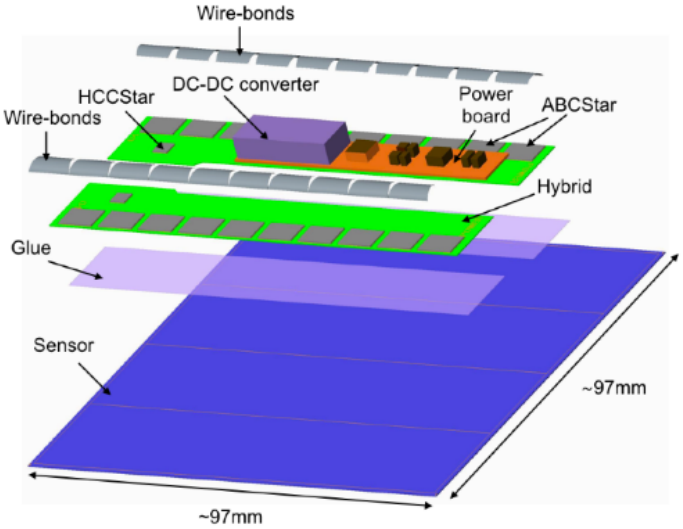


Barrel hybrids with 10 FEs and HCC

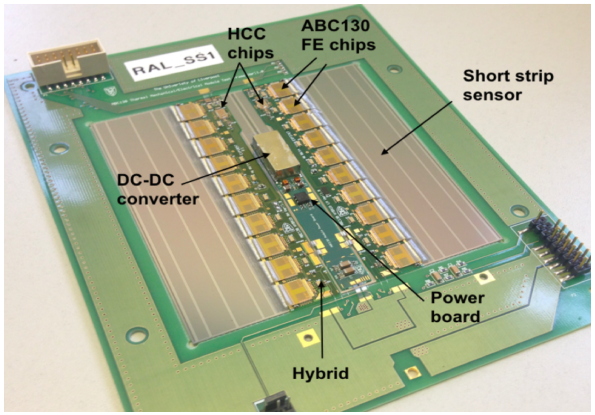


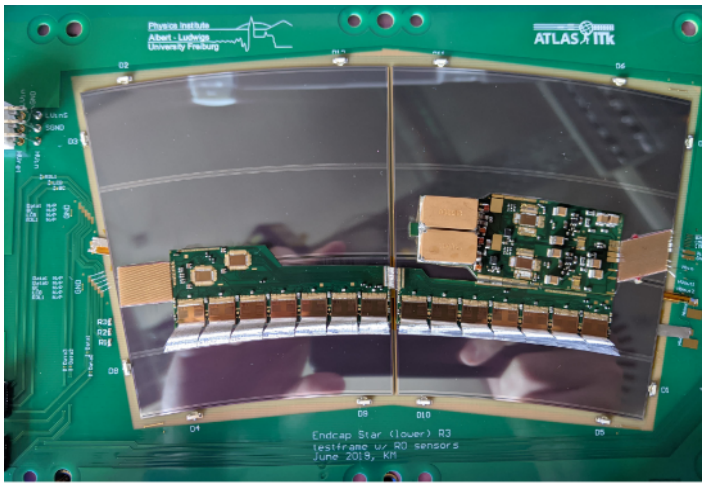
Strip modules

- **Several modules assembled and evaluated before and after irradiation to HL-LHC fluences**
- During module assembly, the hybrids and power boards are glued directly to the sensor
  - Tooling finalized for mass production
- Module production site qualification about to start
- Some EC modules show higher noise → test with a new hybrid design and test on local supports

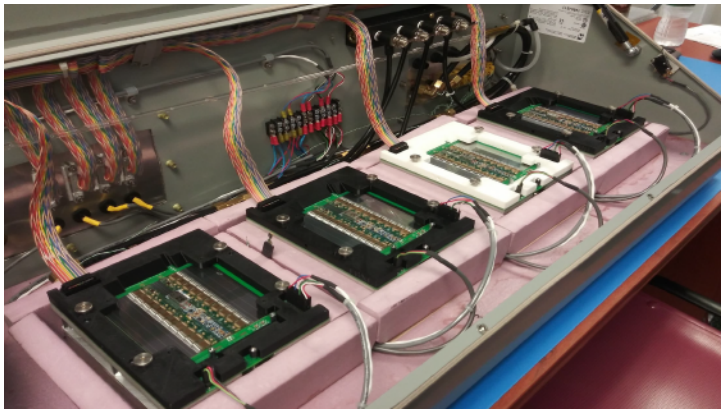


Barrel module





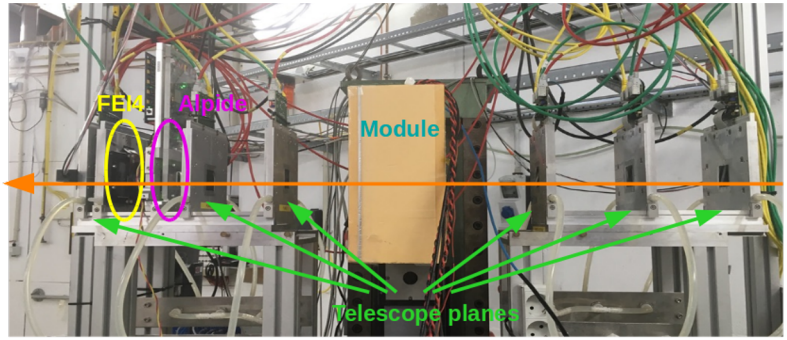
R3-EC module



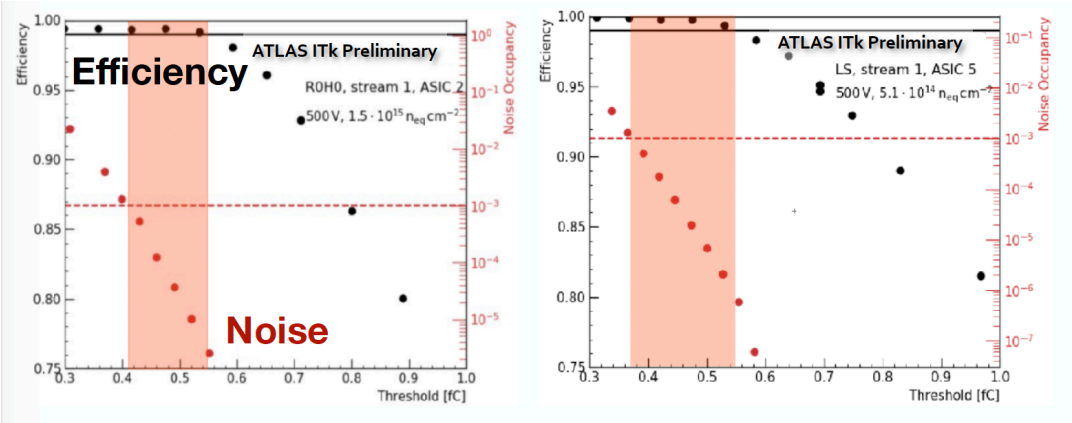
4 module thermal cycler

Module performance in beam test and irradiation

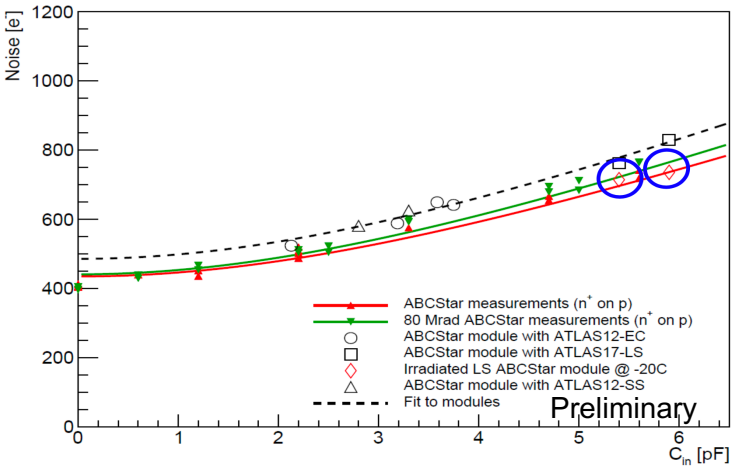
- **Several successful test beam campaigns at DESY-II test beam facility** of non-irradiated and irradiated star modules: Built with annealed sensors irradiated to max. expected fluence and X-ray irradiated hybrids



- Results show clear operating windows meeting >99% efficiency, <0.1% noise occupancy requirement



S. Wonsak, VERTEX 2019



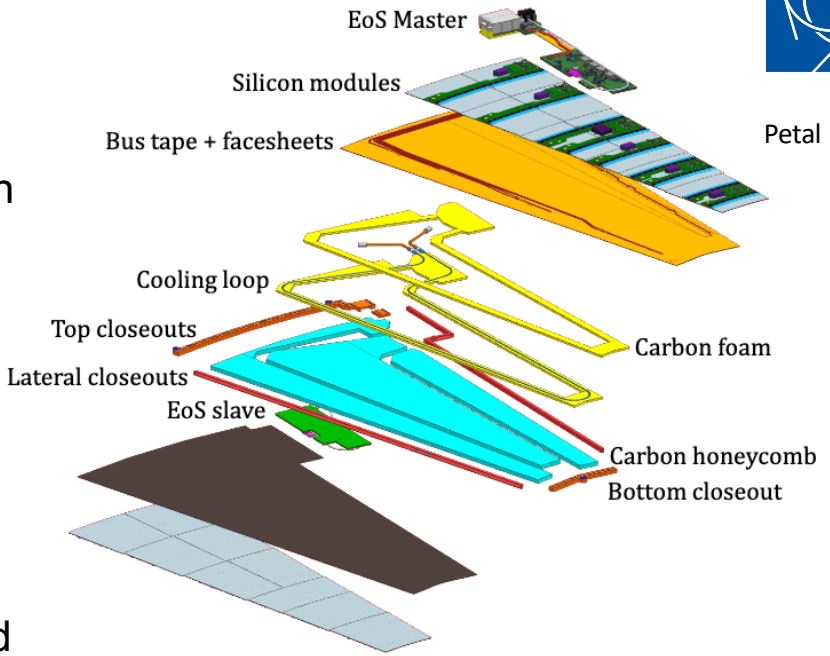
- Measured signal-to-noise ratio values above required value of 10 for all evaluated modules at foreseen bias voltages

Noise comparison of ABCStar chips at different conditions (e.g. single chip tests, module tests) well understood and in agreement with expectations

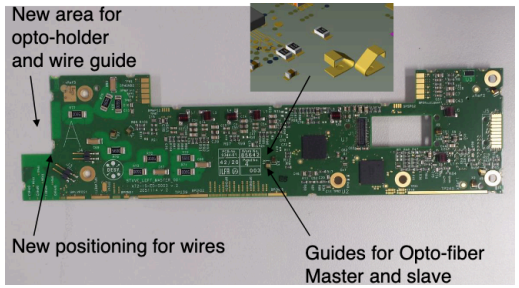
- Further testbeams with irradiated pre-production modules foreseen

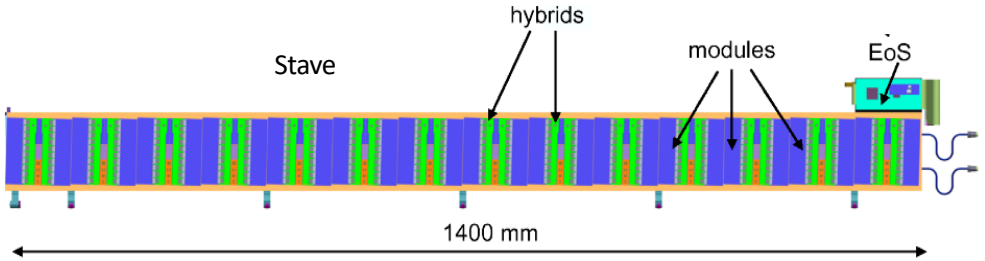
Strip local supports

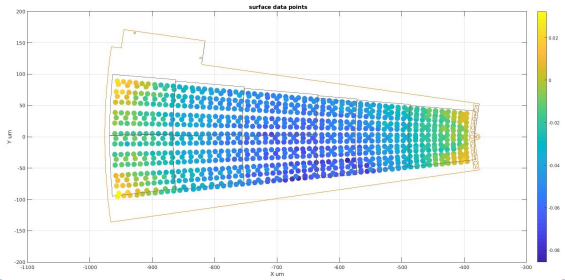
- **Carbon-fibre composite structures** with co-cured copper **bus tapes** have **modules** glued on top of both sides with a stereo angle between both sides
- In central region (barrel): staves with 14 modules on each side
  - 392 staves in total
- In endcaps: petals with 9 modules on each side
  - 384 petals in both endcaps
- **End-of structure cards service the electrical to optical transmission** (lpGBT and VTRx+ links) **and to the outside world:** production and tests with optimized design ongoing



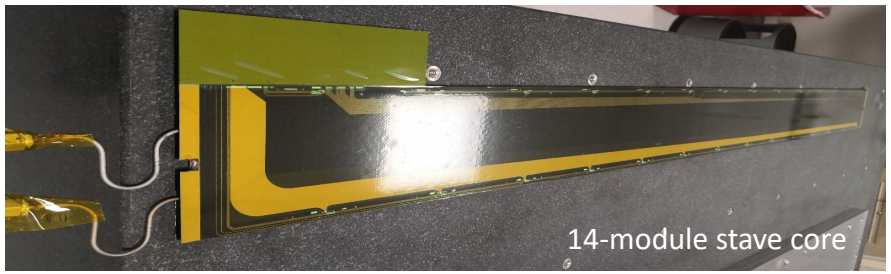
Design, verification and test @ DESY







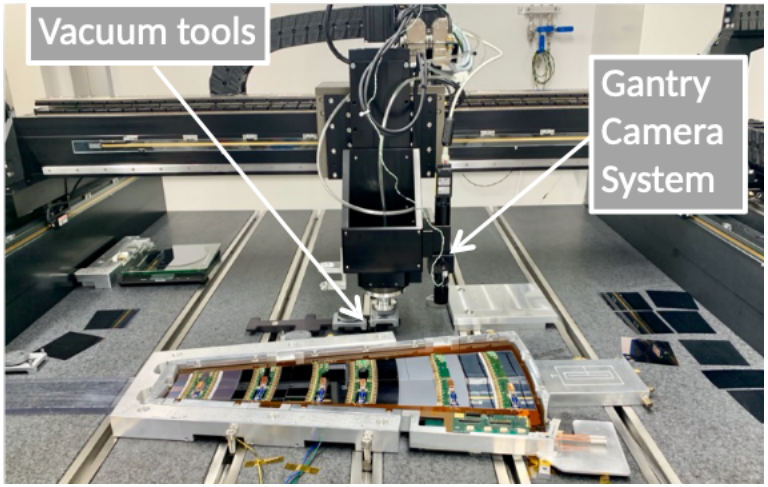
Petal with local flatness: 19 – 41 µm
Global flatness: 93=116 µm

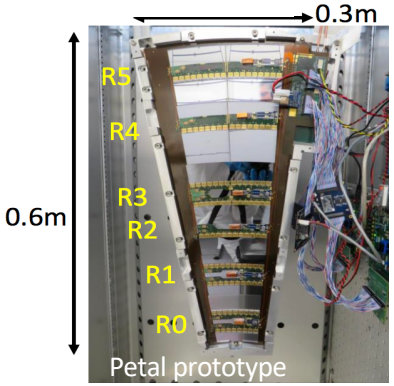


Good thermal performance measured

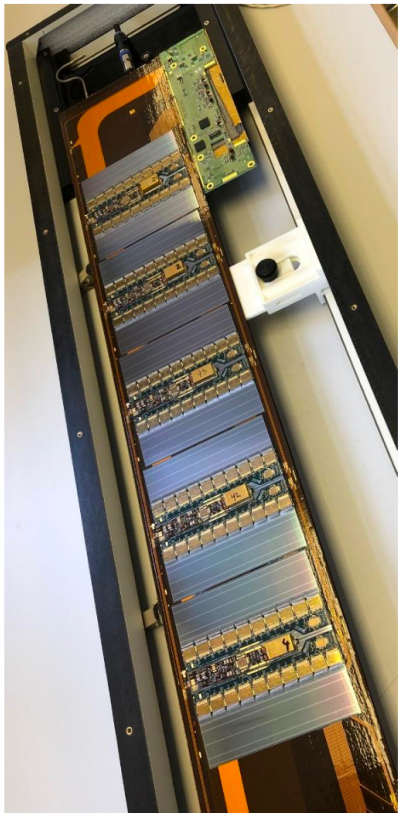
System test of loaded local supports

- Various prototypes have been fabricated and tested for both stave and petal variants
- Loading of modules with gantry systems
- Electrical test of short strip stave with 5 modules



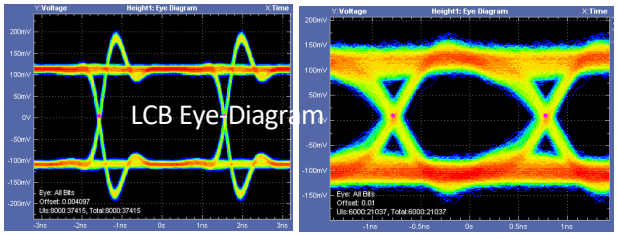


Electrical tests of petal indicate good performance, some excess noise seen caused by grounding issue

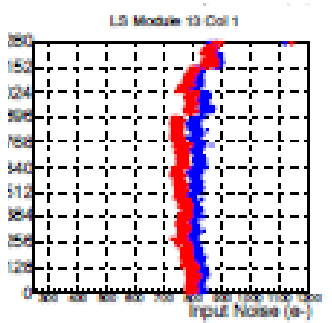


Barrel 5 Short Strip Module Stave

Noise as low as in single modules
320MBit 640MBit (800MHz probe)



Electrical tests after cool down to -30°C showed higher noise → solved by removal of AC-ground reference

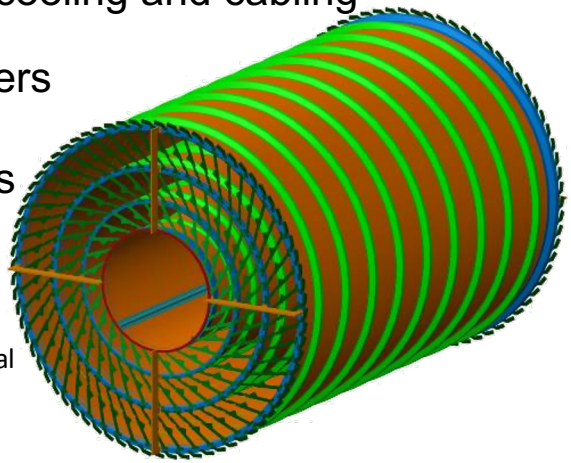


channel vs. input noise in electrons

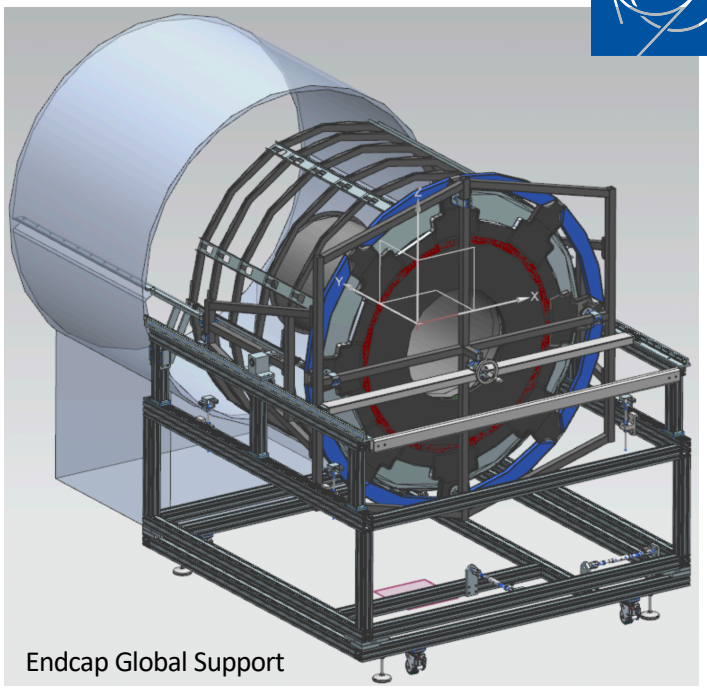
Demonstrated multi-drop command/clock between HCCs/lpGBT and modules on stave have excellent performance

Integration of the strip detector

- Loaded local support structures (staves and petals) are end-insertable including cooling and cabling
- For barrel: carbon cylinders for each layer in which staves are inserted. Tests with mock-ups ongoing



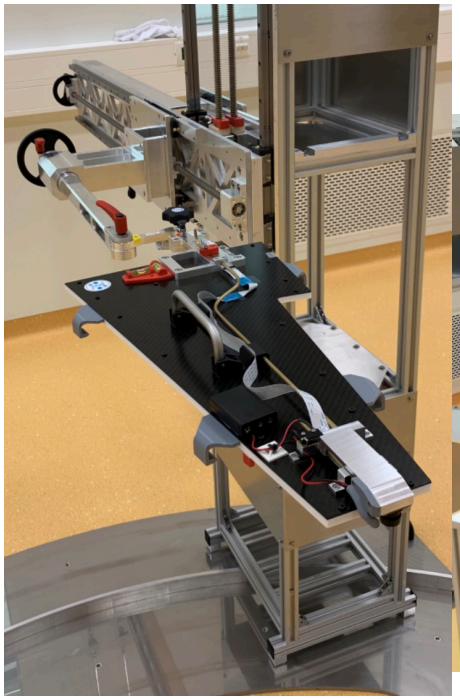
Barrel Global Support

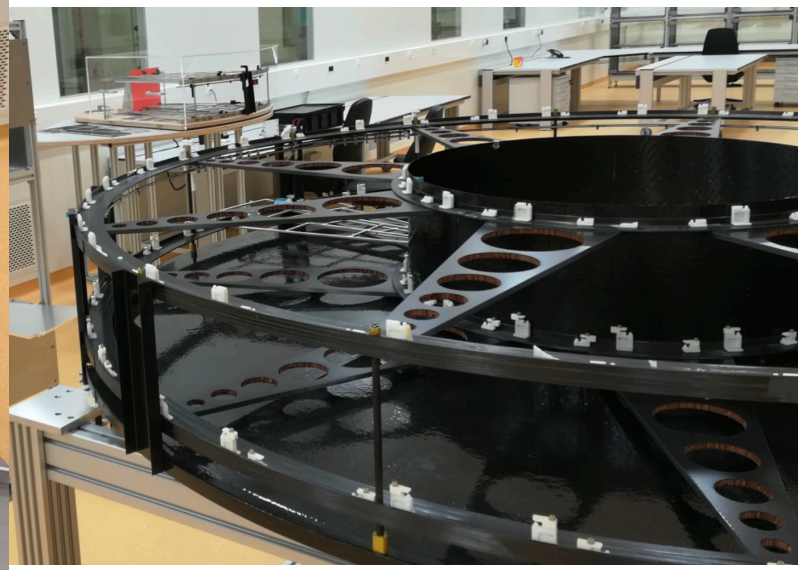


Endcap Global Support

- For endcaps: carbon wheels with blades for each disk mounted in endcap structure

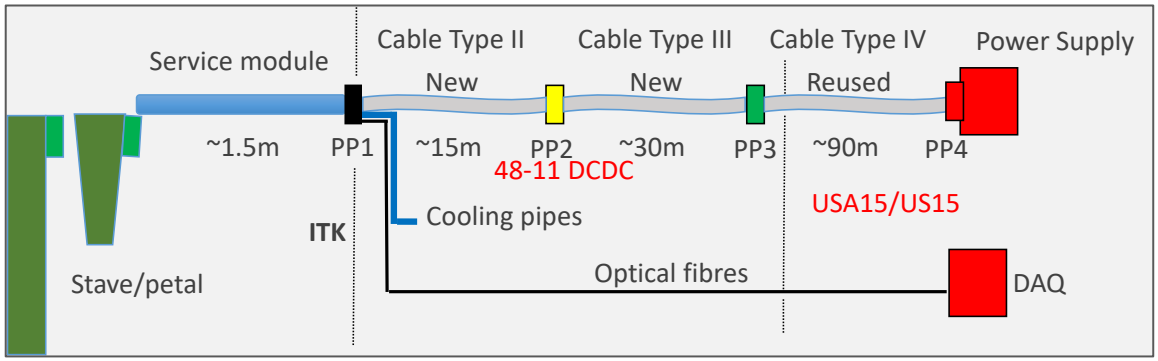
Tests with mock-ups progressing well





Services of the strip detector

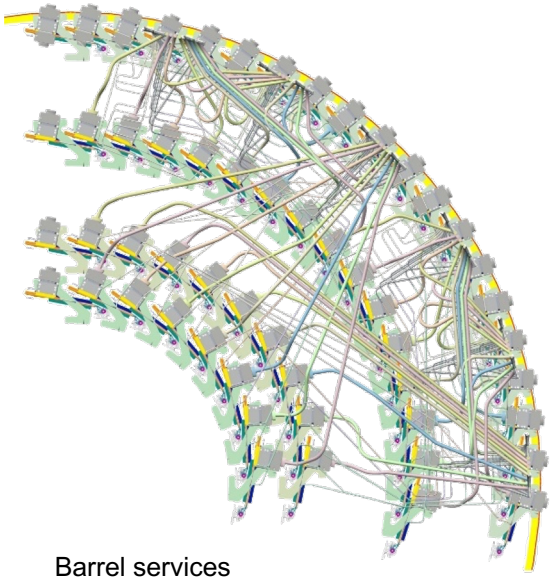
- Full chain defined and services purchased for larger system tests



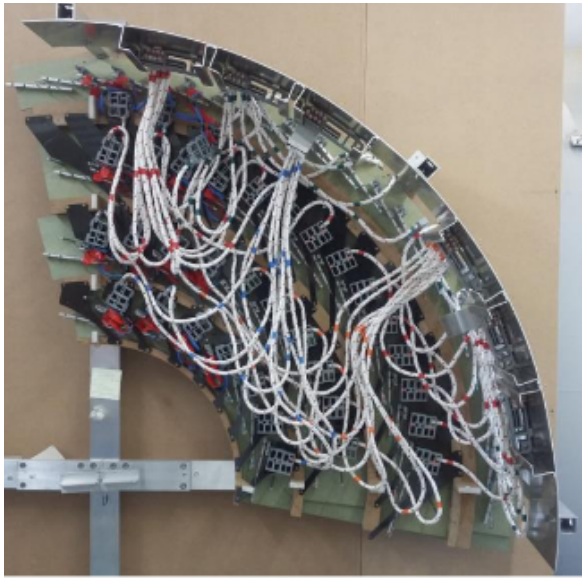
Type-1 Cable Connectors

Type-3 cables

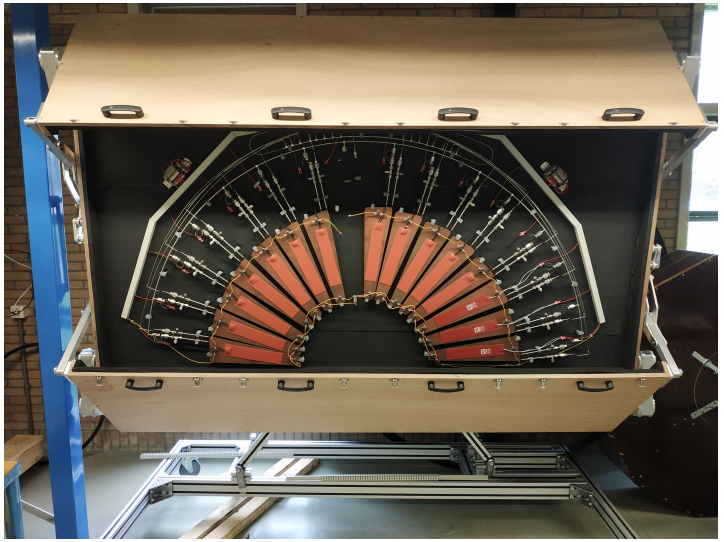
- Services on the detector sorted in service modules



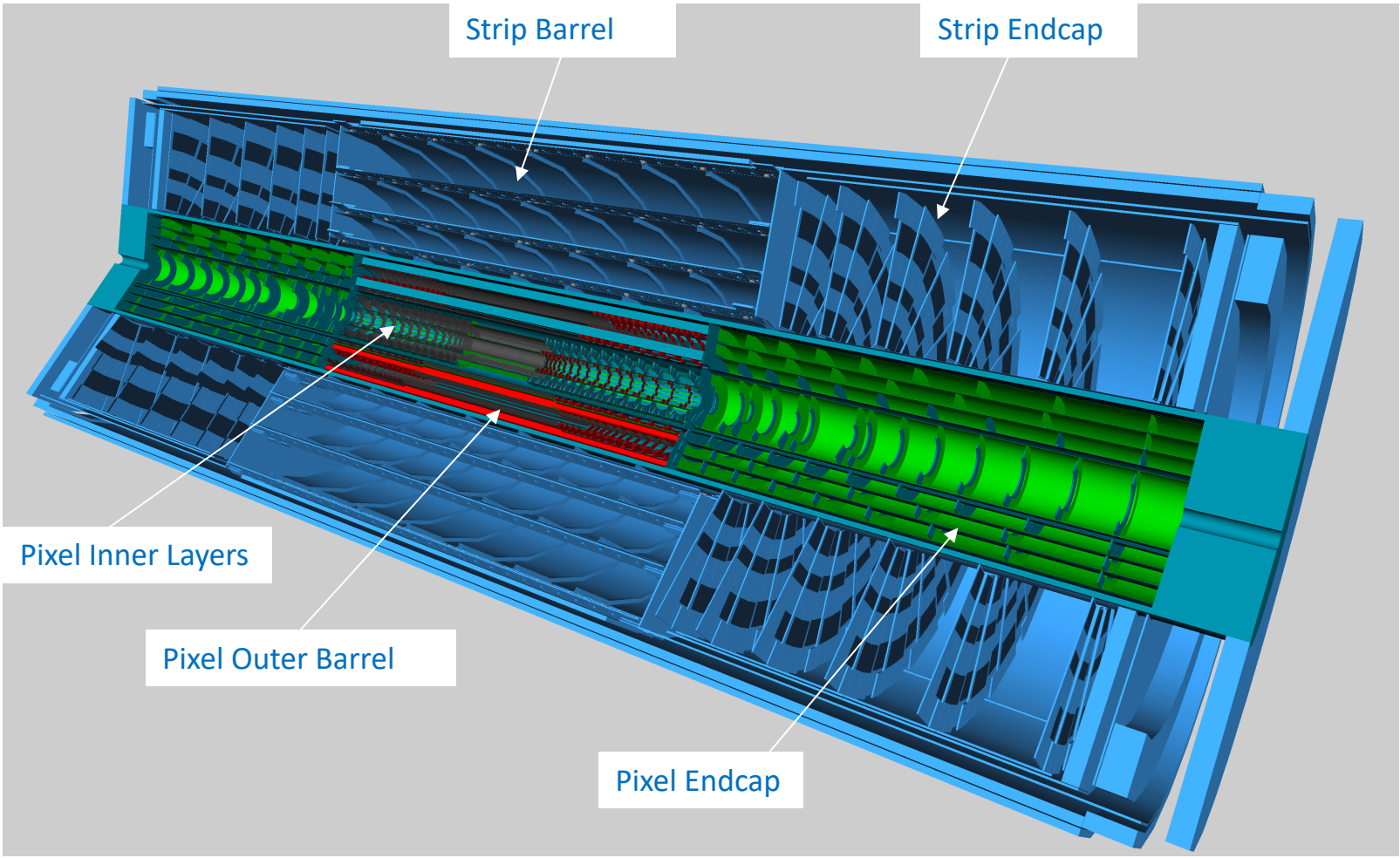
Barrel services



Mockup of services

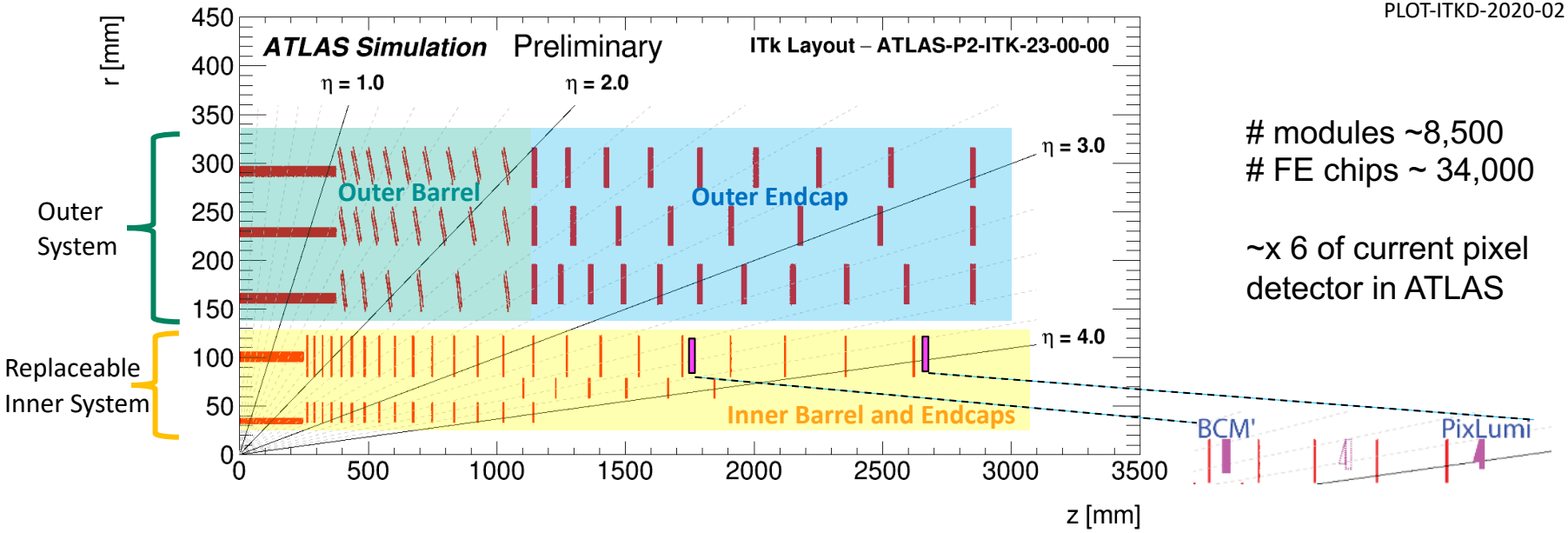


EC cooling manifold ready for testing in CO_2 plant at CERN


Strip Barrel
Strip Endcap
Pixel Inner Layers
Pixel Outer Barrel
Pixel Endcap

The layout of the ITk Pixel detector

PLOT-ITKD-2020-02



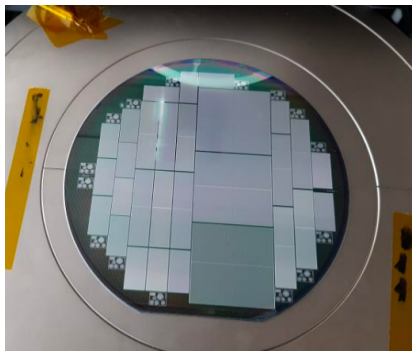
- Different sensors types and technologies depending on distance from interaction point
  - 3D-sensors in triplet assemblies (Layer 0), planar with 100 µm (L1), planar sensors with 150 µm thickness (L2, L3, L4)
  - Pixel size 50x50 μm^2 (L1-L4, rings of L0), 25x100 μm^2 (flat part of L0)

- Luminosity monitoring and beam abort modules recently added
- Fast readout with max. 1 MHz trigger rate
- Fast data transmission with up to six links of 1.28 Gbps (electrical) per lpGBT and VTRx+ link (optical) to FELIX readout
- Reduction of material by deploying serial powering and CO_2 cooling

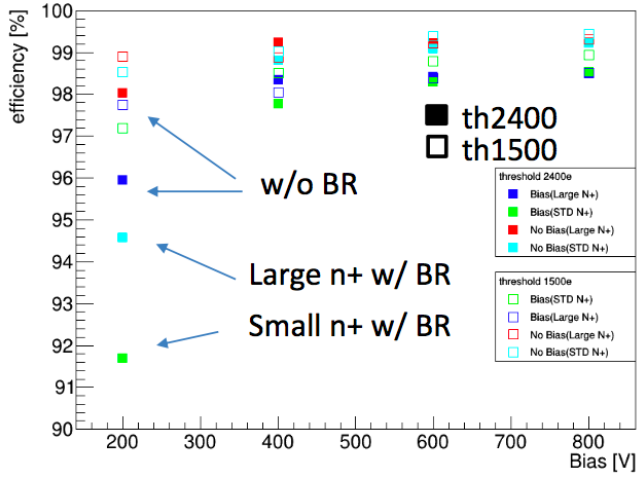
Planar pixel sensors and 3D pixel sensors

Thin n-in-p planar sensors

- Dies of 4x4 cm^2
- 100/150 µm thick
- Bias voltage up to 600 V (at end of life-time)
- Signal: ~10000 e^- (~6000 e^- after HL-LHC dose)
- Market survey completed



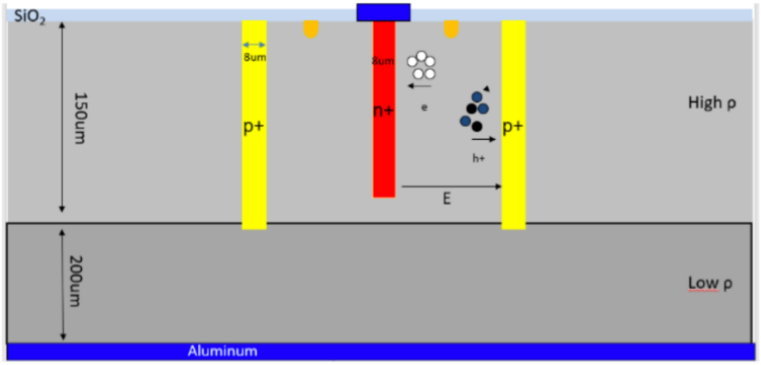
Test beam result for 50x50 μm^2 planar module irradiated with 70 MeV protons to $3*10^{15}$ n_{eq}/cm^2

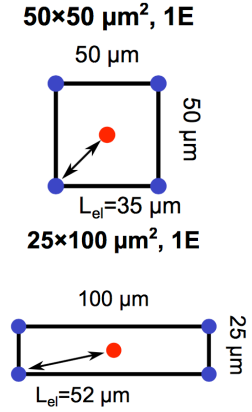


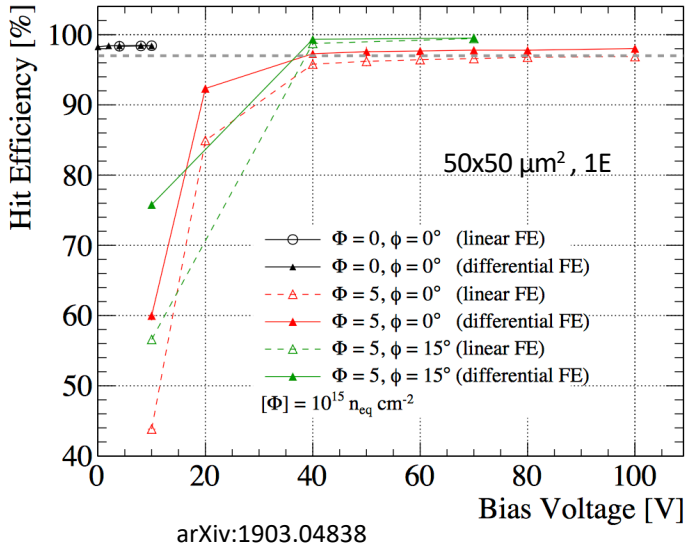
K. Nakamura, Pixel 2018

3D sensors

- For innermost layer: 1.3×10^{16} n_{eq}/cm^2 for 2000 fb^{-1}
- Dies of 2x2 cm^2, 150 µm thickness + 100-200 µm support wafer
- Pixel size of 25x100 μm^2 challenging for radiation hardness and only in part of L0 foreseen







arXiv:1903.04838

- >97% efficiency at perpendicular track incidence
- Power consumption at the operational voltage: <10 mW/cm^2
- Maximum operational voltage: 250 V

New pixel front-end chip: RD53 – ITkPixV1/2

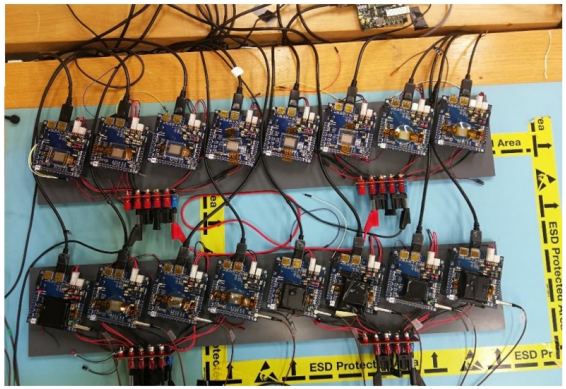
RD53 Collaboration: joint R&D of ATLAS and CMS
ASIC: 65 nm with TSMC

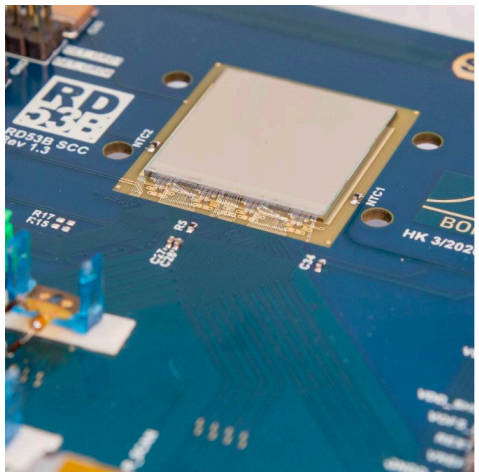
www.rd53.cern.ch
CERN-RD53-PUB-17-001

- 4 data lines at 1.28 Gbps
- Low threshold ~600 e^-
- Integrated shuntLDO
- Design power 0.7 W/cm^2, up to 8 A supply current for four-chip module
- Radiation hardness up to 500 MRads
- 154k pixels per chip, expecting up to 250 hits/chip/bunch crossing, 500 bc buffer

RD53A FE prototype (full width/half depth chip with 3 analogue FE) heavily investigated: **Many results collected, show comparable performance within specifications**

- Wafer probing set up
- Two readout systems for testing available
- Radiation damage depends on dose rate
- Proof-of-principle of operation in serial powering chain shown



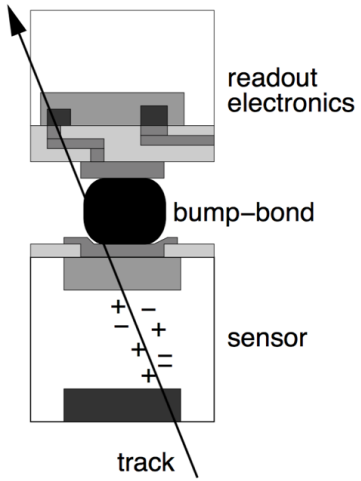


ATLAS ITkPixV1 FE prototype

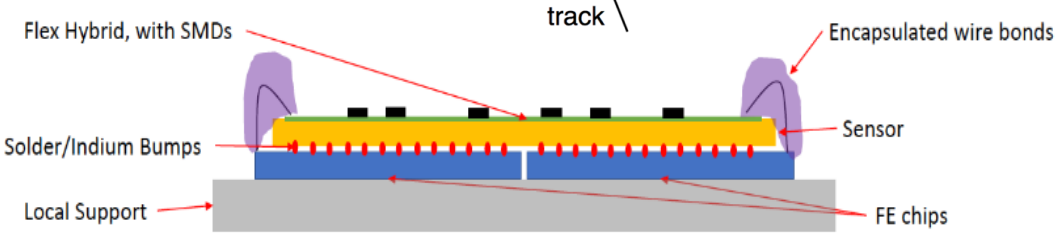
- Differential FE of RD53A FE plus few design changes e.g. under current and over voltage protection
- ATLAS chip submitted March 2020 and received June 2020
- All the tested functionalities are working as expected
- High digital current because of an issue in the ToT latches
- Refined version in preparation

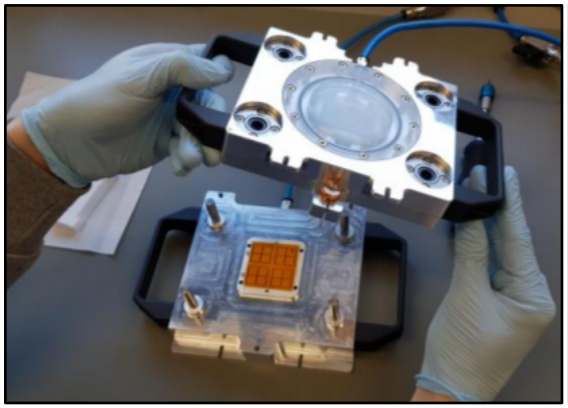
Module concept for the pixel detector

- **Sensor and front-end electronics** connected to bare module with **high density bump bonding** (market survey to qualify several vendors about to fininsh)
- **Modules assembly** of single chip, two chips (duals) and four chips (quads) to one sensor and flex circuit boards
- **Irradiation study of glues and encapsulation materials**

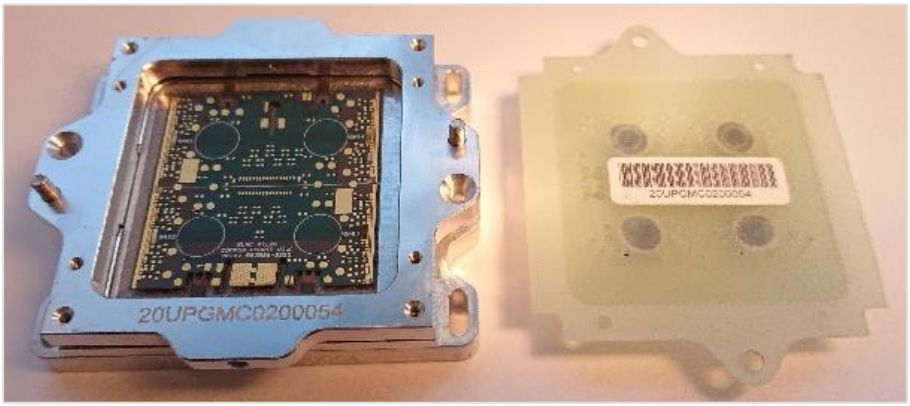


N. Wermes, arXiv:0811.4577

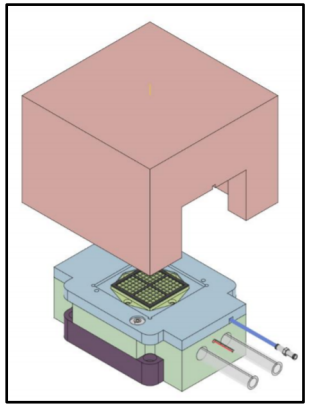




Assembly tooling



Prototype module in carrier for testing and transport



Jig for electrical tests

→ Production of four-chip modules ongoing with RD53A chips with common tooling
→ Systematic evaluation of performance and production flow

Challenges for pixel modules

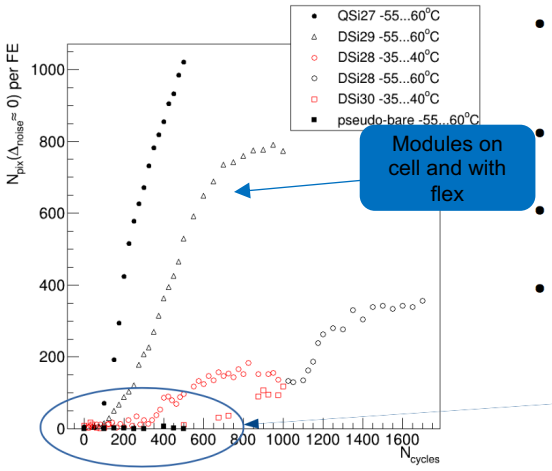
Disconnected bumps after thermal cycling of modules mainly caused by stress from copper in hybrid

- Linear and bump geometries studied in FEA models to analyze thermal stress
- Models predict number of cycles to failure like observed failures in FE-I4 modules

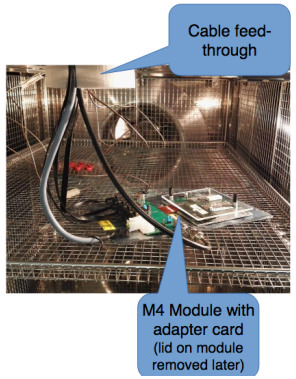
- **Models predict: Survival of 120 thermal cycles for -55°C to 60°C and 4000 for -45°C to 40°C before failure compare to specification of 400 cycles**

- Parylene coating of the module has a beneficial effect
- More studies ongoing

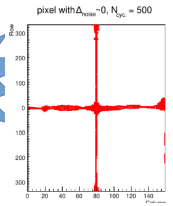
Thermal cycling of quads (-55 °C – 60 °C):
IV ok after 2200 cycles but source tests show disconnected bumps after O(20) cycles (J. Grosse-Knetter)

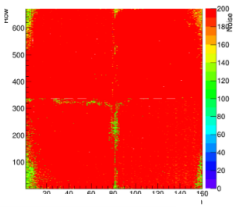


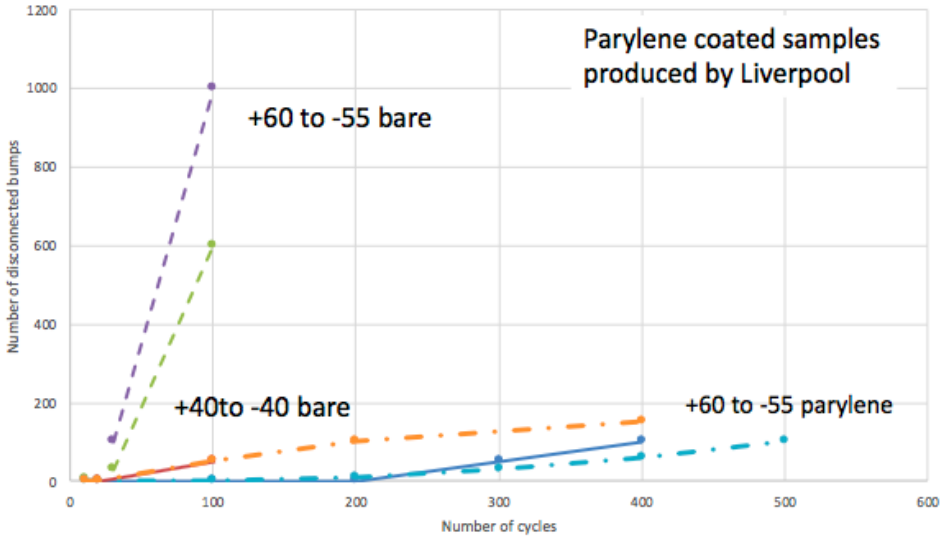
- Black/red: full/smaller temperature range
- Solid circles: QC (x1/4)
- Solid squ.: bare (x1/2)
- Open sym.: DC-mod.



Pseudo bare module added





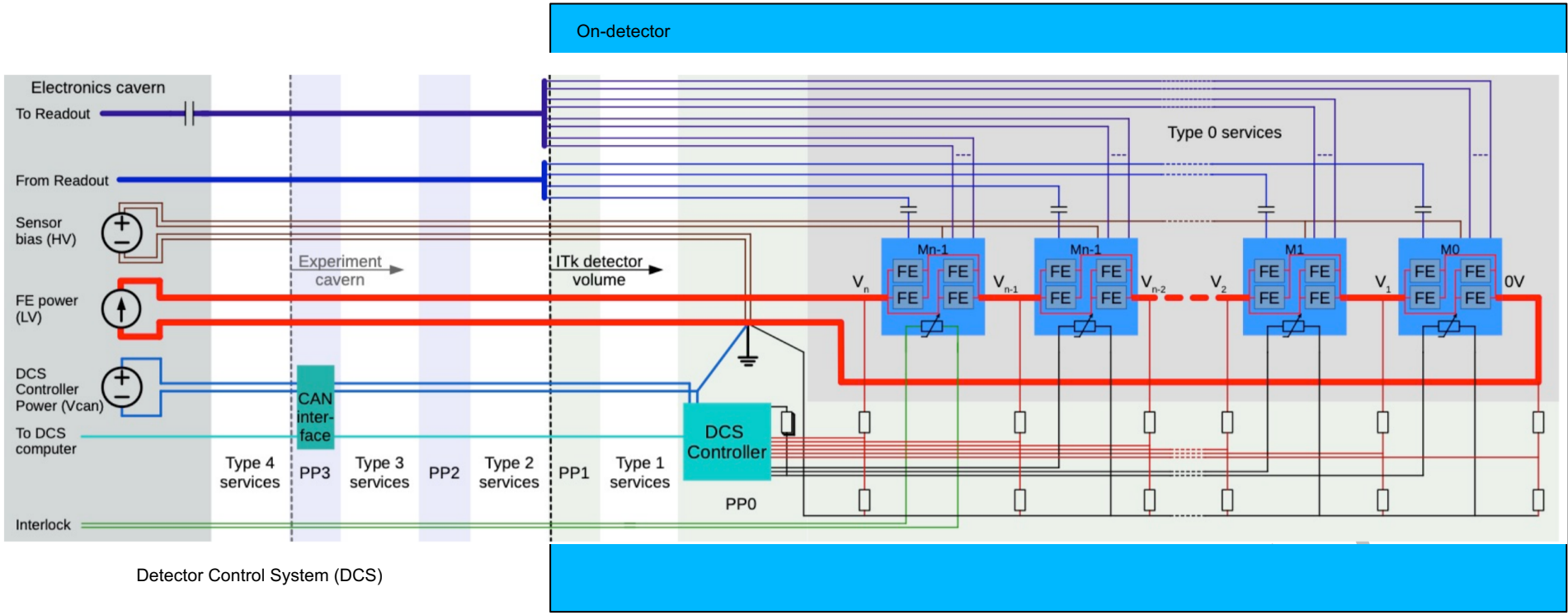


Thermal cycles on single chip FE-I4 module with 48 µm Cu on hybrid, with and without parylene coating (R. Plackett, L. Cunningham)

Powering of the pixel detector: serial powering

- **Powering modules serially with chains of up to 16 quad modules**
  → Reduced number of supply lines, less material
  → Less power dissipation on services than with parallel powering
  → Radiation hard on-chip shuntLDO allows regulation of voltage on chip
- Several HV lines per chain (at least 2 per SP-chain foreseen)
- Each module on different potential → AC coupling of data lines

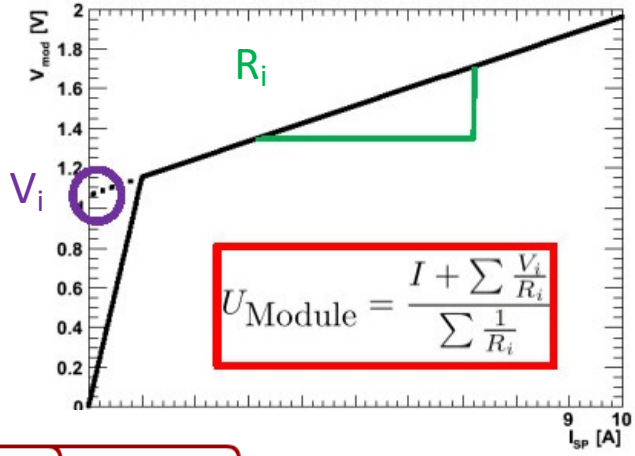
Serial powering:
T. Stockmanns et al., NIM A511 (2003) 174-179
D. Bao Ta et al., NIM A557 (2006) 445-459
L. Gonella et al., JINST 5 (2010) C12002

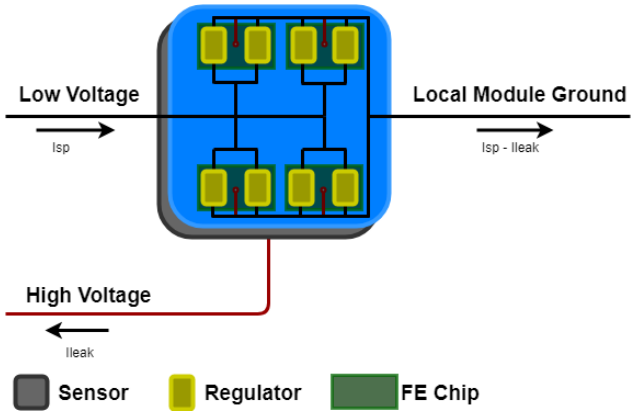


The voltage drop on every module and the temperature on every module is monitored through an independent readout path with a monitoring chip

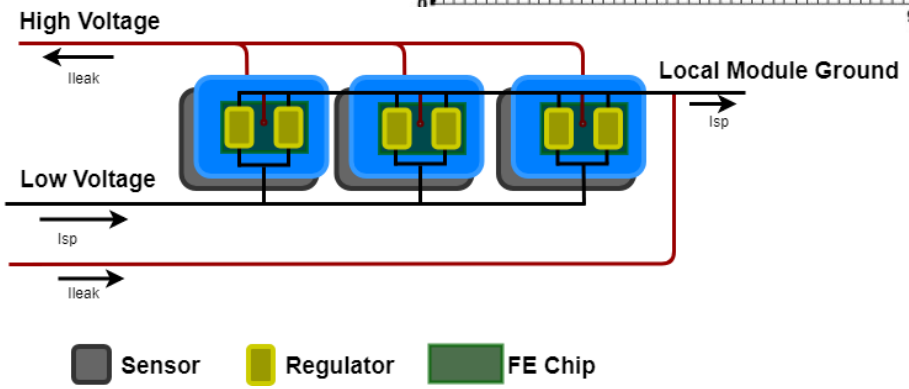
Powering of the pixel detector: serial powering

- **Constant current supplied and parallel distributed on one module to all front-ends**
  - 6-8 regulators in parallel operated: **slope** and **offset** of regulator determines module's IV-curve
  - Input current to shuntLDO regulators can exceed the nominal load current by a factor of ~2 (shunt capability) → Powering chain preserved even if one or two FE chips on a four-chip module fail open → But impact on thermal performance of the module





With planar sensors and 4 FEs



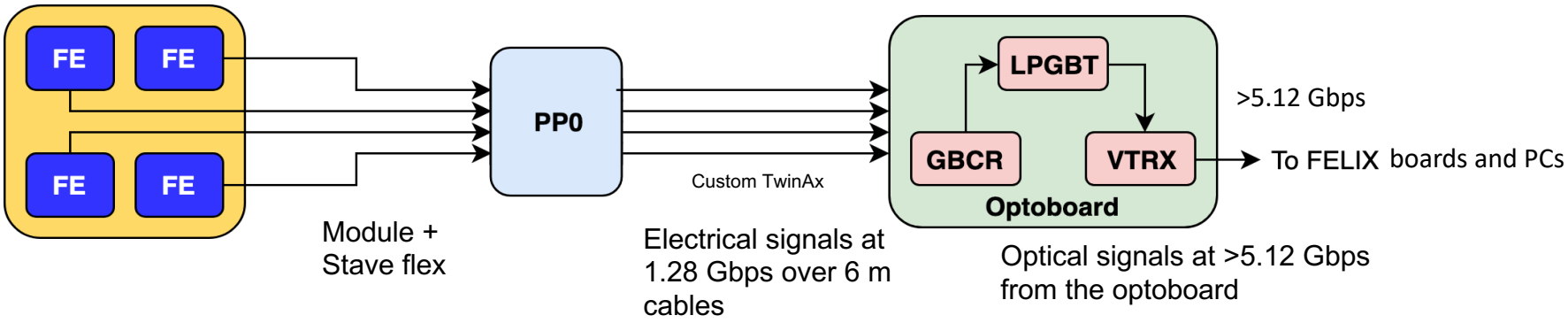
Modules with three 3D sensors

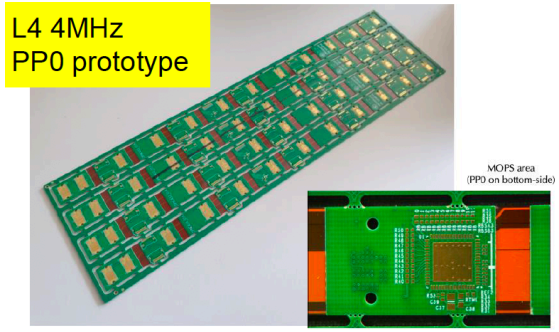
- **About 1000 SP-chains, will validate the SP-chain concept up to a length of 16 modules**
- Challenging to optimize the choice of shuntLDO configuration in order to minimize total power dissipation while meeting all constraints (like same shuntLDO configuration for all quad modules)
- **Total power consumption (112 kW) within cooling budget**
- Regulators/periphery is warmest area inside FE, about 40-45% of power in periphery (10% of FE area) → Taken into account in detector design

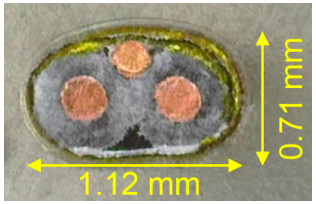
Readout of the pixel detector: data transmission

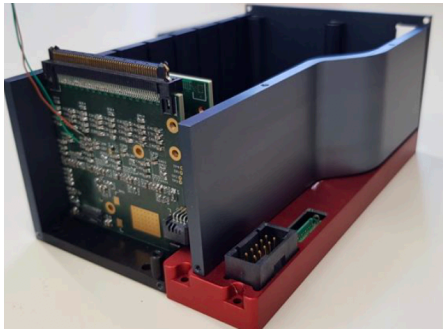
- On-detector: kapton/copper flexes → Patch panel 0 → Twin-axial cables → Giga bit transmitter recovery chip (GBCR) → lpGBT and VTRx+ for aggregation → Optical fibres to readout PCs with FELIX readout boards

- Uplink sharing for all layers to reduce material (320 Mbps inter chip data transmission on the modules)





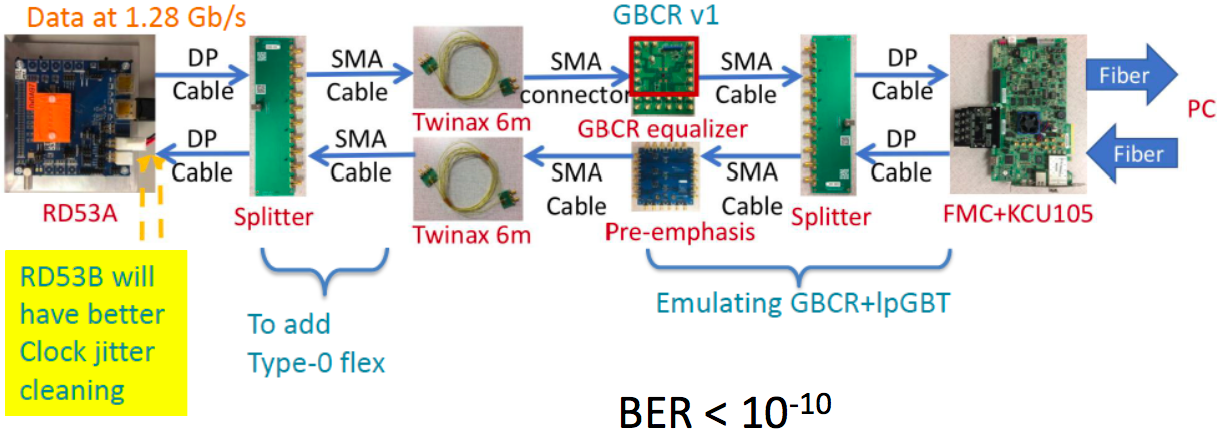




- Losses to be kept below 20 dB for FE-chip and GBCR including connectors, flexes and cable
- Studies for verification and prototyping heavily ongoing

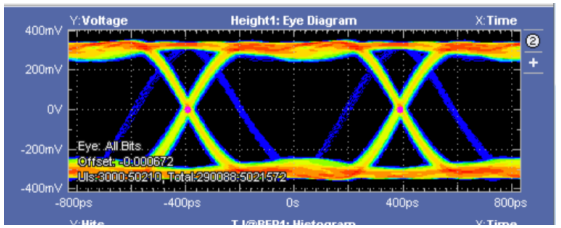
Verification of data transmission

- Developing system test with all elements
- Tested transmission chain with 1.28 Gpbs data rates using GBCRv1, which was optimized for 5.12 Gbps



$BER < 10^{-10}$

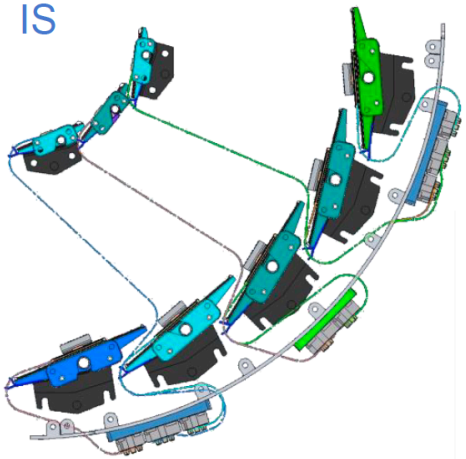
Uni Berne and SLAC



Eye diagram over full chain:

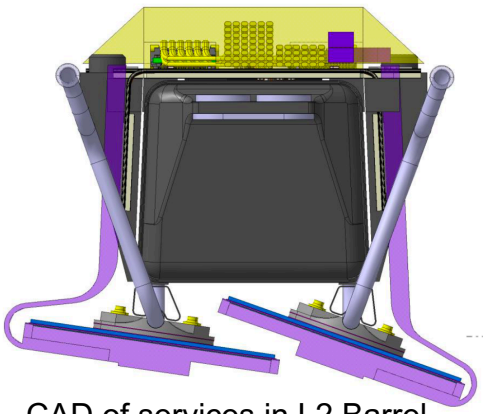
- RD53 CDR + Flex + TwinAx + GBCR with pre-emphasis
- Jitter: ~50 ps, Eye opening: 250 mV

- Further challenge: routing of services since there are many and space is limited between layers



CAD of services in L0

Type-1 Envelope



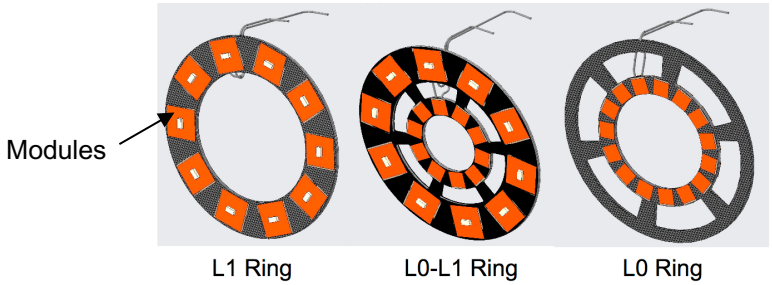
CAD of services in L2 Barrel

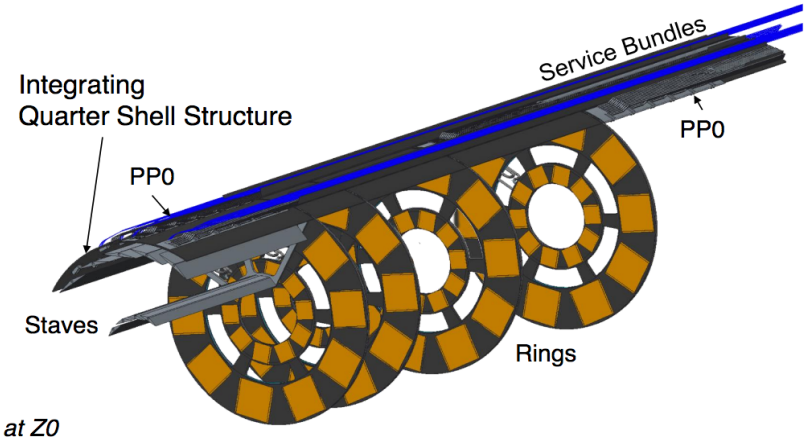
Pixel local support components I

Principle: Structures from carbon foam with carbon fibre co-cured and modules attached

Not to scale

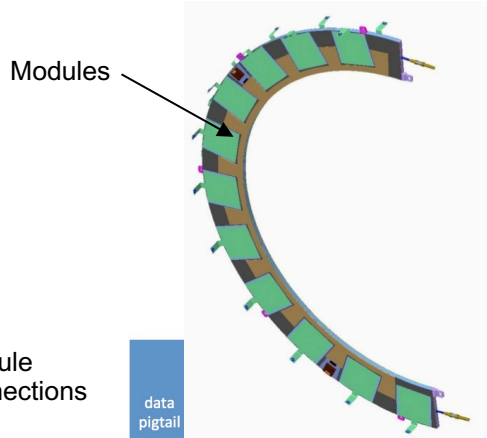
- **Inner system**



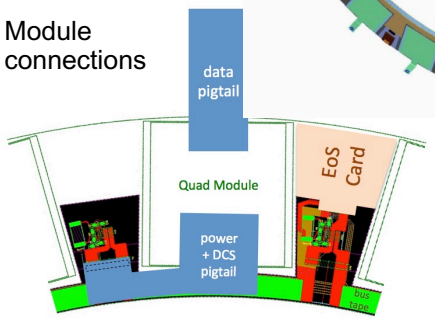


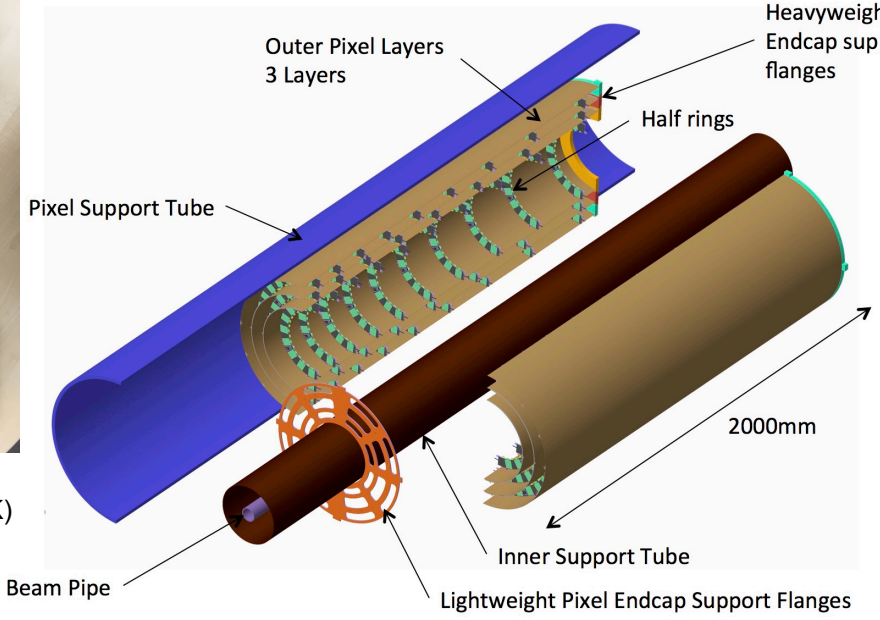
Cut at Z0

- **Endcaps**



Half-ring with embedded cooling pipe (produced in UK)

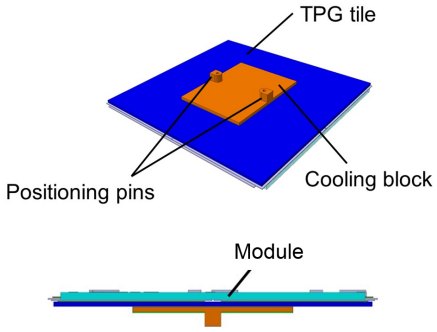




Pixel local support components II

Principle: Structures from carbon-fibre composites with modules attached

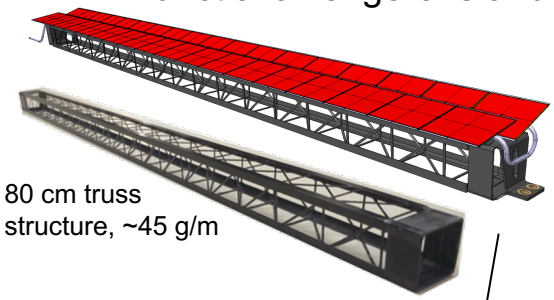
- **Outer barrel layers**

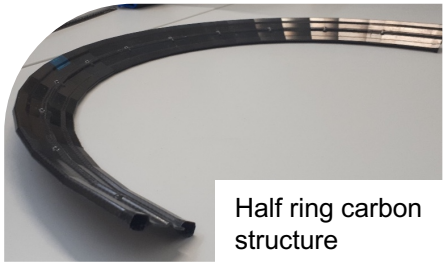


Functional longerons and inclined units with half rings

Not to scale

Produced in EP-DT-EO and Uni Geneva





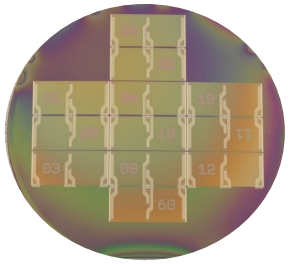
Half layer with inclined units and longerons (services not shown)

- Single and quad modules
- Layout differs in detector areas: varying serial powering chain lengths and varying mechanical solutions to achieve high thermal and electrical performance for stable and safe operation

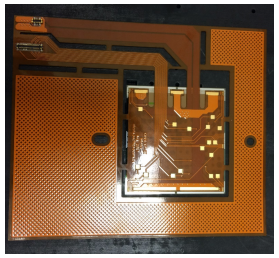
→ Validation in different prototypes

Results of thermal prototypes and simulations

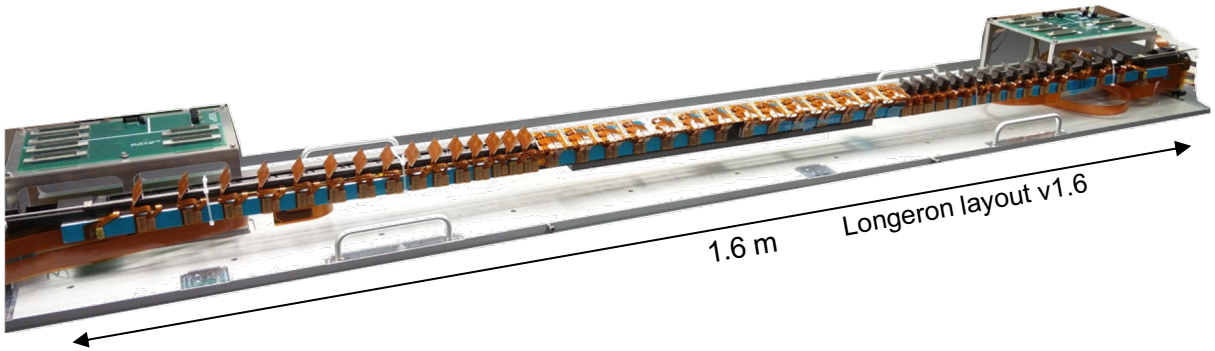
- For outer barrel: longeron with 44 silicon heaters with embedded RTDs evaluated



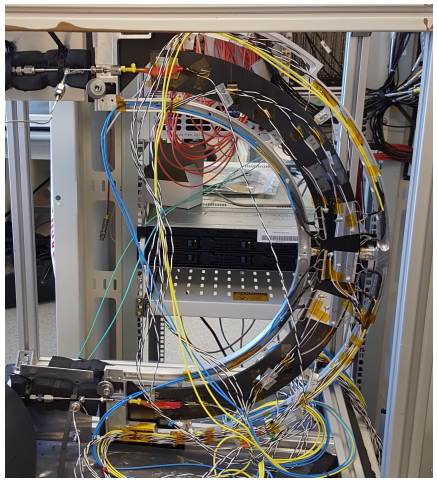
Wafer of heaters



Quad heater with flex

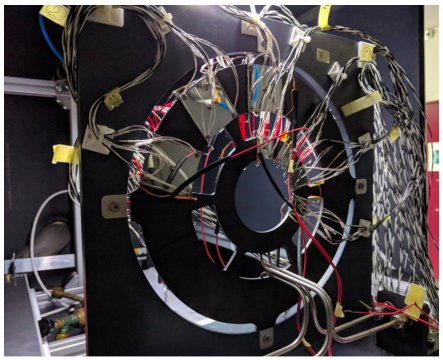


- For endcap: half-ring with temp. sensors on silicon



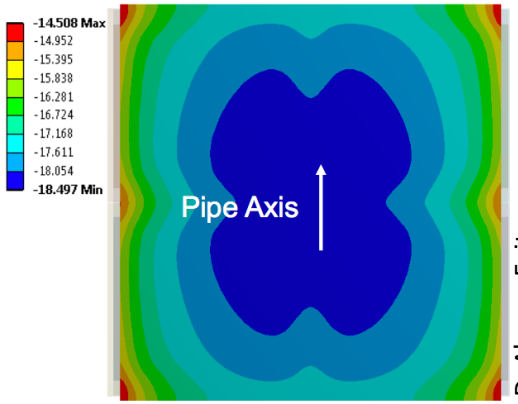
F. Munoz Sanchez

- For inner: ring with temp. sensors on silicon



- CO_2 cooling at -10°C
- Heaters powered in steps from 0.1 to 0.7 W/cm^2

- Thermal FEA simulation



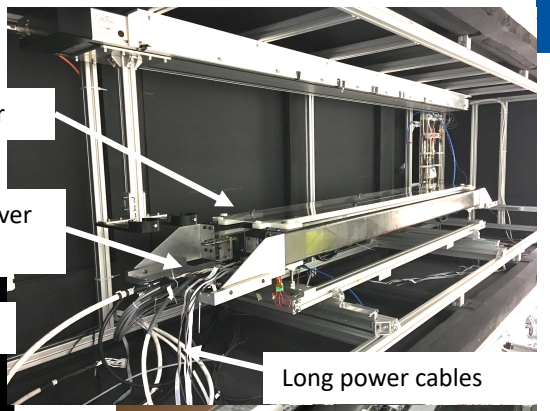
D. Alvarez Feito

Example: sensor temperature in outer barrel flat section

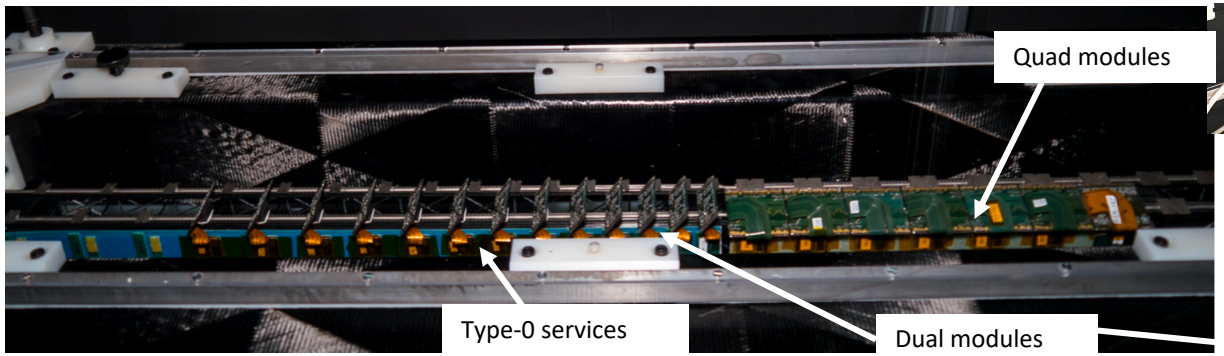
→ **Evaluation of thermal performance and manufacturing variability ongoing**
→ **Initial results and simulations within thermal specifications**: hottest spot on FE expected to be colder than 0°C at the end-of-lifetime

System tests with FE-I4 based prototypes

- **Outer barrel demonstrator program**
  - Short electrical 7-quad module structure
  - Long prototype with 4x8 dual modules and 2x7 quad modules → up to 120 FE-I4 ASICs
  - 6 SP-chains, currently 3 under evaluation

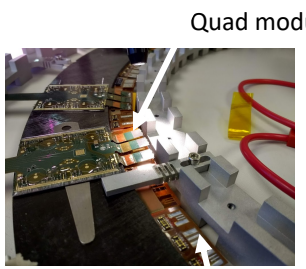


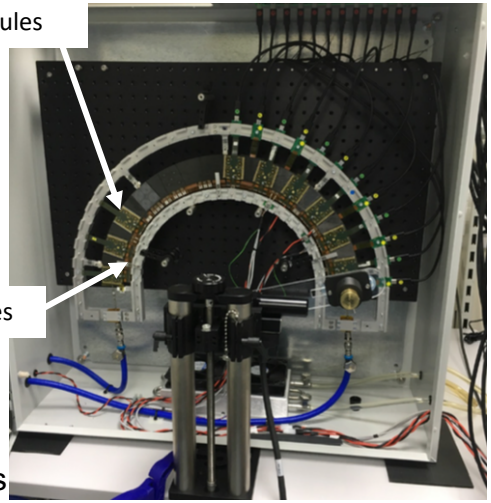
https://cds.cern.ch/record/2661761?ln=en

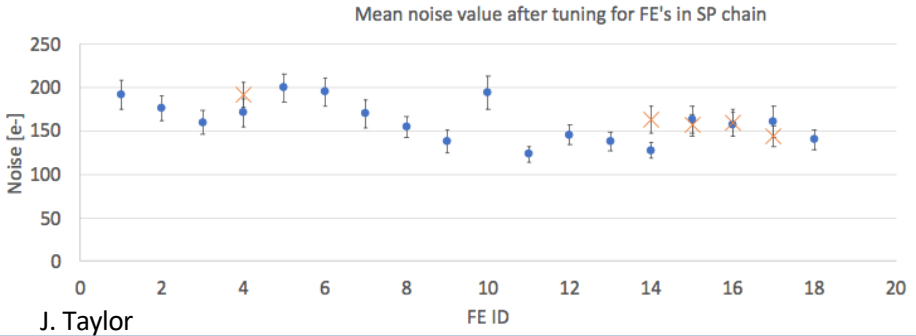


- **Endcap Ring-0**
  - CFRP + carbon foam half-ring with 12 quad modules loaded on top
  - Flexes for 2 SP-chains

→ Evaluation of many system aspects
→ Early practice run for design and integration







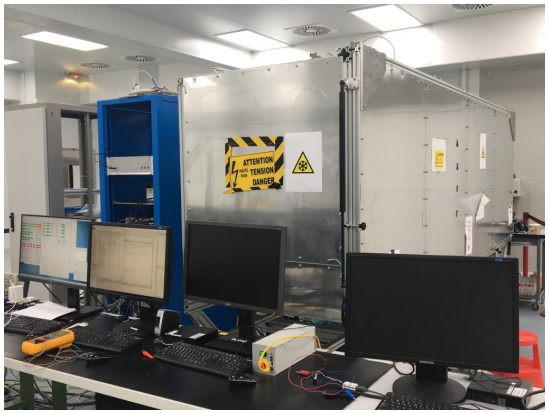
J. Taylor

→ Performance comparable to standalone operation of modules

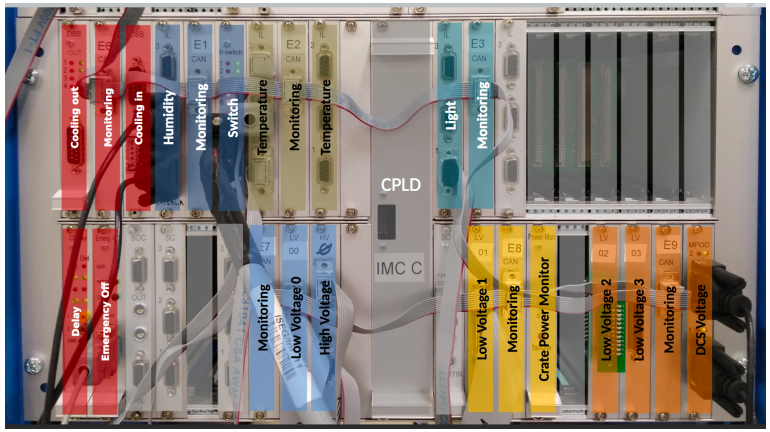
System test setup at CERN

CO_2 plant with ~1.4 kW at -30°C

Racks and PCs for DCS, interlock matrix, PSUs and readout



Light-tight and insulated **box**
Sensors for dew-point, humidity, temperature, light, door switches
Motorized stage for source scans

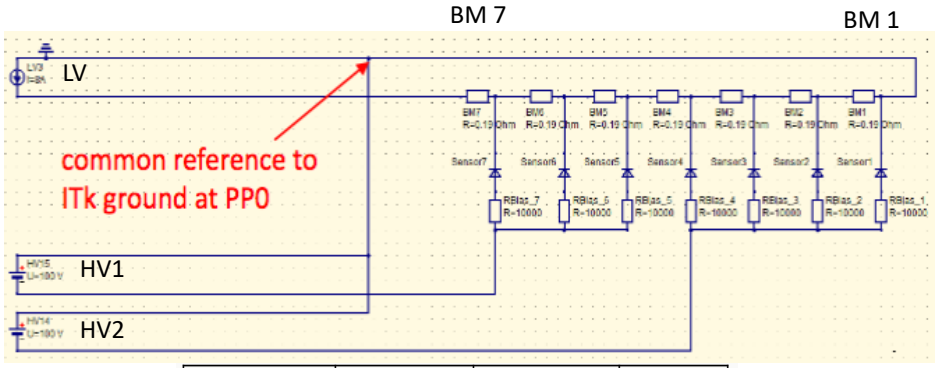


User interfaces for detector interlock, control/monitoring and diagnostics, independent operation

Large common effort!

Results of electrical pixel prototypes

- Tests with different **readout systems** give comparable results
- **Serial powering features**
  - Measurements with realistic power supplies and services scheme → Leakage current return through **HV power supply with low-ohmic off-mode required** to avoid forward bias on module with lowest ground level in chain → **Input to PSU specifications**

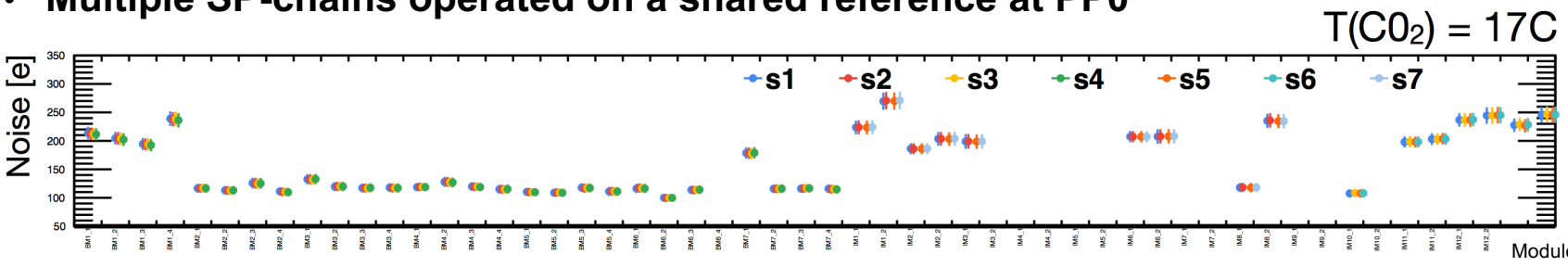


Module	Voltage Drop [V]	Drop over R_HV [V]	ISensor [uA]
BM1	2.12	0.333	30.27272727
BM2	1.78	-0.023	-2.3
BM3	1.95	-0.219	-19.90909091
BM4	1.99		
BM5	2		
BM6	2	-0.041	-3.727272727
BM7	2.01	-0.053	-4.818181818

- **Power fluctuations**
  - Several observations (power fluctuations induced during reset of GBT, register start-up) underline the necessity of the improvement of the shuntLDO regulators
    → Input to RD53 chip requirements, undershunt current protection and overvoltage protection

	powering scheme		
Scenario	SC1	SC2	SC3
1	1	1	1
2	1	1	0
3	1	0	1
4	1	0	0
5	0	1	1
6	0	0	1
7	0	1	0

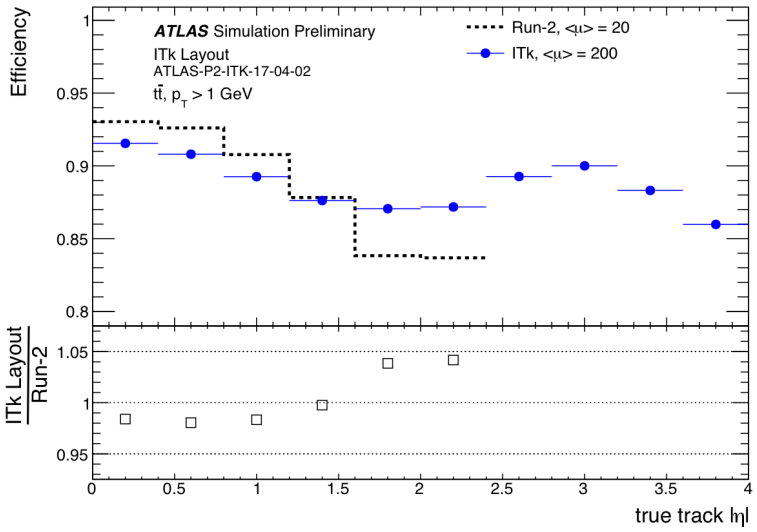
- **Multiple SP-chains operated on a shared reference at PP0**



Fully functional

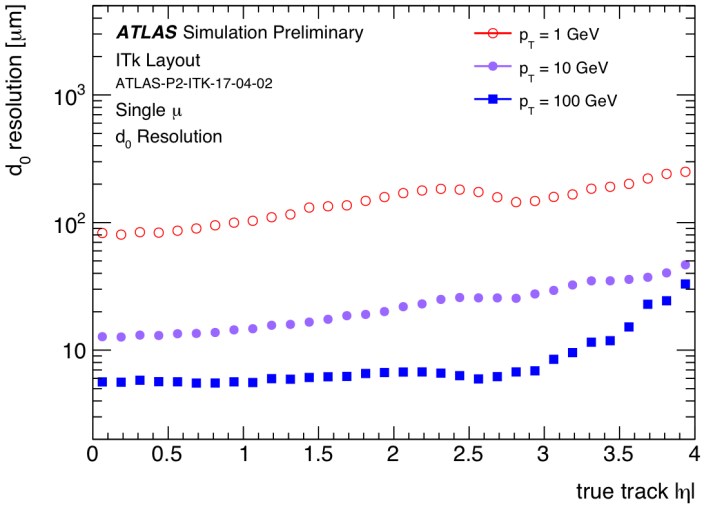
Simulated ITk Performance

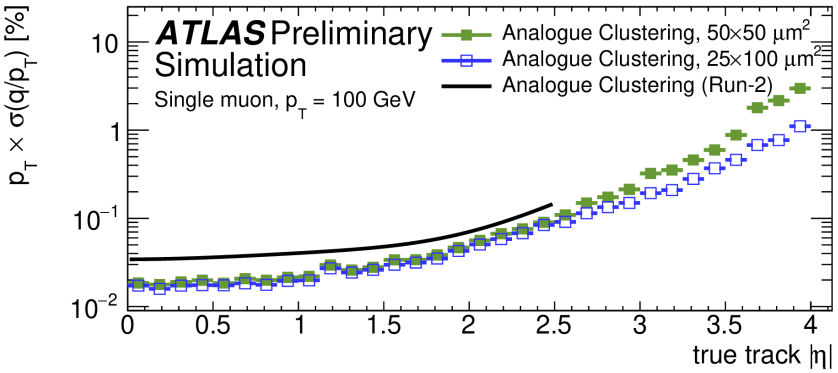
- Track reconstruction efficiency in $t\bar{t}$ events with ⟨μ⟩=200 for the ITk Layout > 87%
- Fake rate < 10^{-4}



PLOT-IDTR-2019-09

- High track parameter resolution





ATL-PHYS-PUB-2019-014

- Improved resolution and robustness compared to present inner detector
  - Strip detector has higher performance than TRT
  - Improved efficiency at |η| > 2.5 even in harsher conditions
  - Smaller pitch in ITk
  - Reduction of radius of pixel-layer 0

Summary

- **New inner tracker in preparation for the ATLAS experiment for HL-LHC**
- 5-layer pixel detector with about 10,000 pixel-hybrid modules (~6 x of current pixel detector)
    - New FE chip, sensors, powering scheme, services scheme and equipment getting designed and produced as prototypes
    - Collaboration working on the validation of the prototypes (electrical and thermal ones, assembly and testing procedures getting defined)
    - Challenges are the verification of data transmission concept and module stress
- 4-layer strip detector with about 18,000 strip modules
    - Design verified and many final design reviews passed
    - Pre-production fully running (QA/QC procedures defined, site qualification ongoing)
- Expected performance will enable rich physics program

Thank you!

Questions?

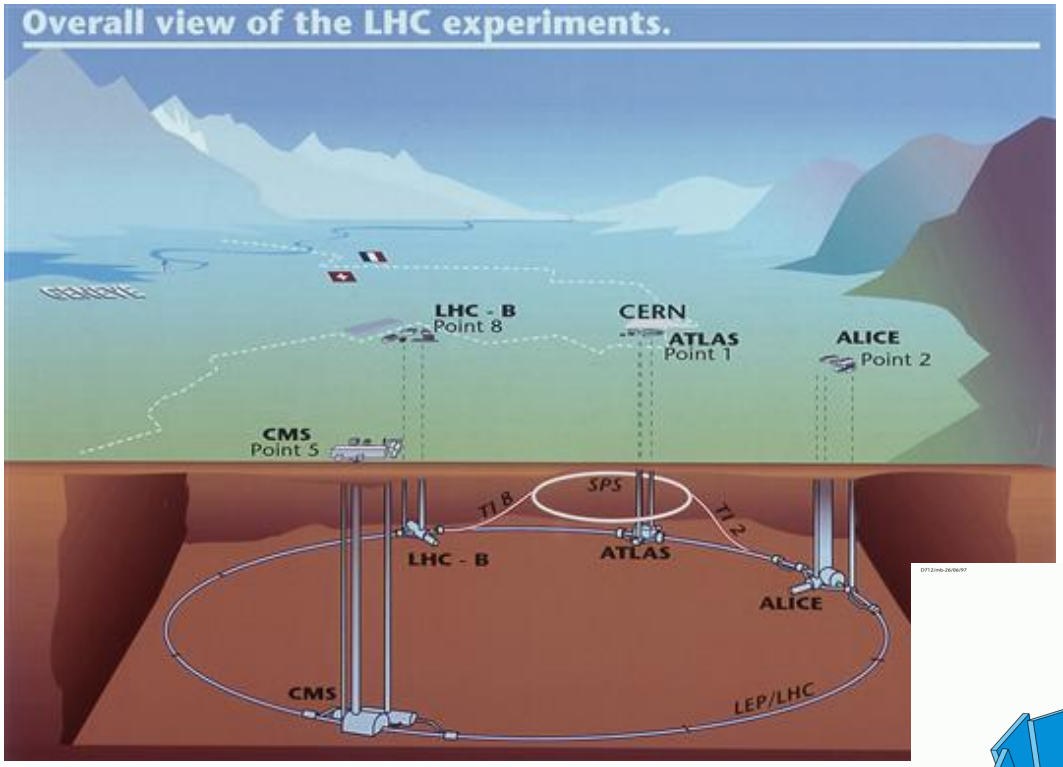
Thank you!

Questions?

Spare

Thank you for material to
Tony Affolder, Attilio Andreazza, Andrew Blue, Craig Buttar, Sergio Diez Cornell, Diego Alvarez Feito, Tobias Flick, Claudia Gemme, Matthias Hamer, Fabian Hügging, Heinz Pernegger, Carlos Solans, Dennis Sperlich, Sven Wonsak

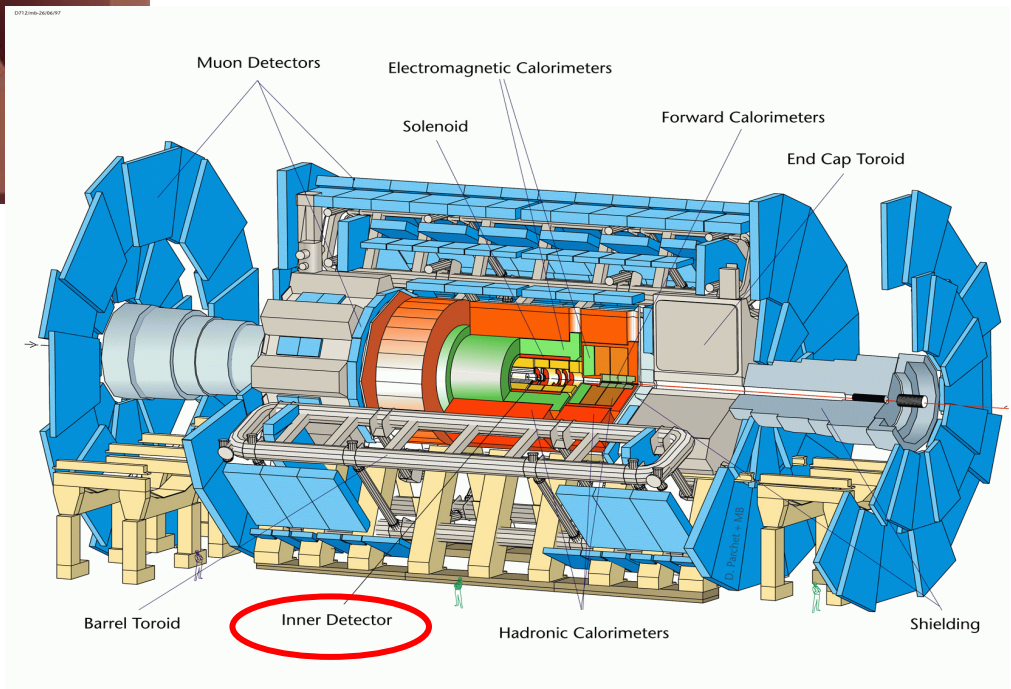
The LHC and the ATLAS experiment



Large Hadron Collider

- p-p, p-HI, HI-HI collider
- up to 14 TeV p-p collisions

Multi-purpose experiment ATLAS

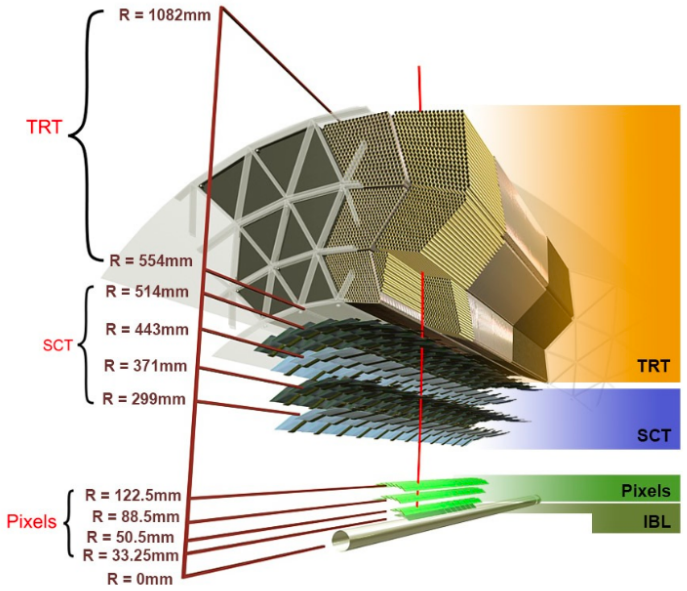


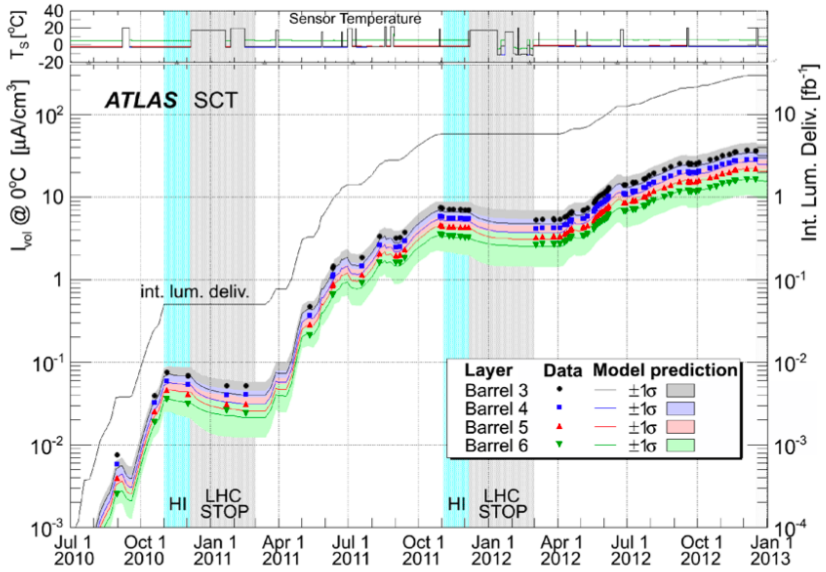
- Many interesting results: Standard model verification, Higgs discovery, first precision measurements
- Exclusion of some popular models
- Probing of Higgs-Sector and TeV-scale BSM requires more data

→ High Luminosity LHC

Inner Detector of the ATLAS Experiment

- Current inner tracker of ATLAS performing very well
- Transition radiation detector and silicon detectors for tracking
  - Planar strip sensors
  - Hybrid pixel with planar and 3D sensors
- However, cannot cope with radiation damage and high occupancy at HL-LHC operation





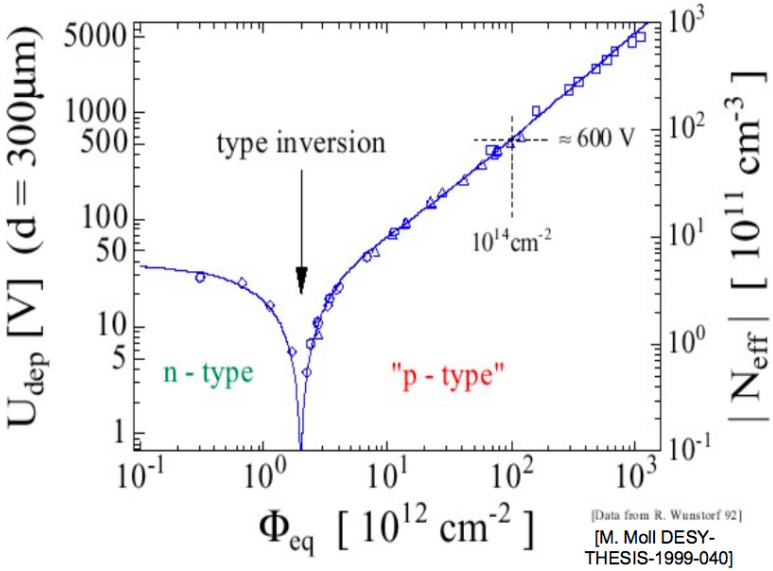
Detector	Area [m²]	Channels	Maximum dose [1MeV n_{eq}/cm²]
Pixel	1.8	92 M	up to $3*10^{15}$
Strip	60	6 M	up to $2*10^{14}$

Radiation Damage in Silicon Sensors

Radiation damage: non-ionising energy loss of charged and neutral particles
→ damage in silicon bulk

Effects:

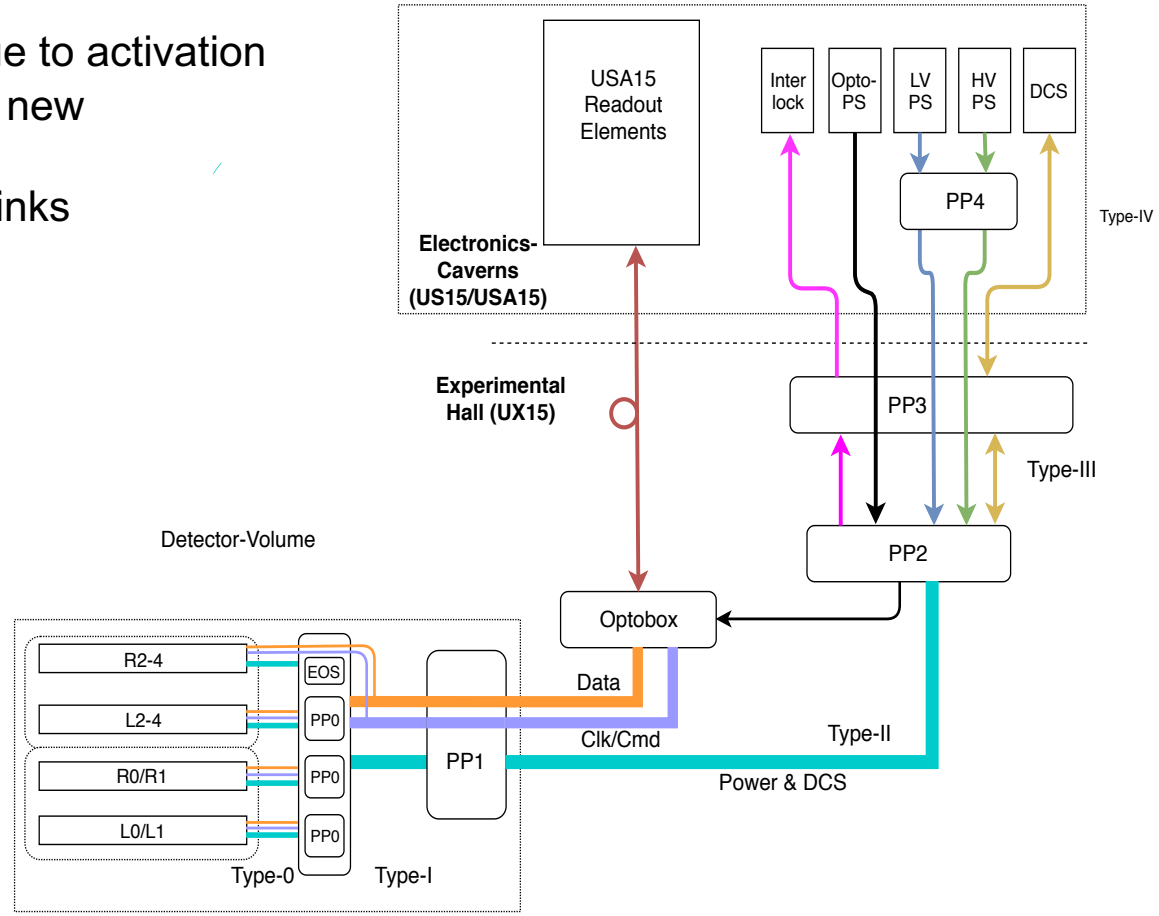
- Increase of leakage current
- Change of effective doping concentration
- Increase of depletion voltage
- Defects act as trapping centres affecting the charge collection efficiency



→ Radiation damage degrades the detector performance and limits the life time

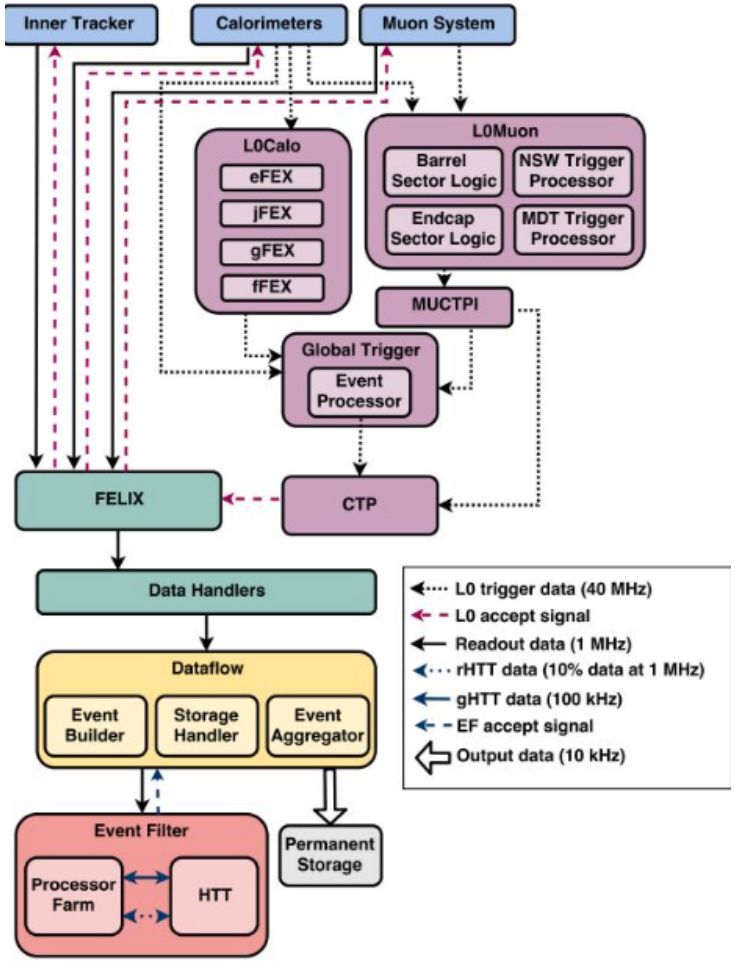
Pixel Services

- Four types of data and power cables from USA15 to the detector
- Reuse most of the type-III cables, plus additional ones for DCS
- Type-II cables will be replaced due to activation
- Type-0 and type-I are completely new
- Not accounting for cooling
- Optimized the amount of optical links

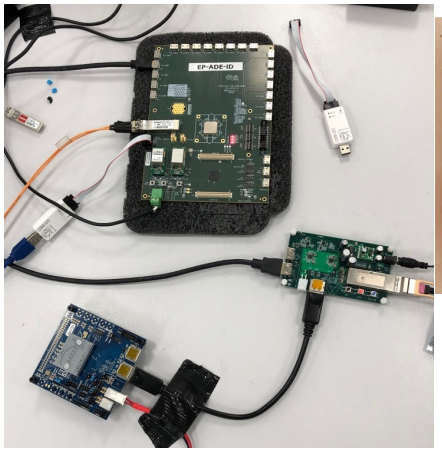


Detector Readout with FELIX

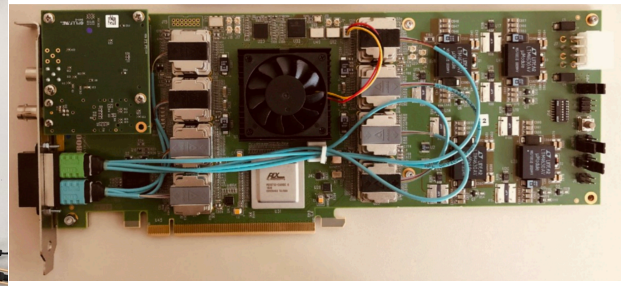
CERN-LHCC-2017-020



- Full FELIX read-out
  - 24 lpGBT links per FELIX IO card
  - Based on network subscription protocol
  - No hardware access to FELIX IO card
- Challenge for calibration and DCS
  - Tuning of front-end prototypes adapted
  - Implications for DCS under discussion



ANL RD53A readout setup



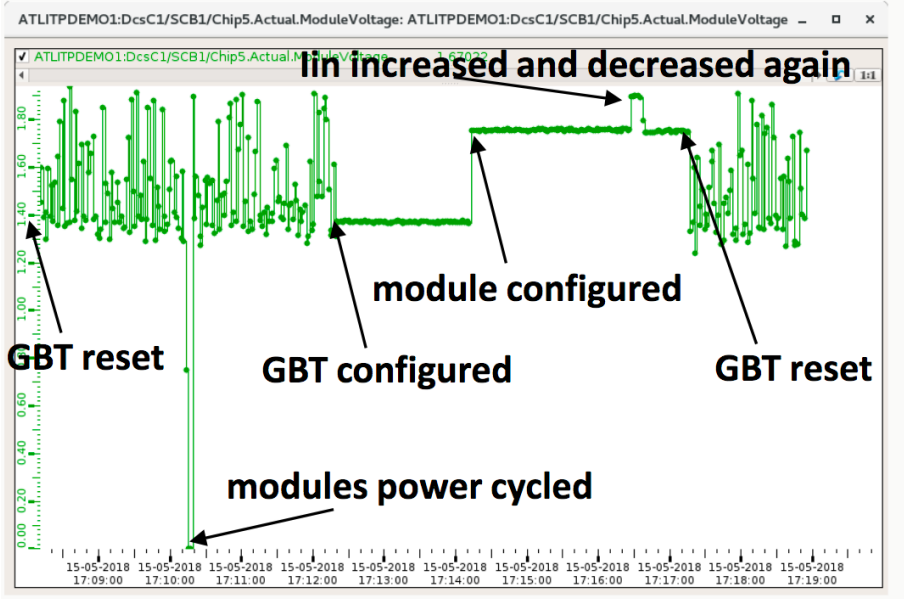
FELIX Phase-I IO card (FLX-712)

Development for adaptions of firmware and hardware heavily ongoing to operate strip and pixel prototypes

Further observations with 7-module tests

- Optical driver chip (GBT) induced power fluctuations during reset: to be checked with new version of chip (lpGBT) and also RD53 front-ends → Input to requirement of front-end chip

- Differences in power in module voltage after startup and first configuration (up to 600 mV): feature how registers are set at startup (hopefully only in FE-I4)



Irradiation Campaign

- Not only FE, sensors and ASICs need to be qualified but also all glues and materials
- Radiation campaign for adhesives, resins, wirebond encapsulants and local support materials coordinated by Nicola Pacifico.
- More on https://maxrad.web.cern.ch/maxrad/

Thermal Testing

- Sandwich coin samples with Al substrates
- Tested following ASTM D5470

Nicola Pacifico

Electrical Testing

- Dedicated test geometry to measure impedance/attenuation developed at UniGe

Yannick Favre

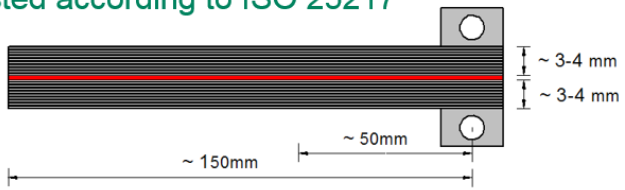
Mechanical Testing

Bulk adhesive properties

- Tensile dog-bone specimens
- Tested according to ISO 527 or ASTM D638

Adhesive bonding/fracture properties

- DCB specimens with CFRP substrates
- Tested according to ISO 25217



Detector control system

- Detector control for operation and user interface to allow
  - Interlock
  - Control/Monitoring
  - Diagnostics