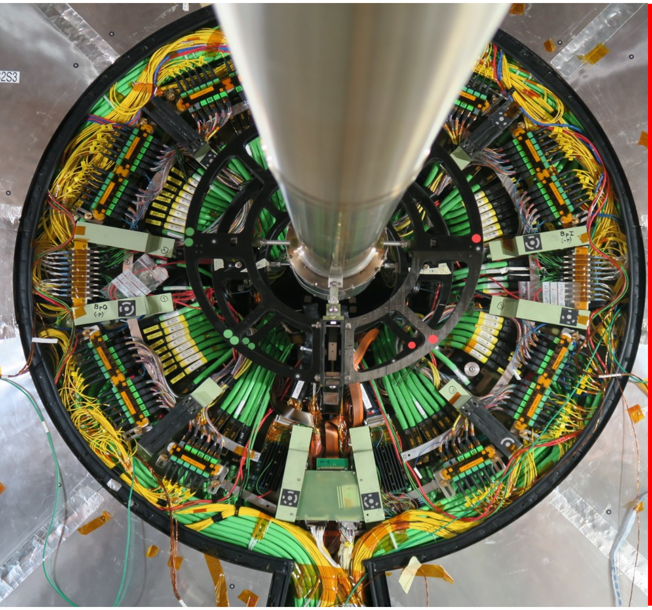

Two years of the phase-1 CMS pixel detector

technology choices, operational experience, and future prospects

Benedikt Vormwald
Joint Instrumentation Seminar
DESY Hamburg
14.06.2019

Universität Hamburg
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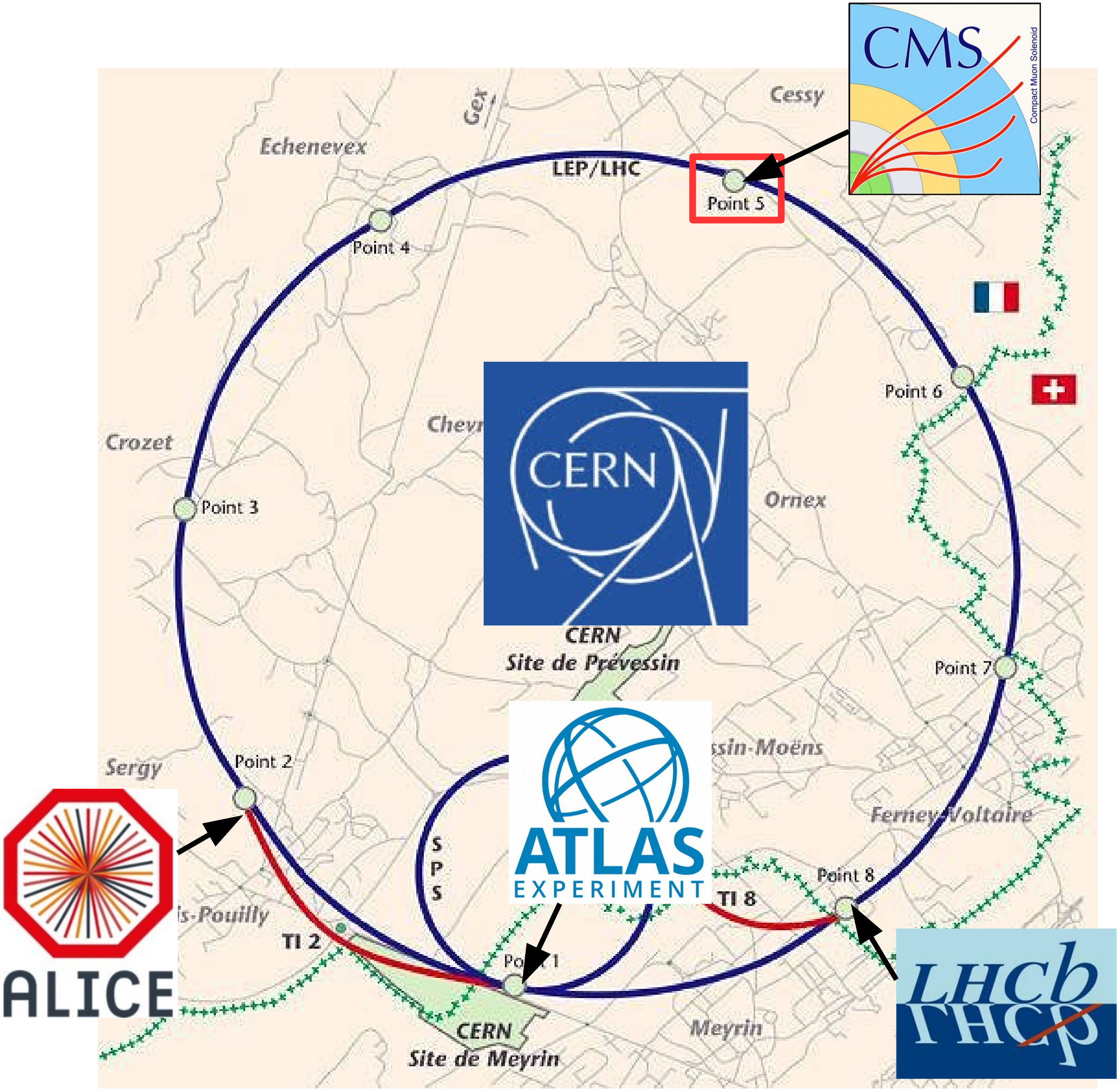
CLUSTER OF EXCELLENCE
QUANTUM UNIVERSE

Large Hadron Collider



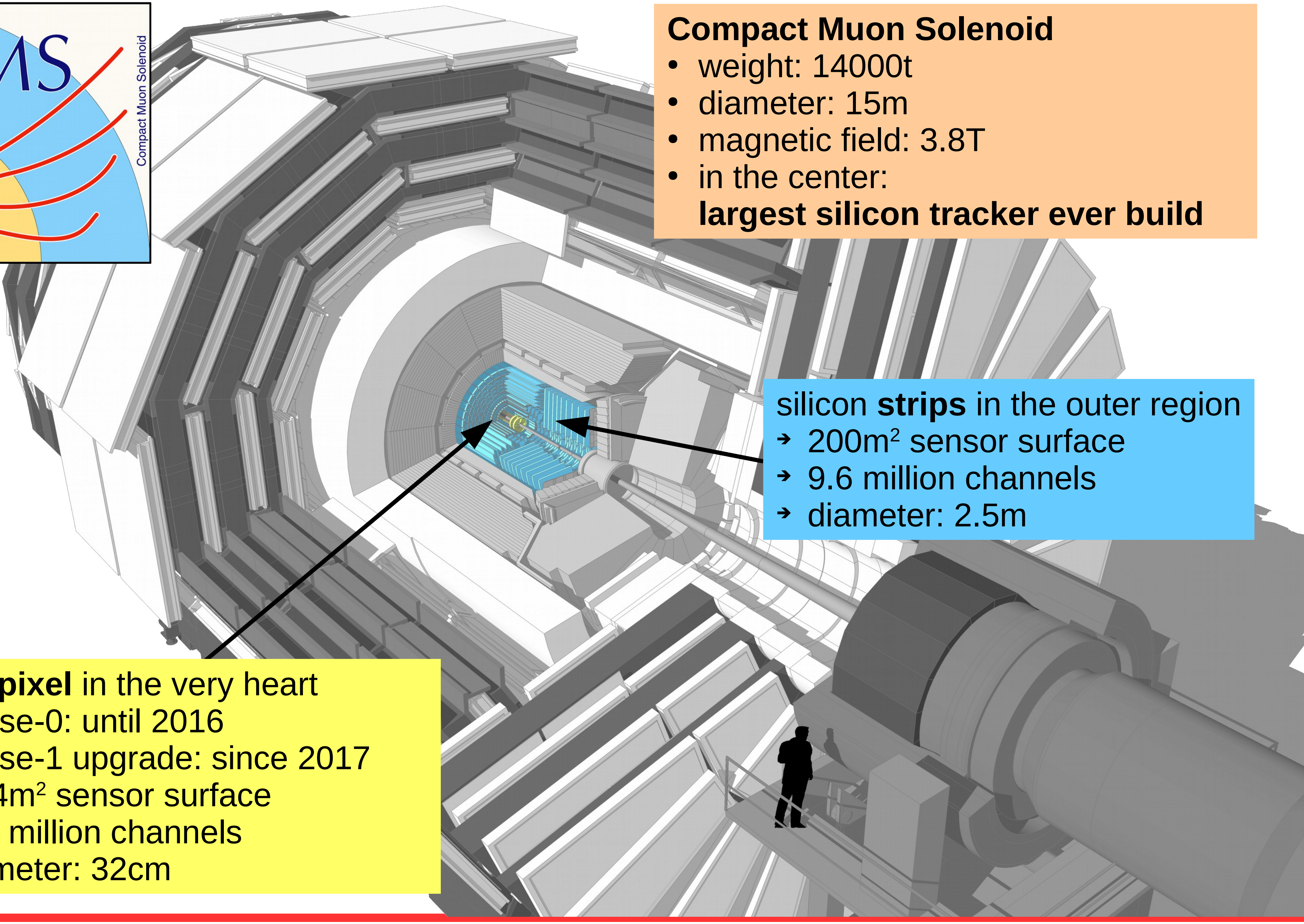
largest and most powerfull collider in the world

- locates at CERN near Geneva
- **p-p collisions**
- 13 TeV center-of-mass energy

running conditions in 2018:

- 40MHz collision rate
- ~50 pile-up events per bunch crossing
- luminosity: <2e34 cm^{-2} s^{-1}

CMS and its Tracker

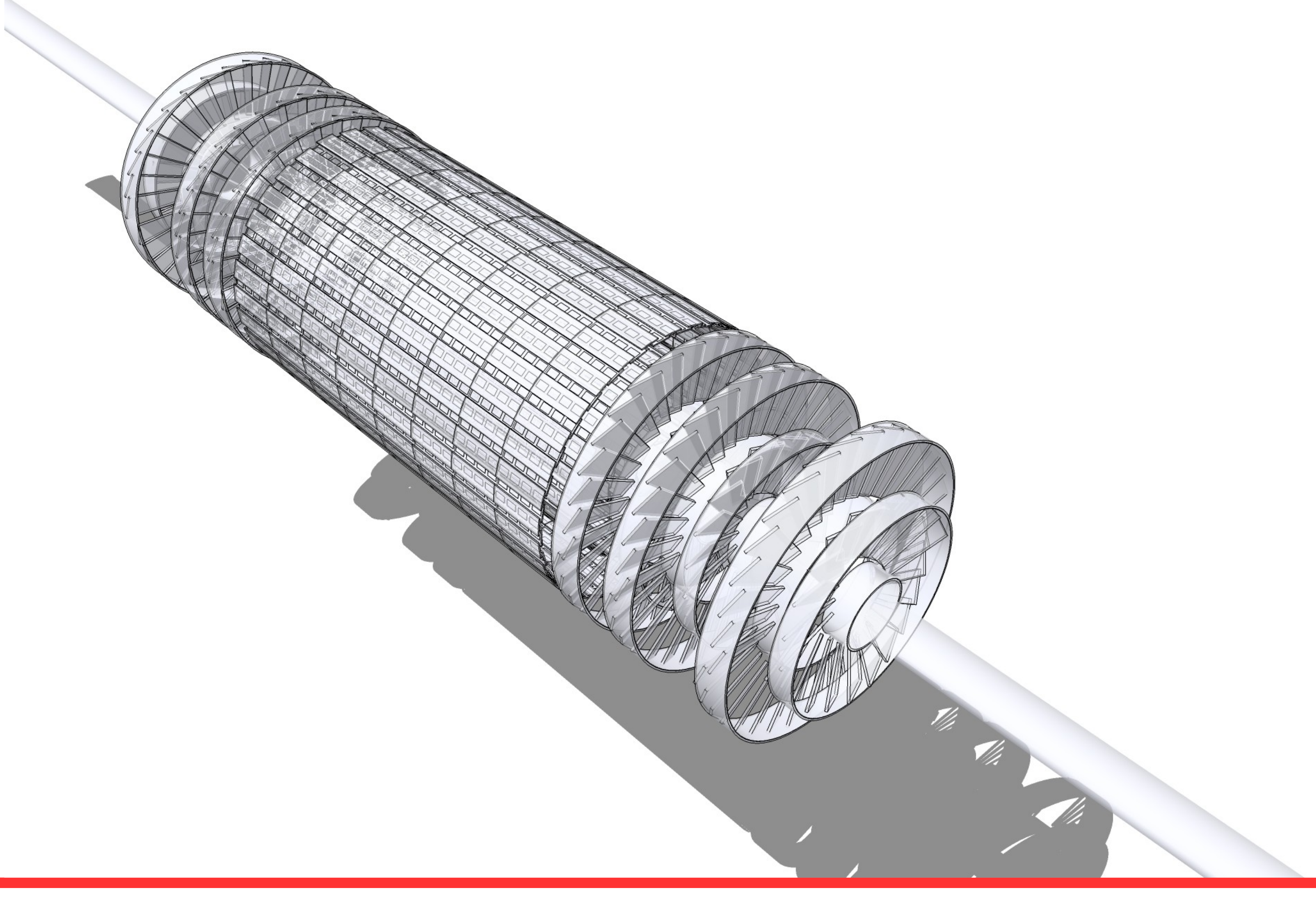


Compact Muon Solenoid
- weight: 14000t
- diameter: 15m
- magnetic field: 3.8T
- in the center:
  largest silicon tracker ever build

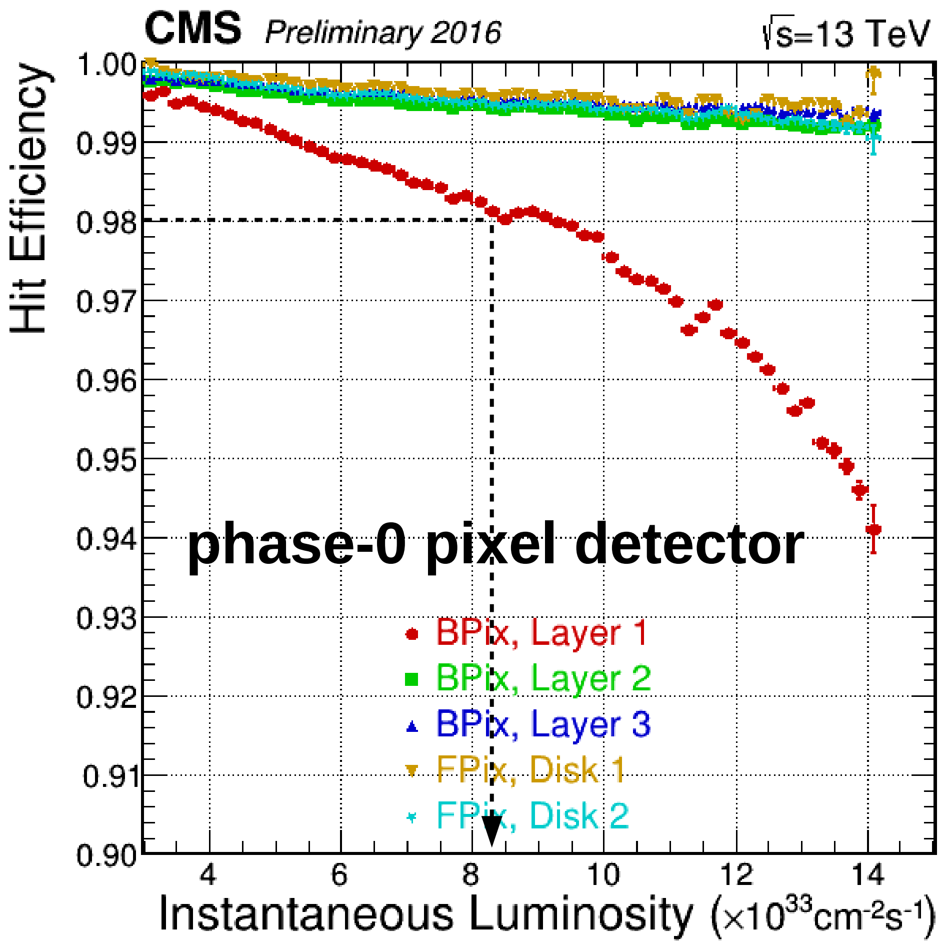
silicon **strips** in the outer region
- ➔ 200m^2 sensor surface
- ➔ 9.6 million channels
- ➔ diameter: 2.5m

silion **pixel** in the very heart
- ➔ phase-0: until 2016
- ➔ phase-1 upgrade: since 2017
- ➔ 1.24m^2 sensor surface
- ➔ 124 million channels
- ➔ diameter: 32cm

The CMS Phase-1 Pixel Detector

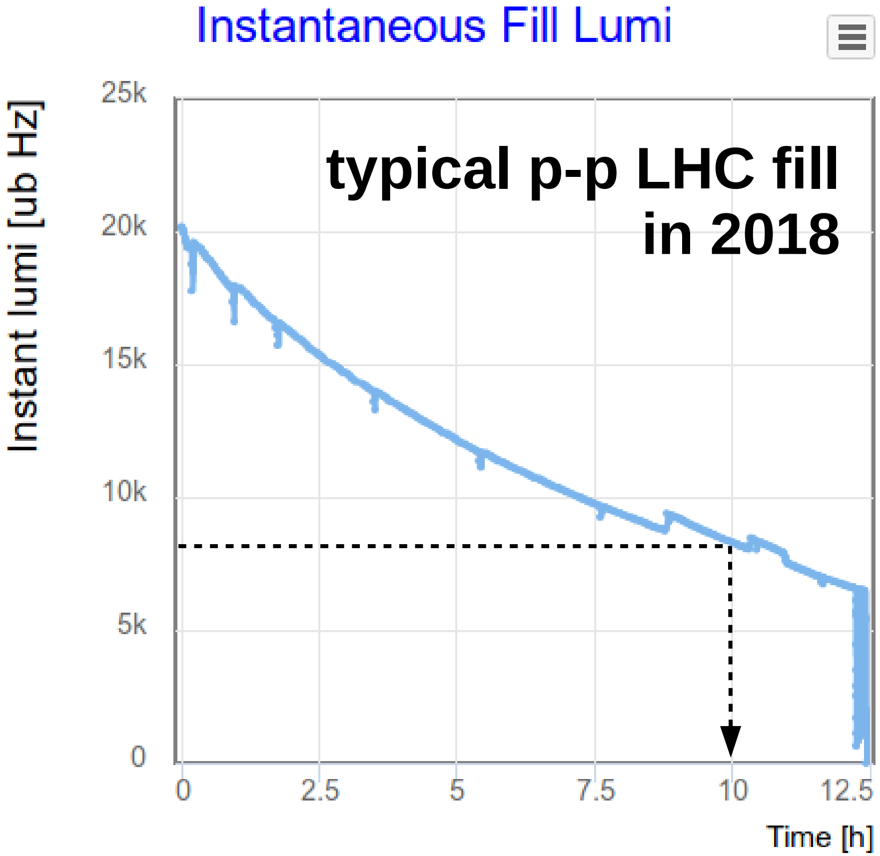


Why did we need an upgrade?



making the case

- with the old detector: >10h data taking with an inefficiency in layer 1 larger than 2%
- extrapolation to 2e34 cm^{-2}s^{-1}: 30% inefficiency
- clearly demonstrates that an upgrade is necessary



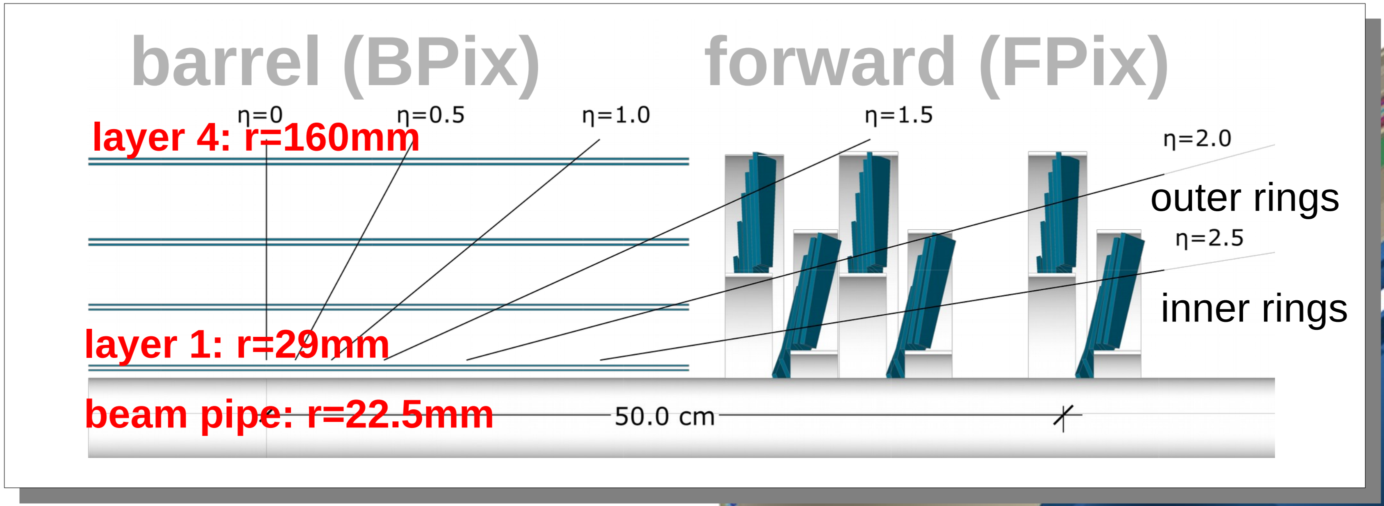
design guidelines for phase-1

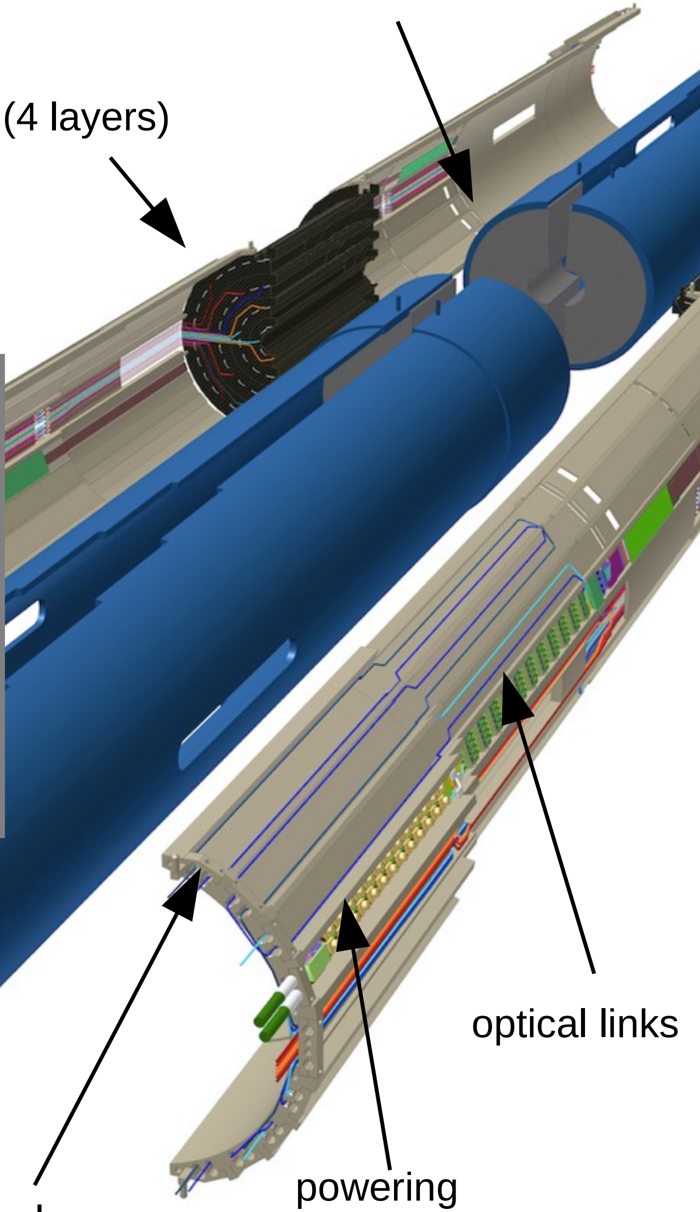
- improved ROC
- increased bandwidth
- additional tracking layer
- optimization of material budget

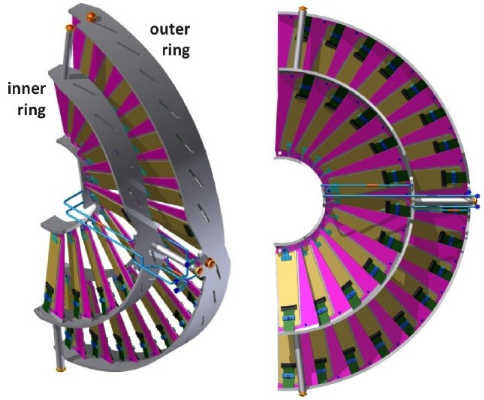
CMS Phase-1 Pixel Detector

mechanical design

- 4-hit coverage up to |η|<2.5
- closer first pixel layer (new beam pipe)
- turbine-like module arrangement in forward disks
- inner rings tilted for optimal radial and azimuthal resolution







CMS Phase-1 Pixel Detector

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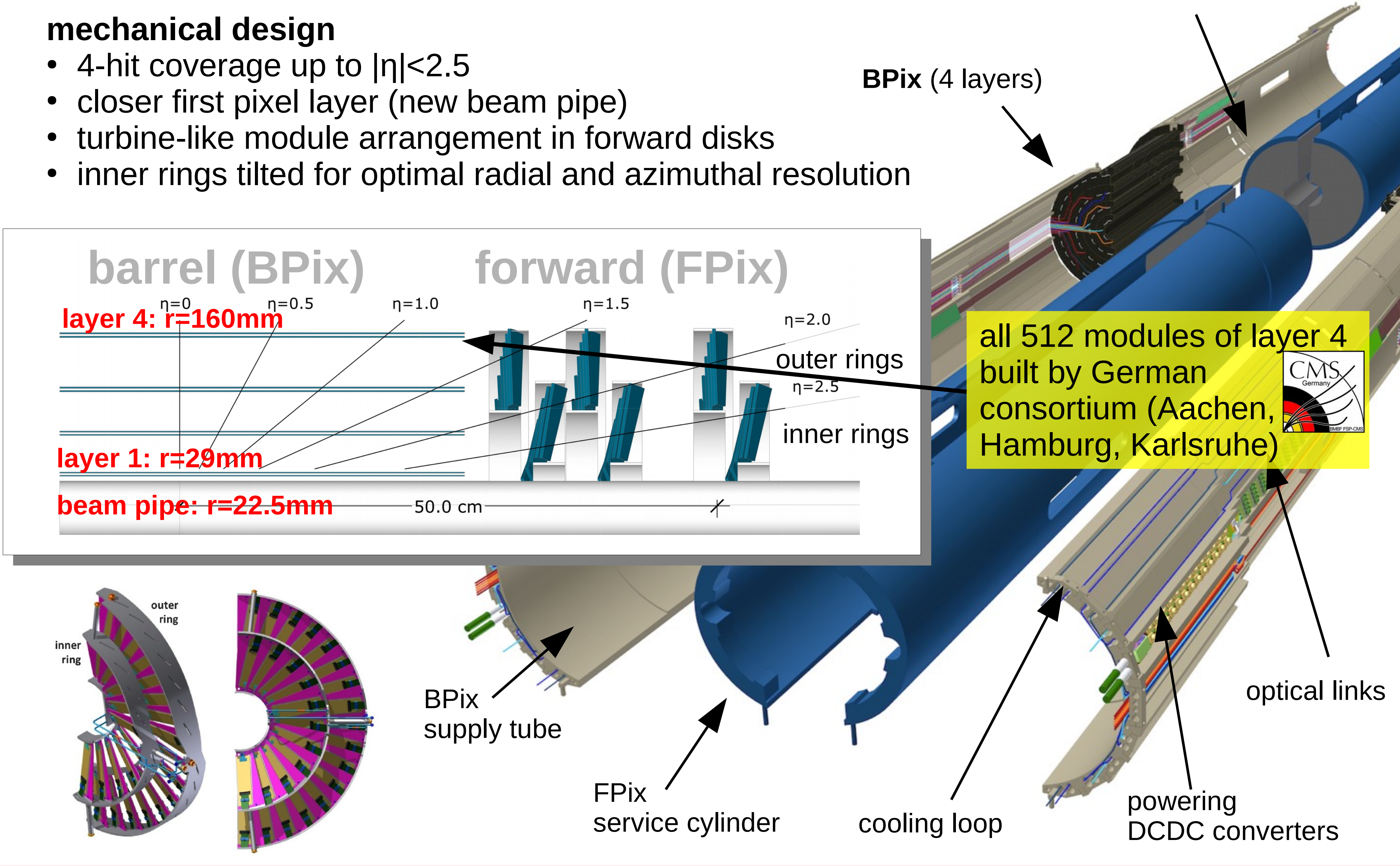
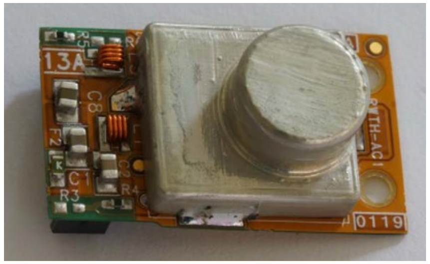
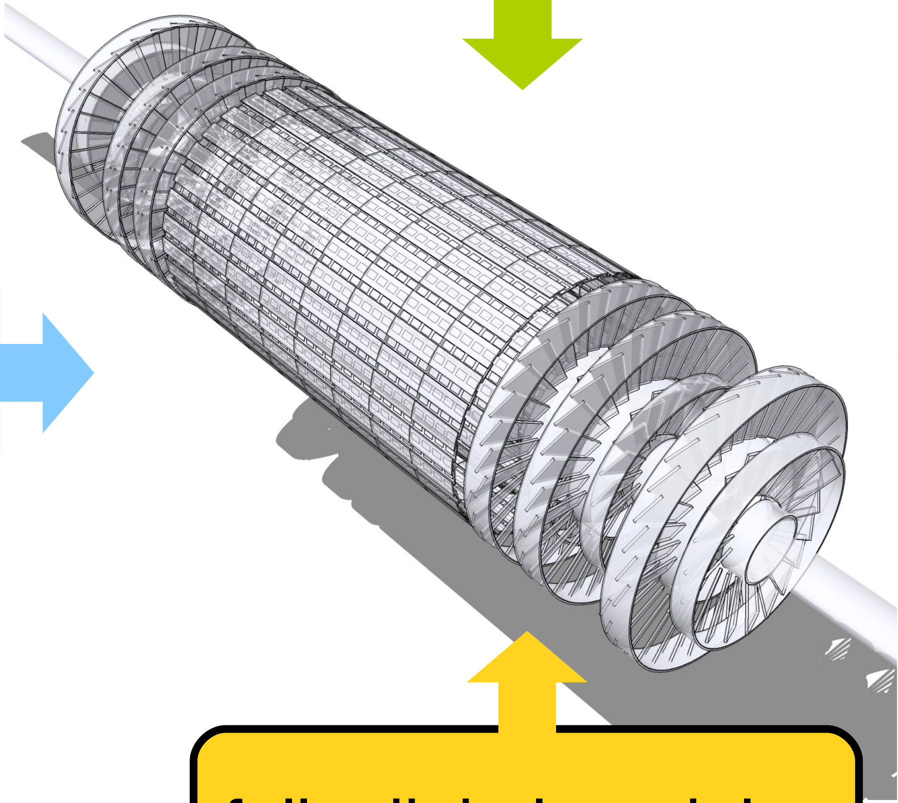


all 512 modules of layer 4 built by German consortium (Aachen, Hamburg, Karlsruhe)

CMS Phase-1 Pixel Detector – Key Technologies

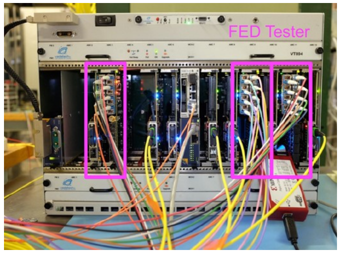


DC-DC powering



CO_2 cooling

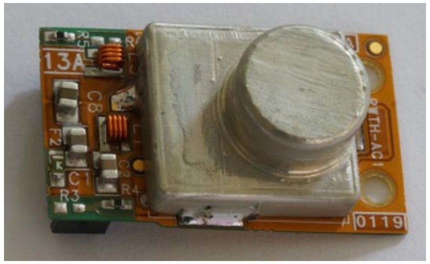
µTCA DAQ



fully digital modules

The Phase-1 Pixel Detector contains many key technologies used in the LHC phase-2 upgrade

CMS Phase-1 Pixel Detector – Key Technologies



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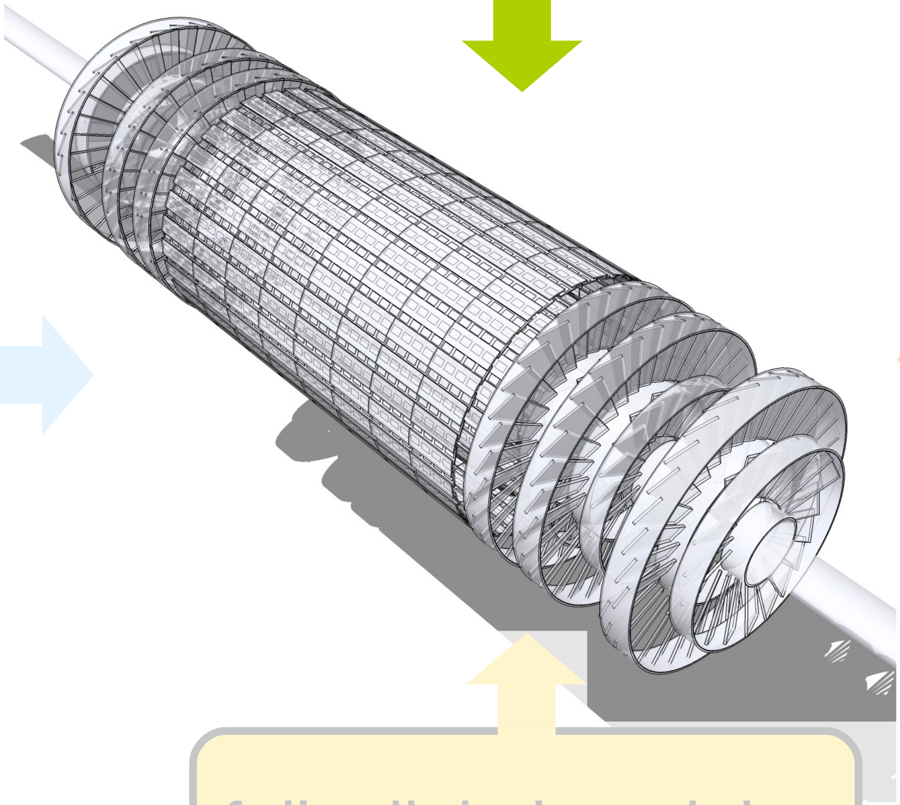


CO_2 cooling

μTCA DAQ

fully digital modules

The Phase-1 Pixel Detector contains many key technologies used in the LHC phase-2 upgrade

DC-DC Powering – Why?

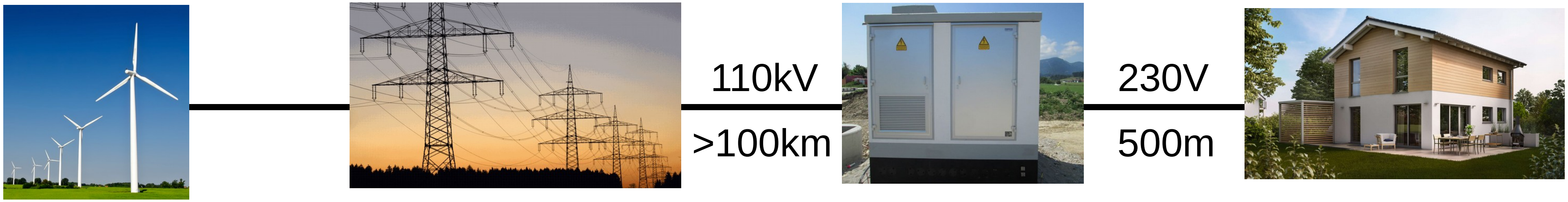
- 1.9 times more channels compared to phase-0
- same number of power cables due to **very** limited space
- without changes: larger currents over the same cable causing large power losses

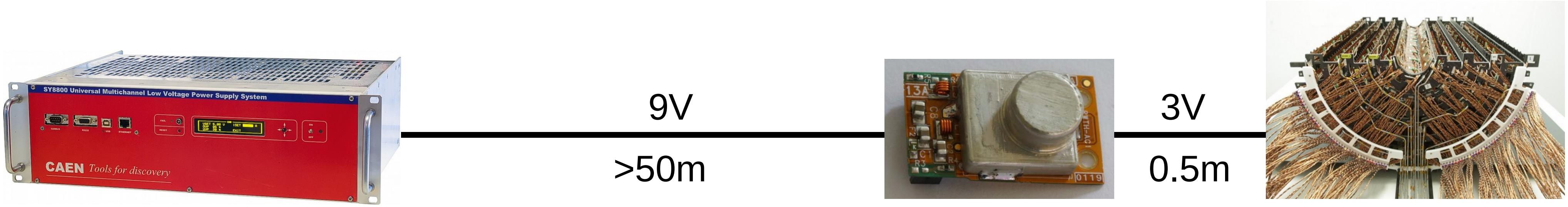
$$P_{cable\,loss} = R\,I^{2}$$

- currents driven by power consumption of the detector module

$$P_{detector} = U \cdot I = const$$

- **solution: transfer energy into detector with higher voltage/lower current and transform just before the load to operation voltage**
- known concept for power supply of households, but we do it with direct currents (DC)



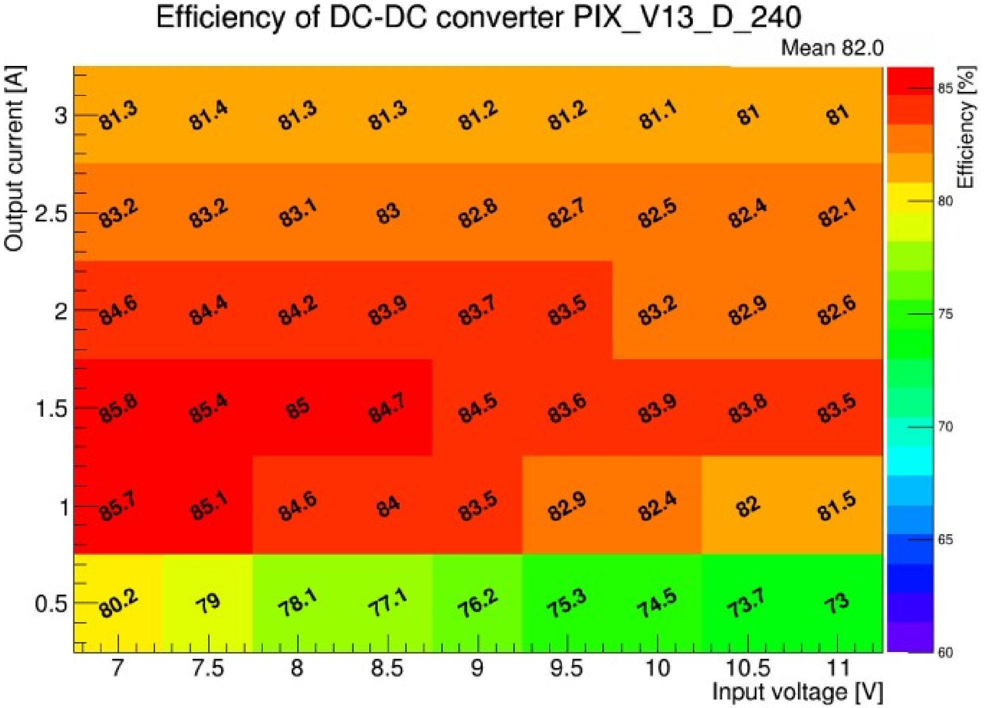


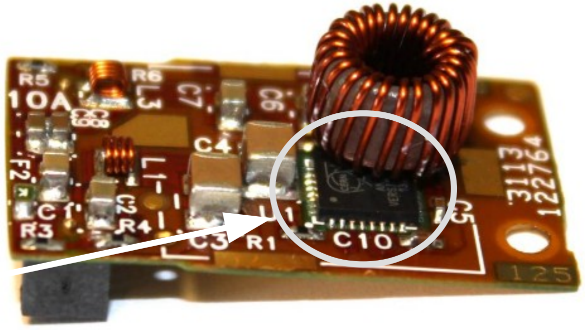
DC-DC Powering

- DC-DC conversion standard technology in electronics
- buck/step-down converter in every computer
- but: not easy to build it radiation hard & magnetic field tolerant

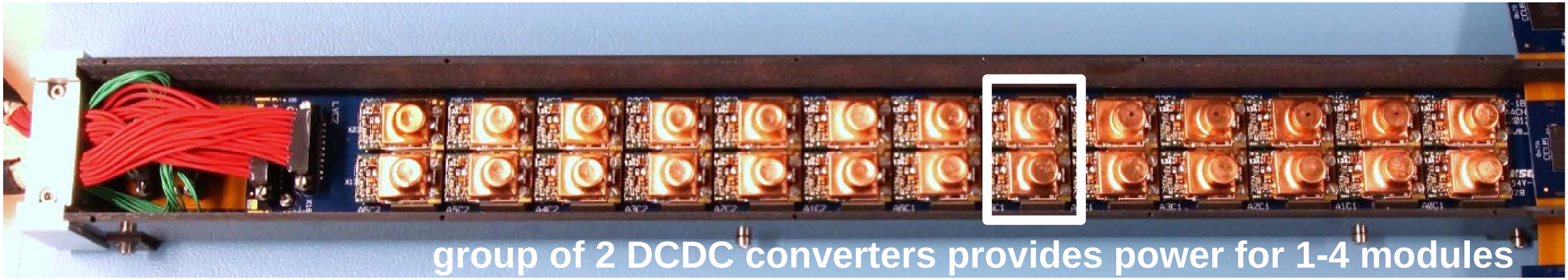
design and specifications

- core: FEAST 2 ASIC designed by CERN
- conversion from 9-12V to 2.4V/3.0V
- magnetic field tolerant: up to 4T
- radiation hard: 150 Mrad (Si), 5e14 n_{eq}/cm^2
- conversion efficiency ~82%



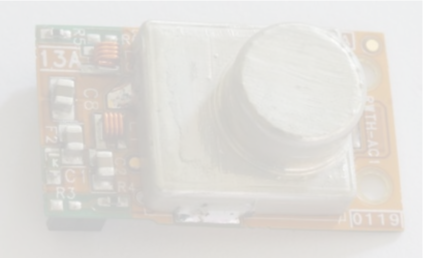


FEAST2

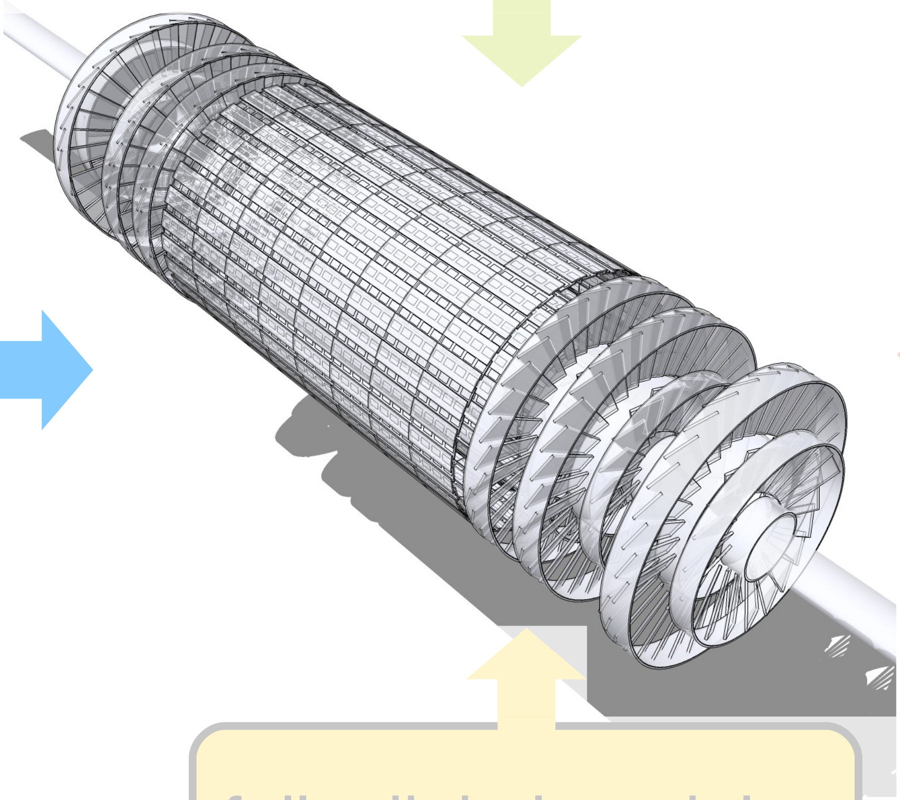


group of 2 DCDC converters provides power for 1-4 modules

CMS Phase-1 Pixel Detector – Key Technologies



DC-DC powering



CO$_2$ cooling

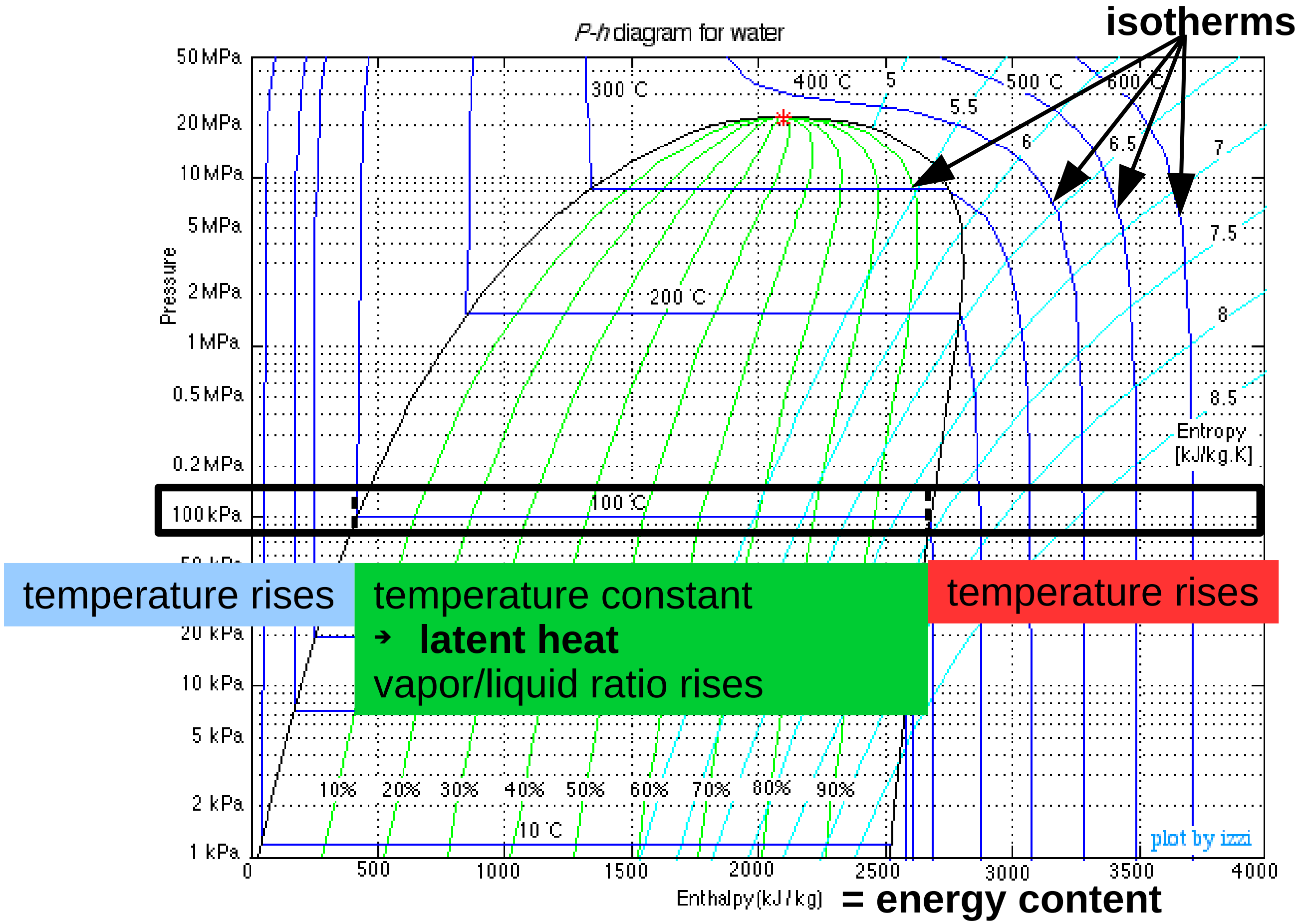
µTCA DAQ

fully digital modules

The Phase-1 Pixel Detector contains many key technologies used in the LHC phase-2 upgrade

Phase Transition and Latent Heat

What happens at a transition between the liquid and gaseous phase?
example: evaporation of water



isotherms

temperature rises

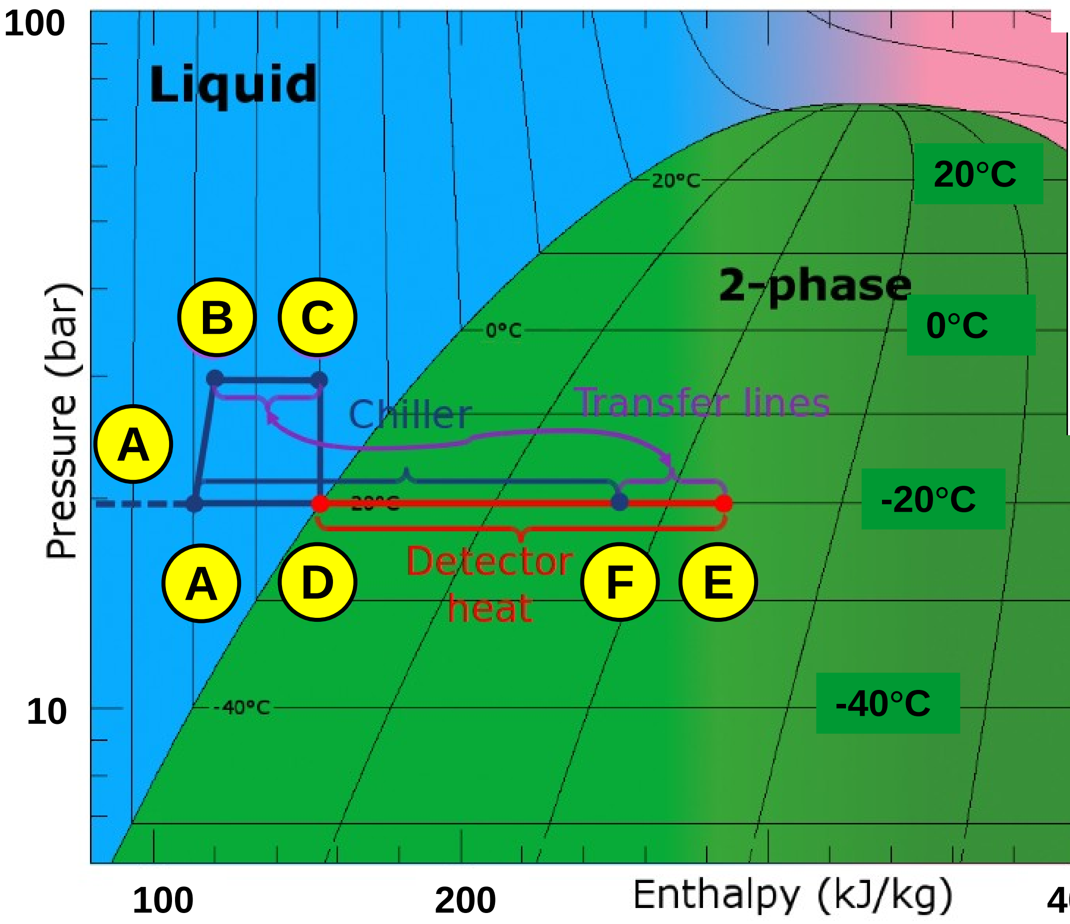
temperature constant
➔ **latent heat**
vapor/liquid ratio rises

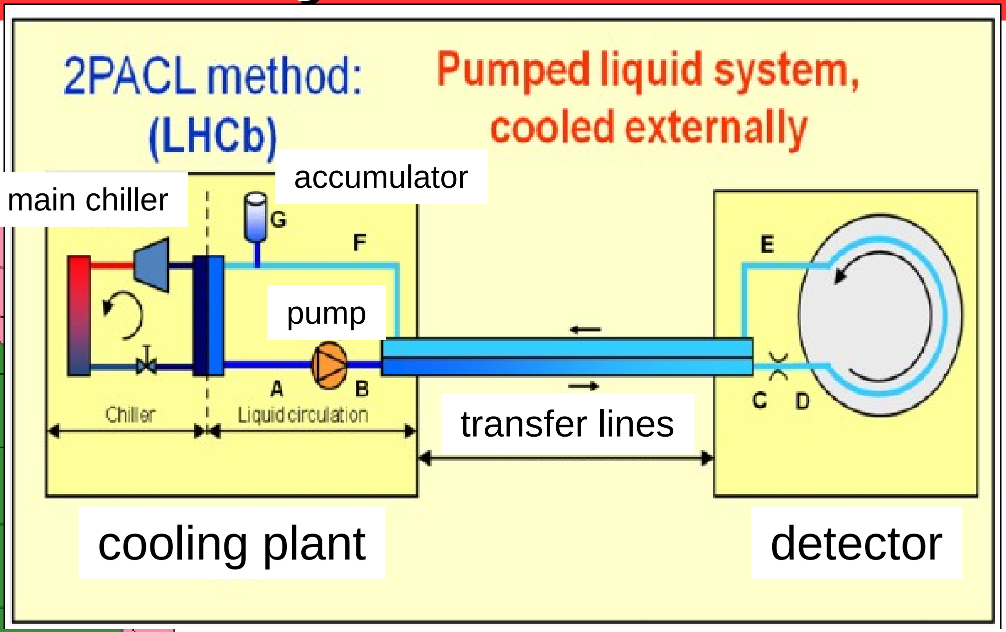
temperature rises

= energy content

- in the **2-phase state** the material can absorb **a lot of energy** without changing temperature
  ➔ **ideal property of a coolant**
- region of 2-phase state of CO2 usable for cooling (-50°C → 30 °C)

CO_2 Cooling – Thermodynamic Cycle



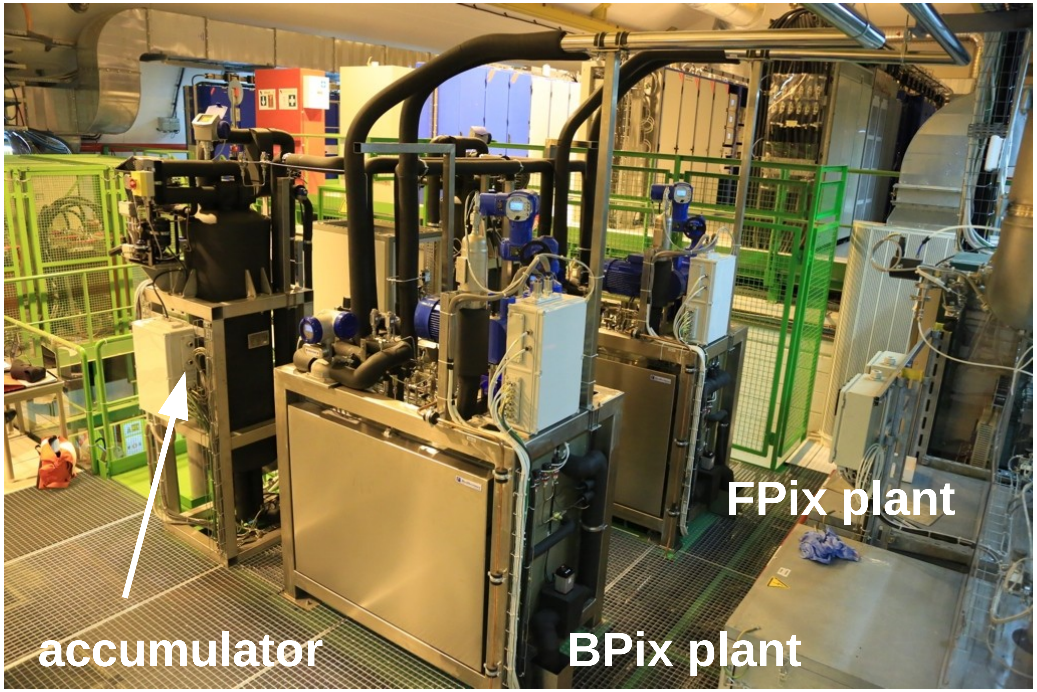


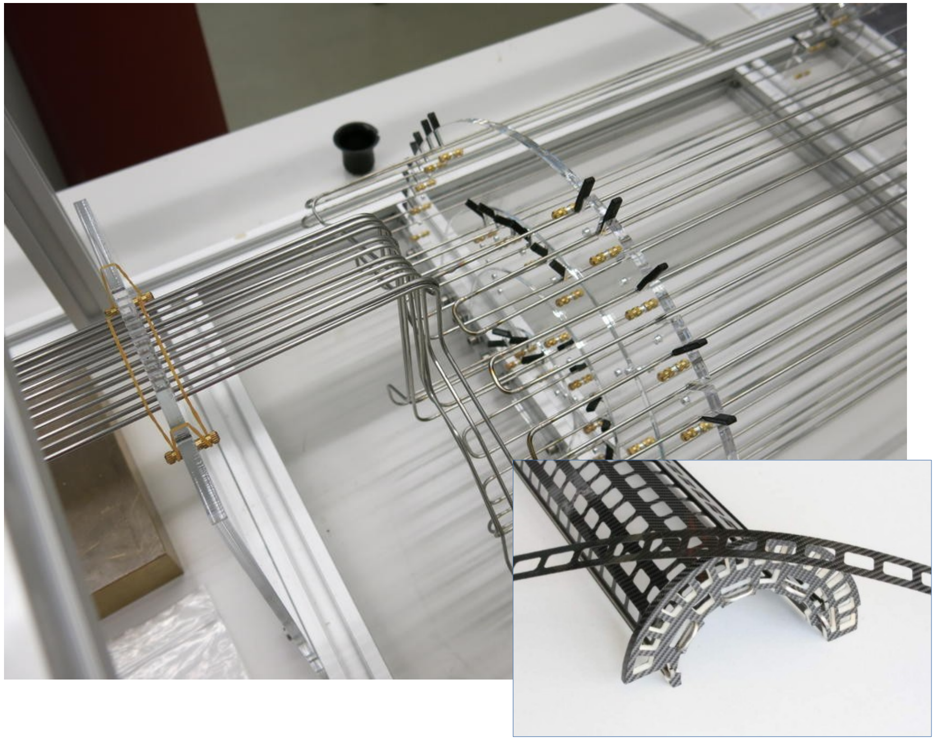
A → B: increase CO2 pressure for transfer to the experiment
B → C: increase temperature due to heat exchange with returning CO2
C → D: reduce pressure inside the detector to reach on-set of evaporation
D → E: absorb heat from the detector
E → F: condensate CO2 fluid/vapor mixture using incoming (colder) CO2 pipe
F → A: cool down CO2 with main chiller

- D → G : low impedance system = almost constant pressure from the inlet to the detector up to the accumulator in the cooling plant
- pressure in accumulator (G) steers temperature inside the detector

in theory

CO$_2$ Cooling – Specifications





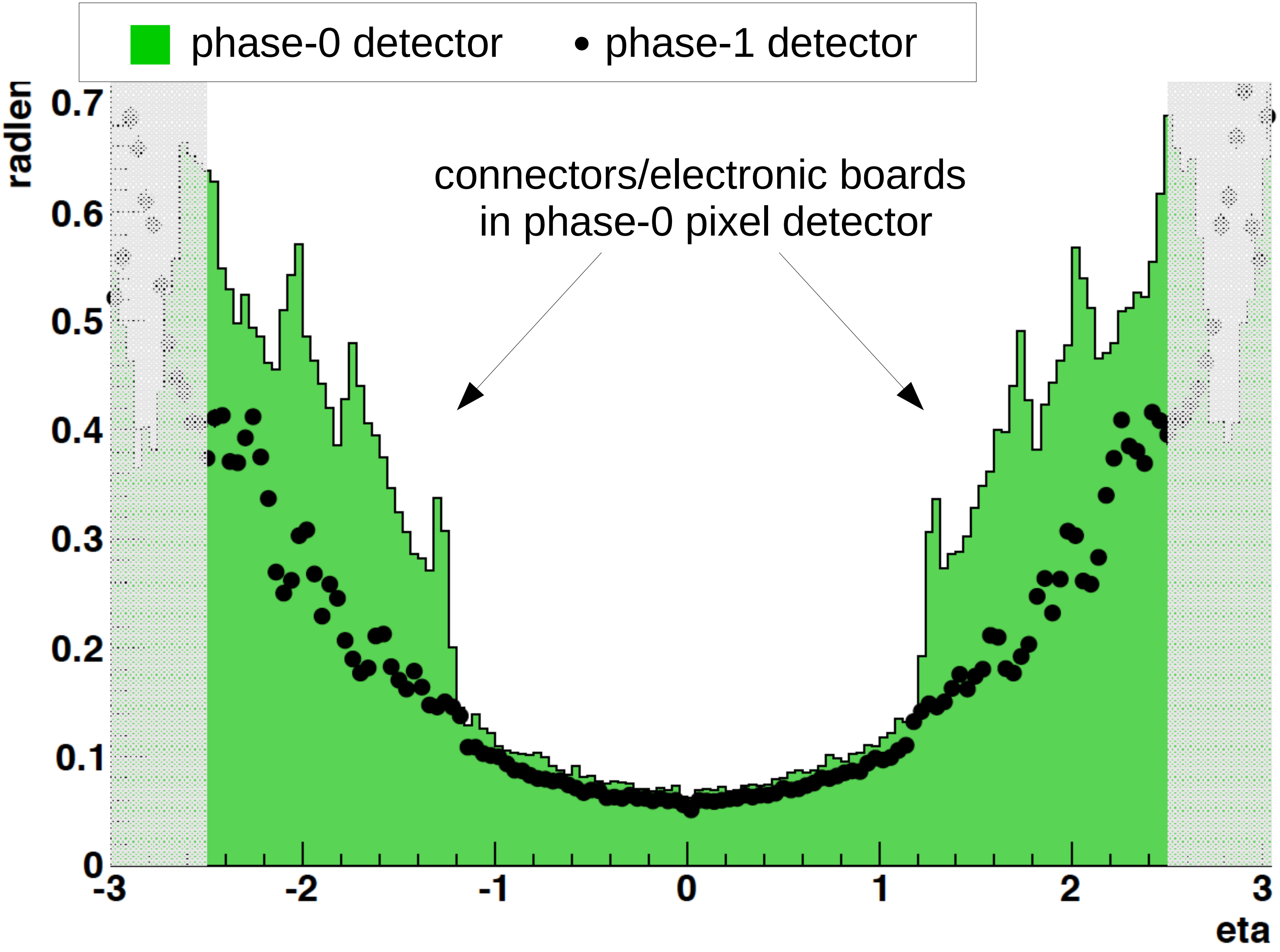
CO2 cooling plants

- 2 identical cooling plants (BPix, FPix)
- redundant system
- cooling power per plant: 15kW
- location: in CMS service cavern (accessible)
- operational range:
  16°C (60bar) → -22°C (20bar)
- lower temperature possible, but not commissioned

inside the detector

- → carbon fiber structure for efficient heat exchange
- → stainless steel cooling loops
  - → diameter 1.7mm
  - → wall thickness 50µm
- → **very lightweight detector design possible!**

Material Budget

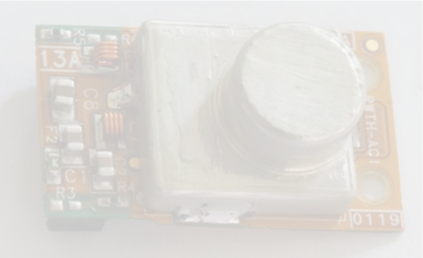


connectors/electronic boards in phase-0 pixel detector

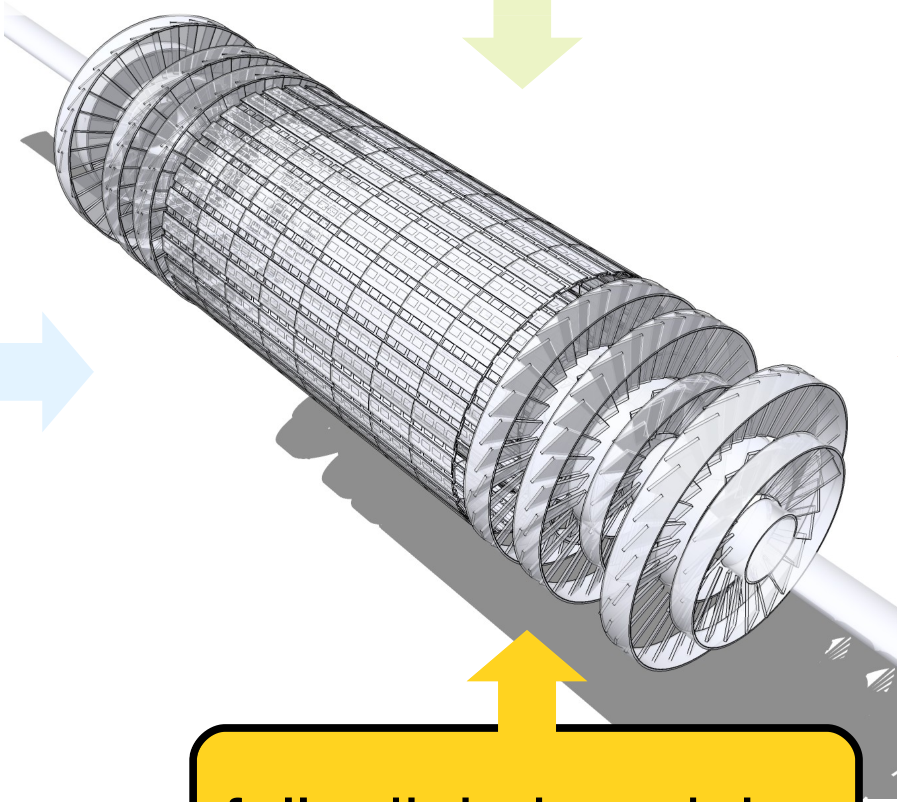
- electronic boards/connectors moved to higher η
- 2-phase CO_2 cooling
- lightweight mechanical support structures

despite additional tracking layer:
material further reduced

CMS Phase-1 Pixel Detector – Key Technologies



DC-DC powering



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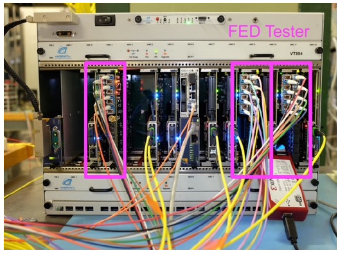
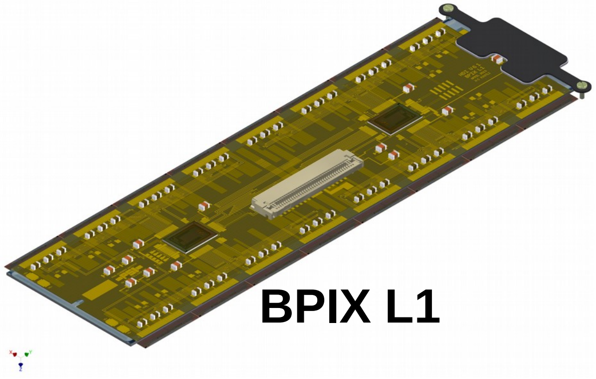
μTCA DAQ

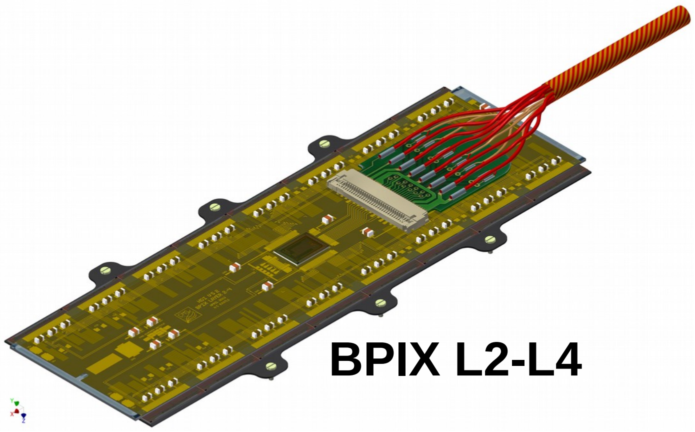


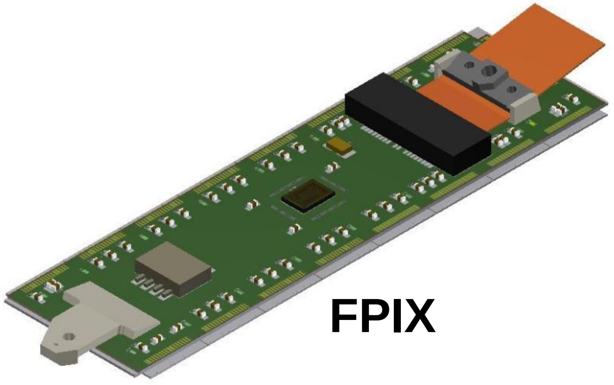
fully digital modules

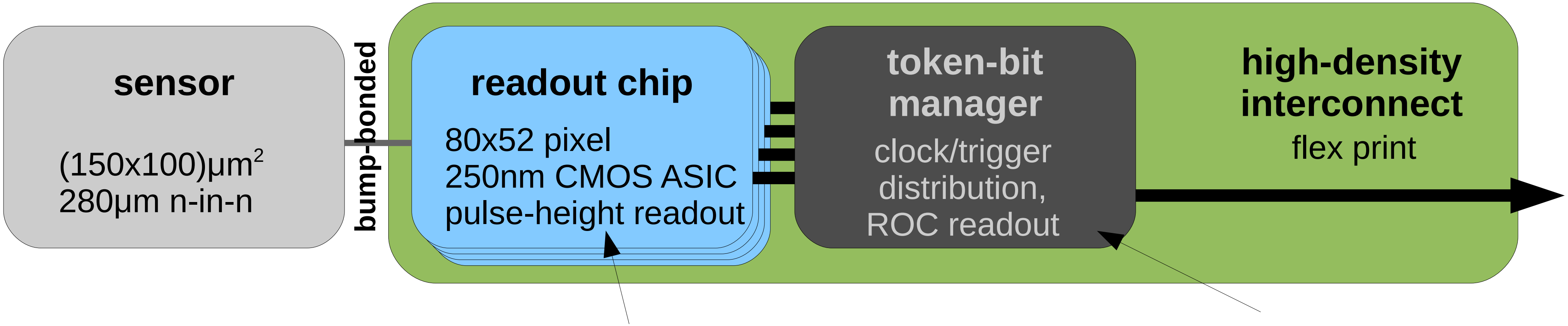
The Phase-1 Pixel Detector contains many key technologies used in the LHC phase-2 upgrade

Signal Path – Digital Modules


BPIX L1


BPIX L2-L4


FPIX



sensor

$(150 \times 100) \mu m^2$
280µm n-in-n

bump-bonded

readout chip

80x52 pixel
250nm CMOS ASIC
pulse-height readout

token-bit manager

clock/trigger distribution,
ROC readout

high-density interconnect

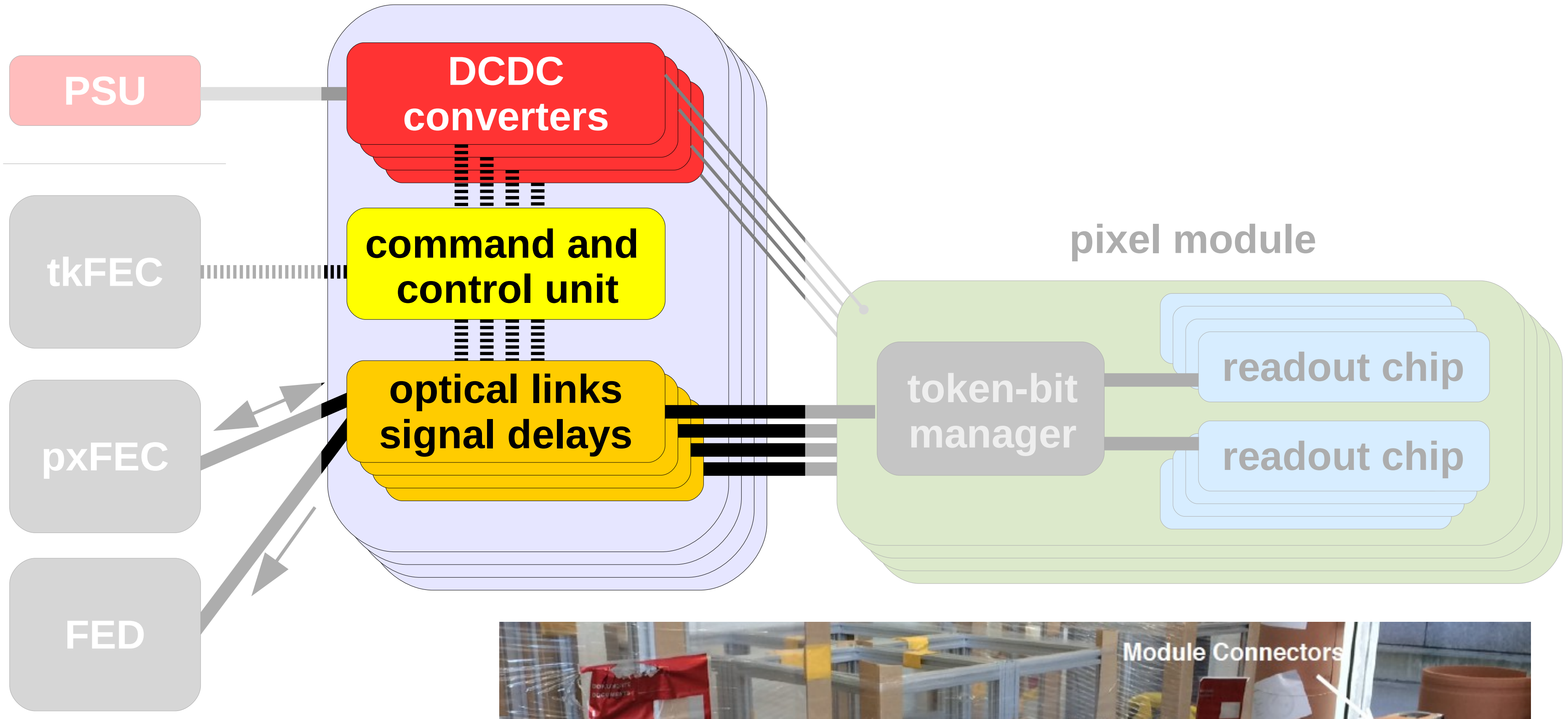
flex print

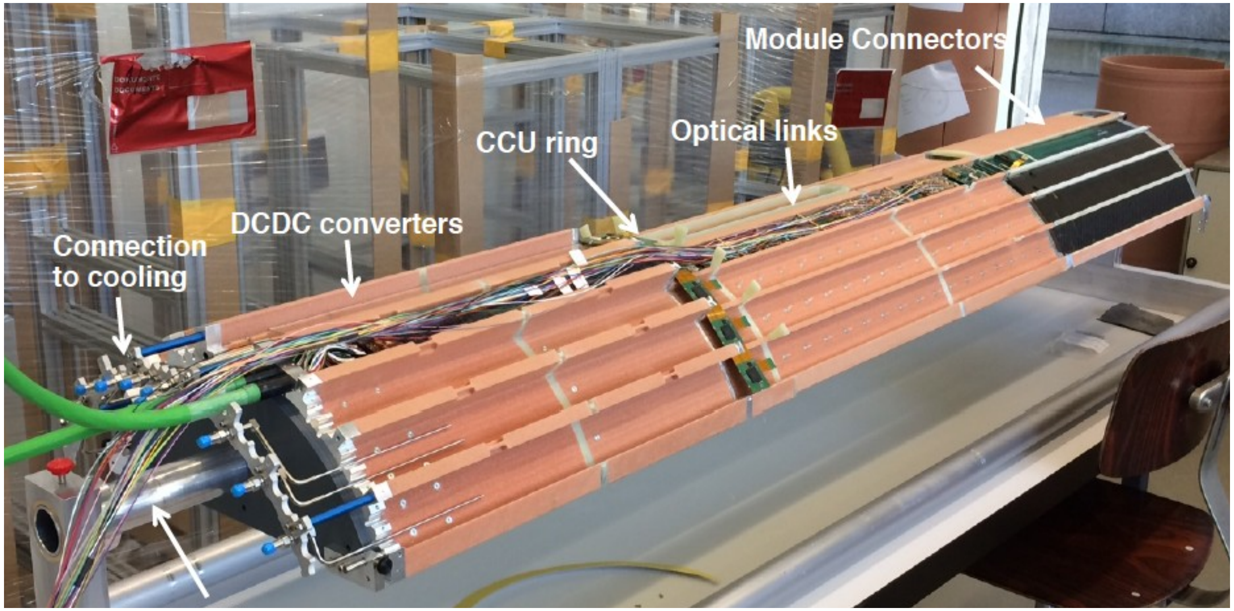
- **ROC** with **digital RO** based on psi46
- same architecture (“column drain“)
- on-chip digitization (8bit ADCs)
- increased buffers (hit, timestamp)
- improved charge threshold (reduced by factor ~1.5)
- ***special layer-1 ROC (“dynamic cluster drain”), PROC600 which is capable to cope with 600MHz/cm²***

- **digital TBM**
- 160Mbit/s digital
- module out-bound data stream: 400Mbit/s

all components capable to deal with high integrated & instantaneous luminosities

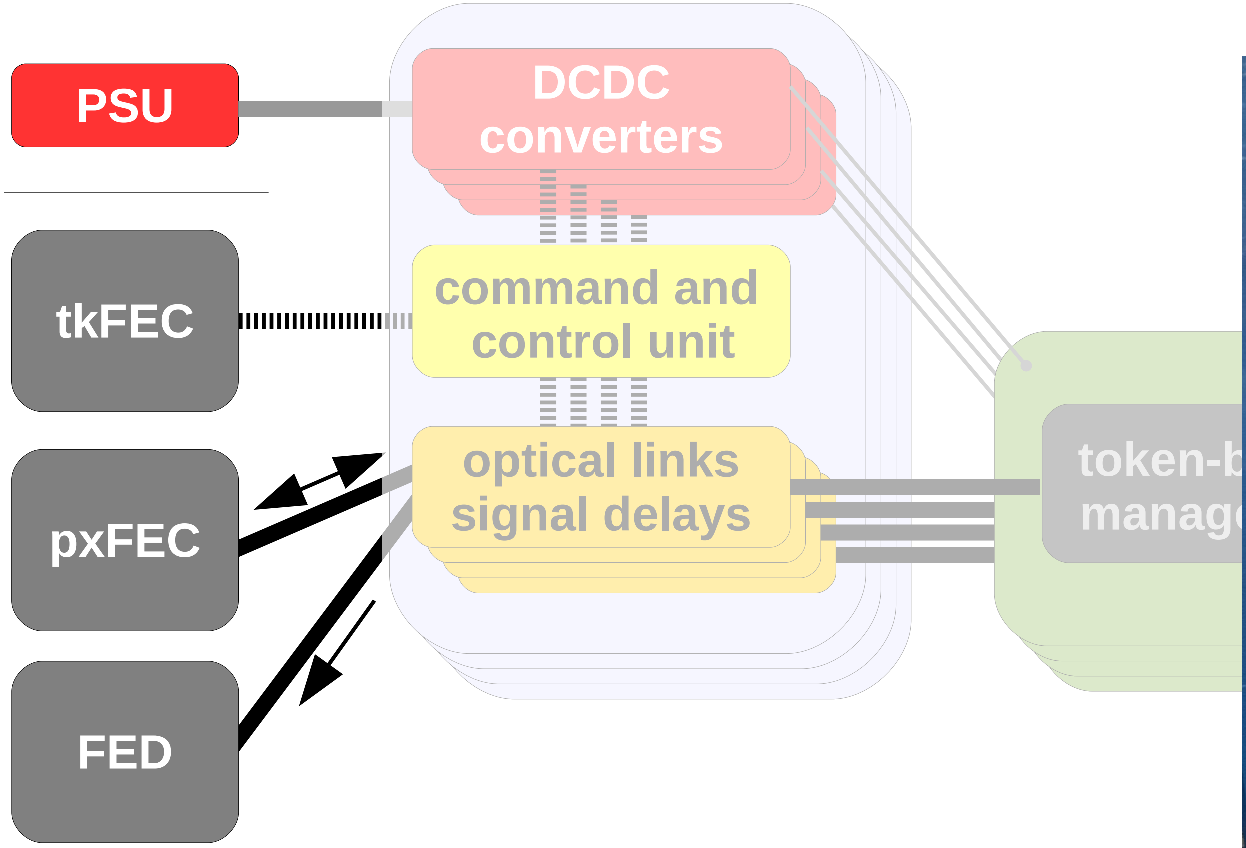
Signal Path – Service Cylinder

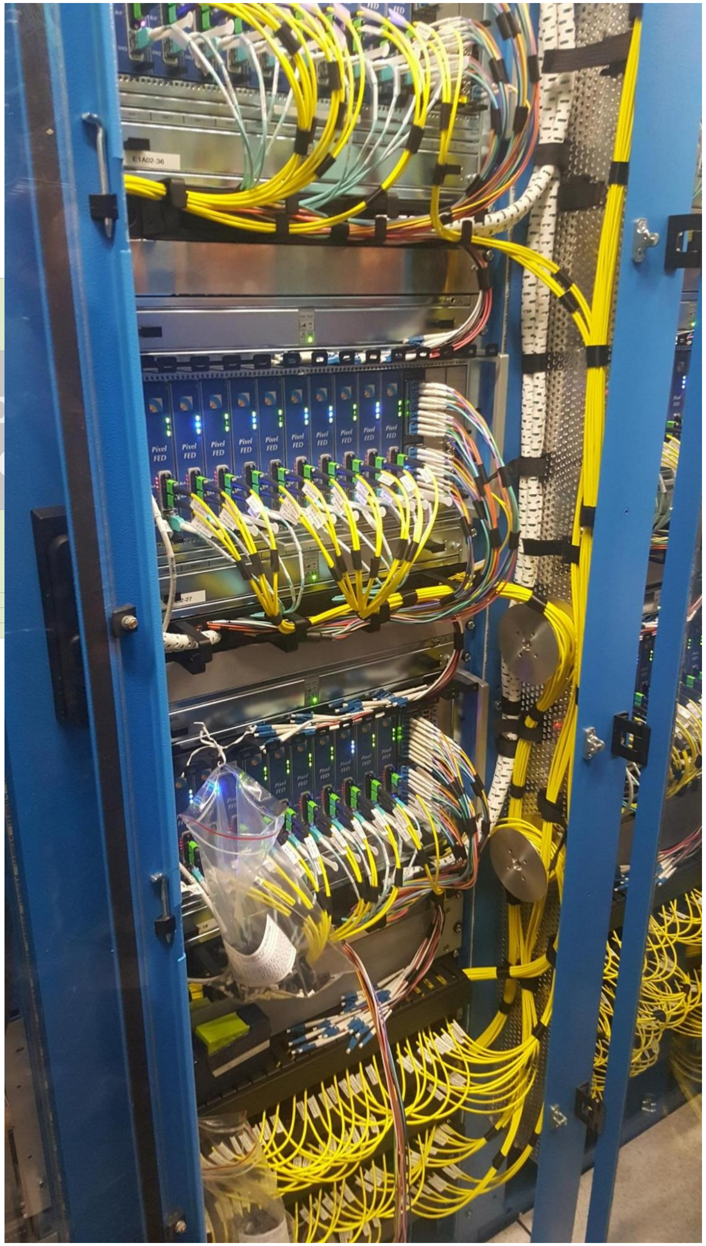




service electronics integrated in long channels outside the tracking volume (high-η region; η>2.5)

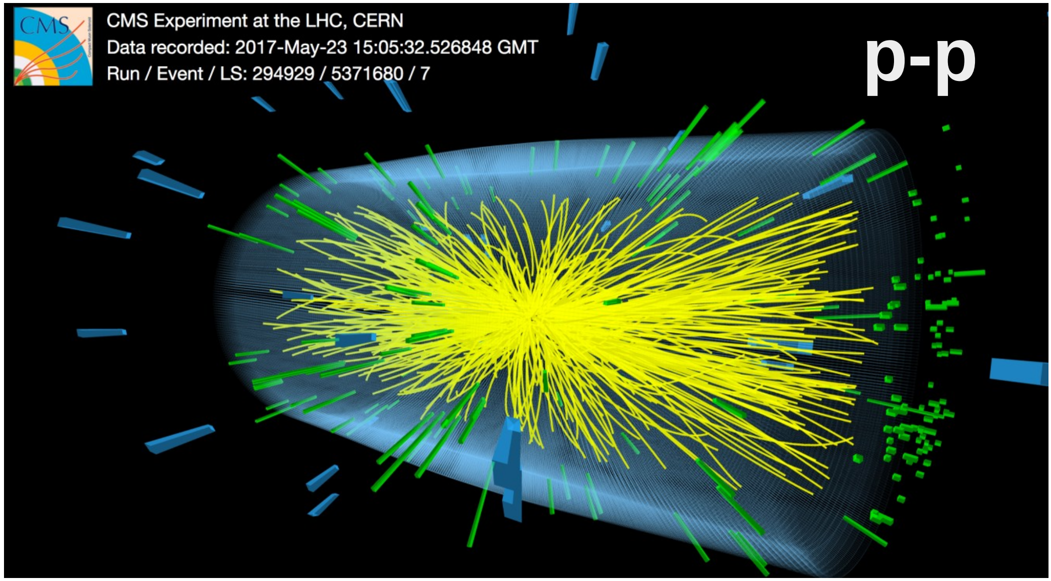
Signal Path – µTCA Backend Electronics

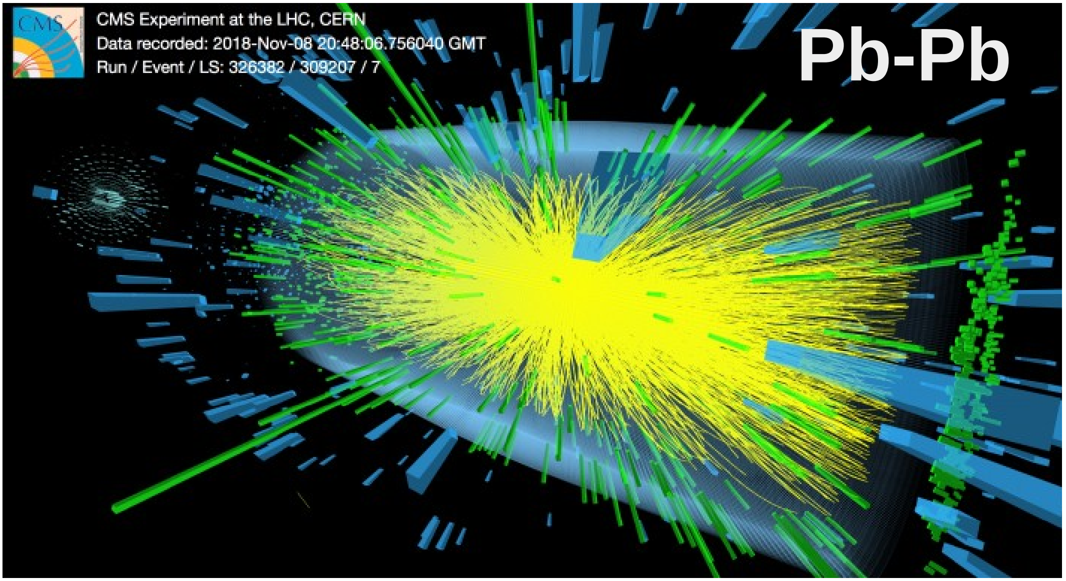




- replacement of VME **front-end boards**
  - 108 **FrontEndDrivers** (FED) → detector readout
  - 16+3 **FrontEndController** (FEC) → detector control
- new CMS-wide crate standard: **µTCA**
  - all based on **generic AMC card** (FC7) built around Kintech 7 FPGA and 4GB DDR3 RAM
  - different **flavors** realized with **FPGA mezzanine cards/ firmware**
- capable to drive/receive links of **up to 10Gb/s**

Operational Experience

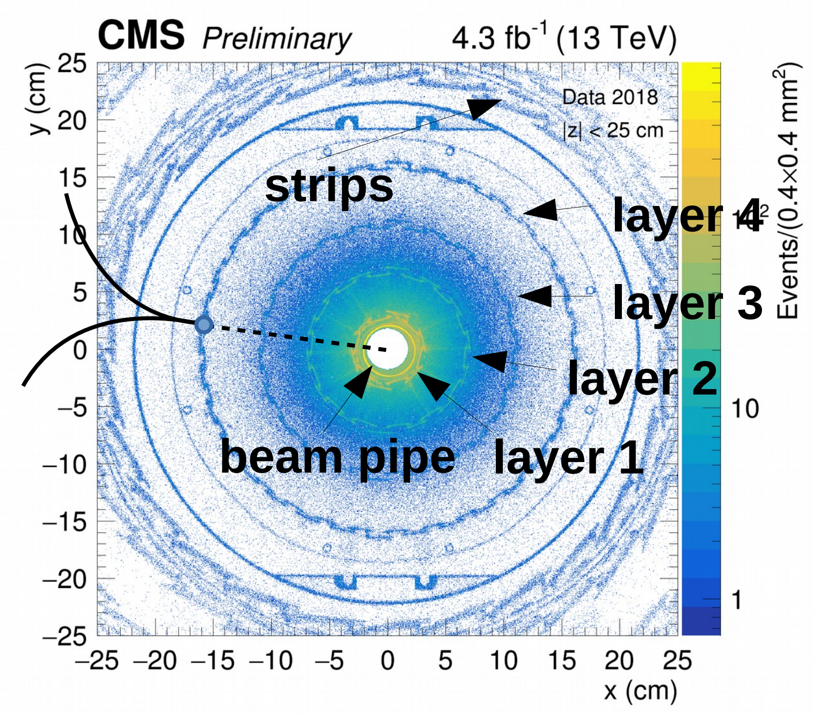




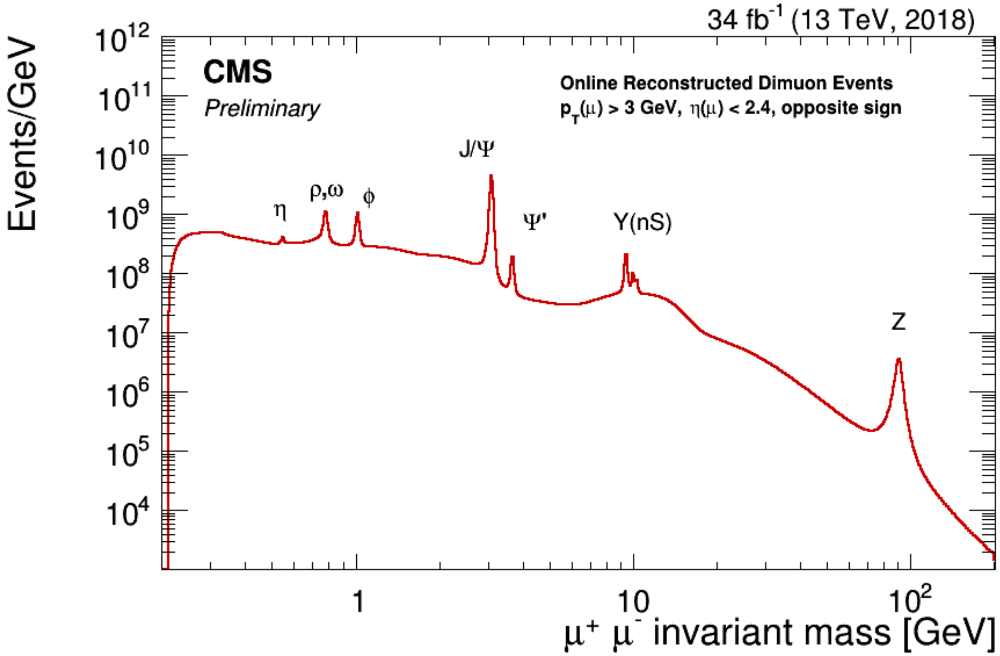
Disclaimer

- I will be **very open on problems** we encountered during the last two years
- BUT: don't get the wrong impression that the detector did not work
- the physics performance was always excellent not at last thanks to an hard-working, fantastic operation team!

vertices from nuclear interaction



di-muon mass on HLT trigger level



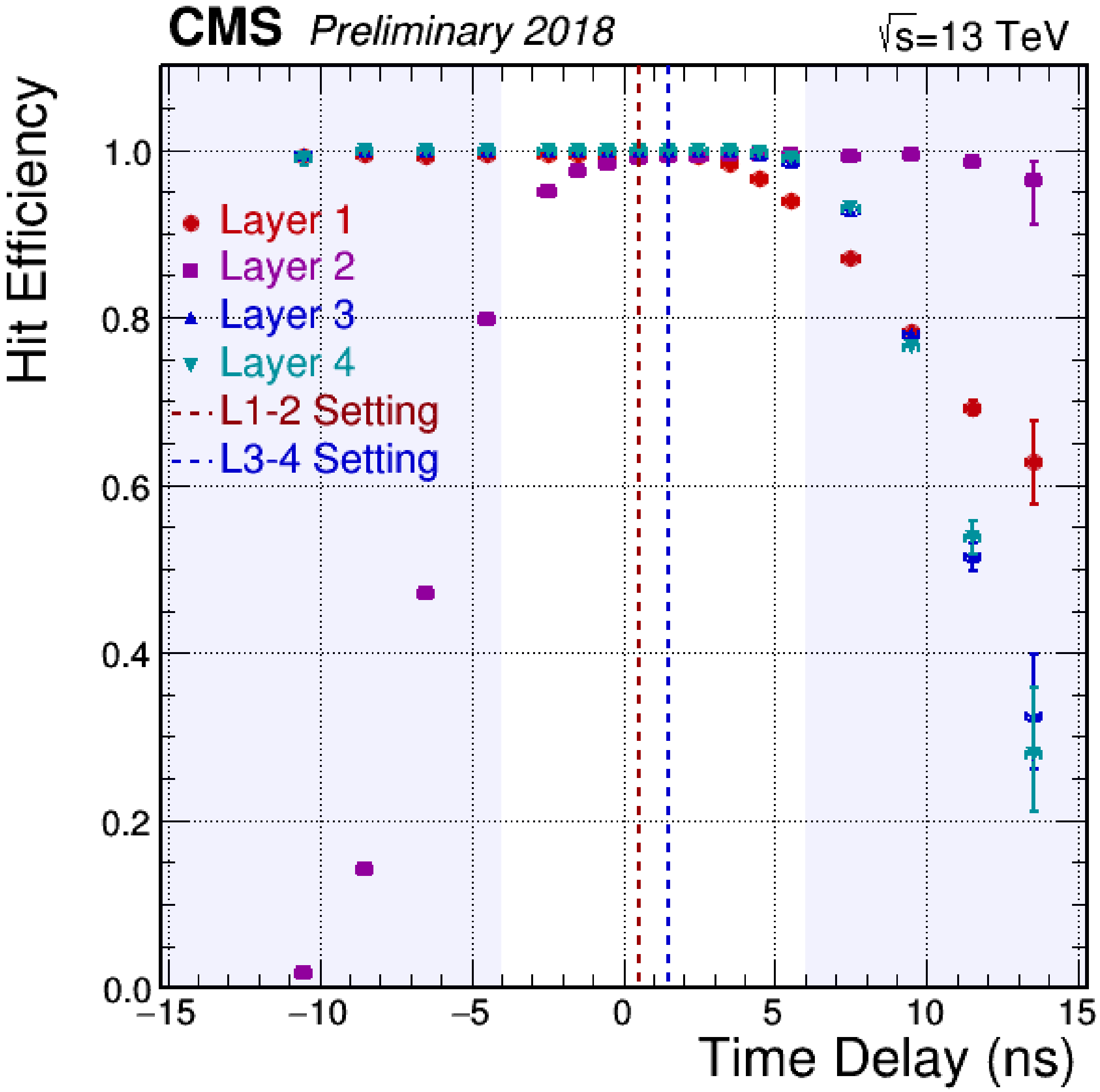
Timing between Layers

timing between layers

- read-out chip in layer 1 (PROC600) half a clock cycle (12.5ns) faster than the ROCs in layer 2-4 and FPix (psi46dig)
- shared clock/trigger distribution in layer 1/ layer 2 per φ-sector
- read-out of layer 2 too early, layer 1 too late
- very small overlap of efficiency plateau

plans for the future

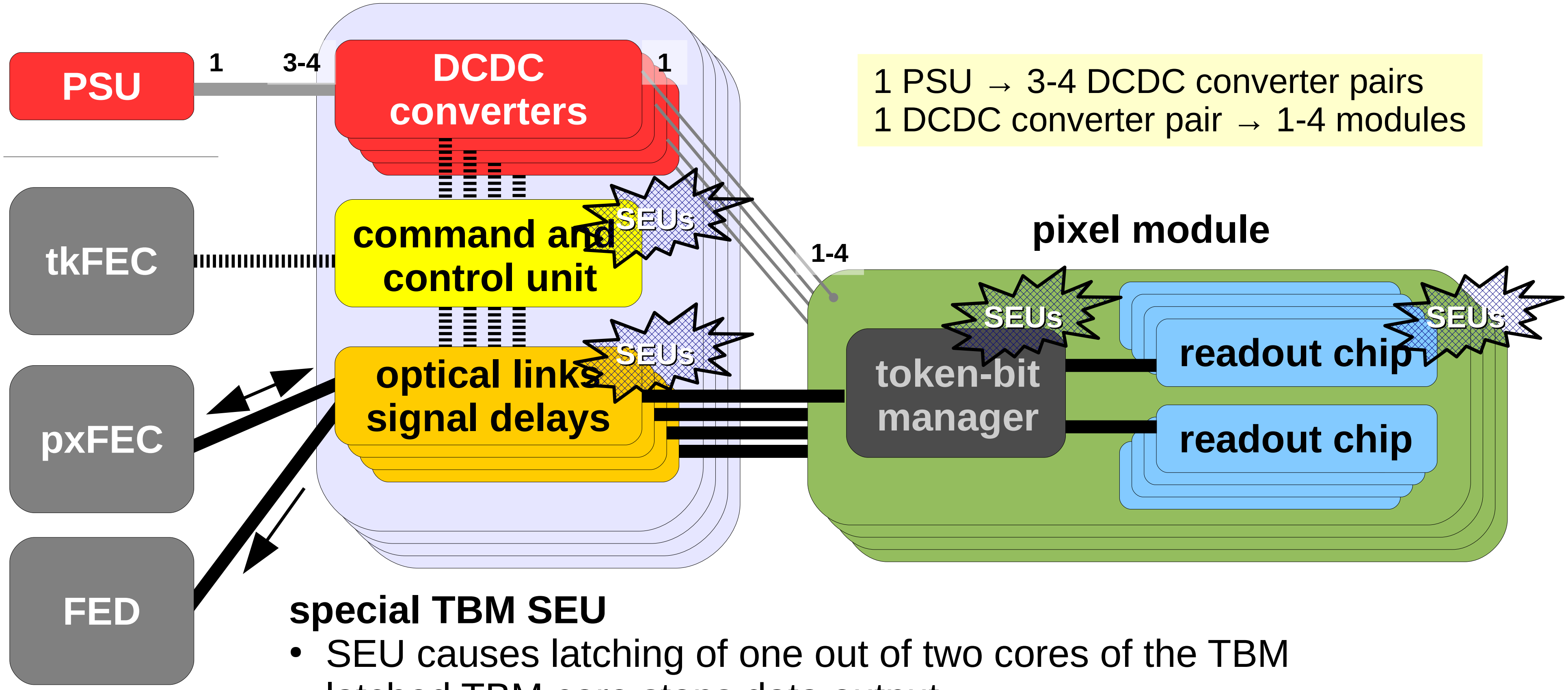
- current solution seems to work, though is not comfortable to operate so close to the efficiency edge
- TBM for layer 1 replacement includes adjustable delay (on the module level)



Single Event Upsets

status in 2017/2018

- single event upset expected in high radiation environment
- SEUs observed in many components in 2017/2018
- normal procedure: download configuration parameters to the front-end regularly



1 PSU → 3-4 DCDC converter pairs
1 DCDC converter pair → 1-4 modules

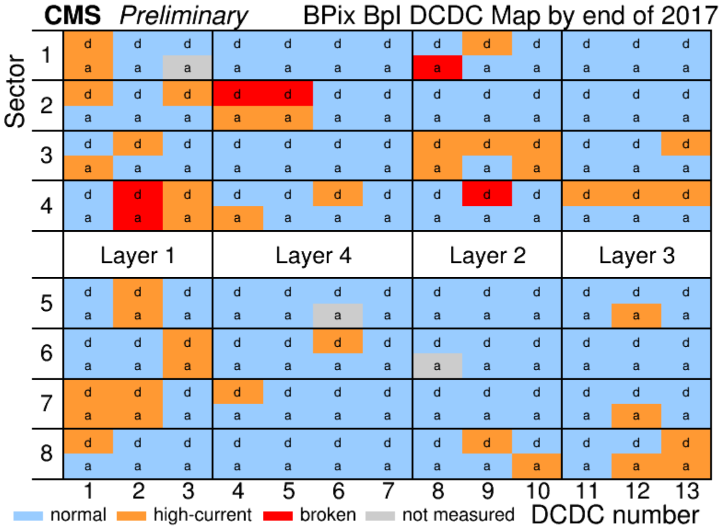
special TBM SEU

- SEU causes latching of one out of two cores of the TBM
- latched TBM core stops data output
- reprogramming the TBM does **not** resolve the problem
- only powercycle recovers the TBM core and thus the ROCs behind
- in 2017: command and control unit used to disable/enable DCDC converter

The DCDC Story

timeline

- October 5th 2017: first DCDC converter stopped working
- extrapolation of failure rate to 2018: no sufficient tracking by mid 2018
- extraction of the detector during YETS 2017/2018
- replacement of **all** converters with similar version, but bigger fuse (allowing to operate the converters at a lower input voltage)
- early 2018: reinstalled the detector without managing to break a single converter outside CMS(!)



CMS *Preliminary* BPix BpI DCDC Map by end of 2017

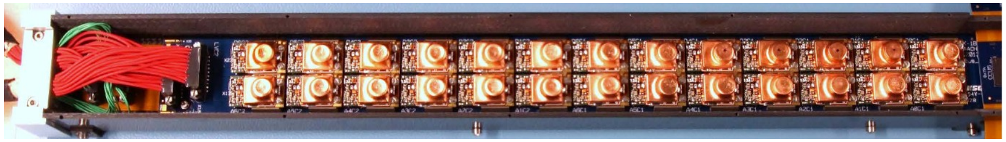
Sector		1	2	3	4	5	6	7	8	9	10	11	12	13
1		🟧 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d	🟧 d	🟦 d	🟦 d	🟦 d	🟦 d
		🟧 a	🟦 a	⬜ a	🟦 a	🟦 a	🟦 a	🟦 a	🟥 a	🟦 a	🟦 a	🟦 a	🟦 a	🟦 a
2		🟧 d	🟦 d	🟧 d	🟥 d	🟥 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d
		🟦 a	🟦 a	🟦 a	🟧 a	🟧 a	🟦 a	🟦 a	🟦 a	🟦 a	🟦 a	🟦 a	🟦 a	🟦 a
3		🟦 d	🟧 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d	🟧 d	🟧 d	🟧 d	🟦 d	🟦 d	🟧 d
		🟧 a	🟦 a	🟦 a	🟦 a	🟦 a	🟦 a	🟦 a	🟧 a	🟦 a	🟧 a	🟦 a	🟦 a	🟦 a
4		🟦 d	🟥 d	🟧 d	🟦 d	🟦 d	🟧 d	🟦 d	🟦 d	🟥 d	🟦 d	🟧 d	🟧 d	🟧 d
		🟦 a	🟥 a	🟧 a	🟧 a	🟦 a	🟦 a	🟦 a	🟦 a	🟦 a	🟦 a	🟦 a	🟦 a	🟦 a
		Layer 1			Layer 4				Layer 2			Layer 3		
5		🟦 d	🟧 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d
		🟦 a	🟧 a	🟦 a	🟦 a	🟦 a	⬜ a	🟦 a	🟦 a	🟦 a	🟦 a	🟦 a	🟧 a	🟦 a
6		🟦 d	🟦 d	🟧 d	🟦 d	🟦 d	🟧 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d
		🟦 a	🟦 a	🟧 a	🟦 a	🟦 a	🟦 a	🟦 a	⬜ a	🟦 a	🟦 a	🟦 a	🟦 a	🟦 a
7		🟧 d	🟧 d	🟦 d	🟧 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d
		🟧 a	🟧 a	🟦 a	🟦 a	🟦 a	🟦 a	🟦 a	🟦 a	🟦 a	🟦 a	🟦 a	🟧 a	🟦 a
8		🟧 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d	🟦 d	🟧 d	🟦 d	🟦 d	🟦 d	🟧 d
		🟦 a	🟦 a	🟦 a	🟦 a	🟦 a	🟦 a	🟦 a	🟦 a	🟦 a	🟧 a	🟦 a	🟧 a	🟧 a

DCDC number

🟦 normal 🟧 high-current 🟥 broken ⬜ not measured

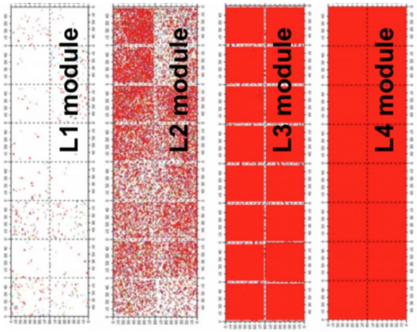
characterization of extracted converters

- ➔ I-V characterization of all extracted converters:
  - 65 not switching anymore
  - 333 higher currents in disabled state
  - rest (~800) behaves normally



damage on modules

- sensor leakage currents cannot be drained efficiently if ROC is not powered
- damage on the pre-amplifier if HV on/ LV off
- damage proportional to time and sensor leakage current
- 6 (accessible) out of 8 damaged modules in L1 replaced



The DCDC Story

after months of investigation

- chip designers of the FEAST chip found a way to reproduce the breaking symptoms
- once a feedback loop was established, breaking mechanism could be identified quickly

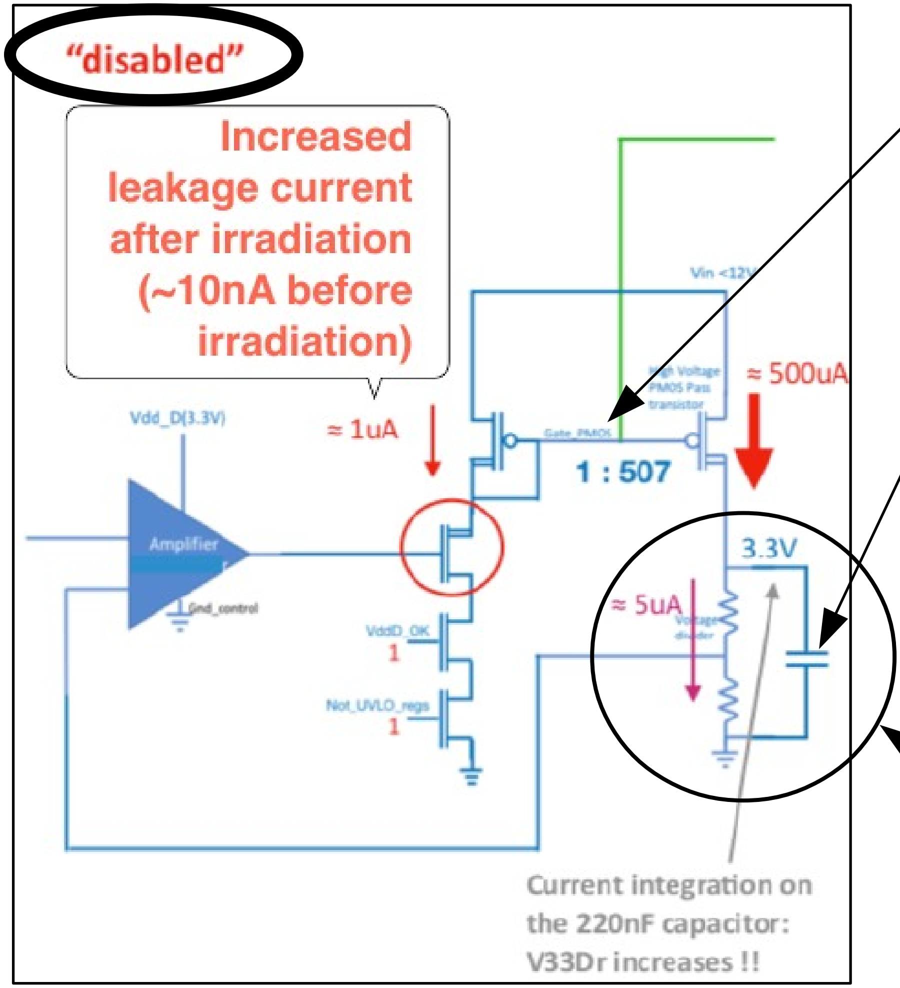


figure by Federico Faccio

amplifying current mirror

capacitor charging up in the disabled state causing voltage spikes well beyond 3.3V

part providing current to the drivers of the power transistors

two possible results

- high leakage current forms new ohmic path to ground (→ high current)
- converter breaks irreversibly (→ broken)

consequences for operation

- lower input voltage helps
- stop disabling the output
- what about latched TBM cores? → enable/disable output of the power supply (not DCDC)

no DCDC converter broke in 2018!

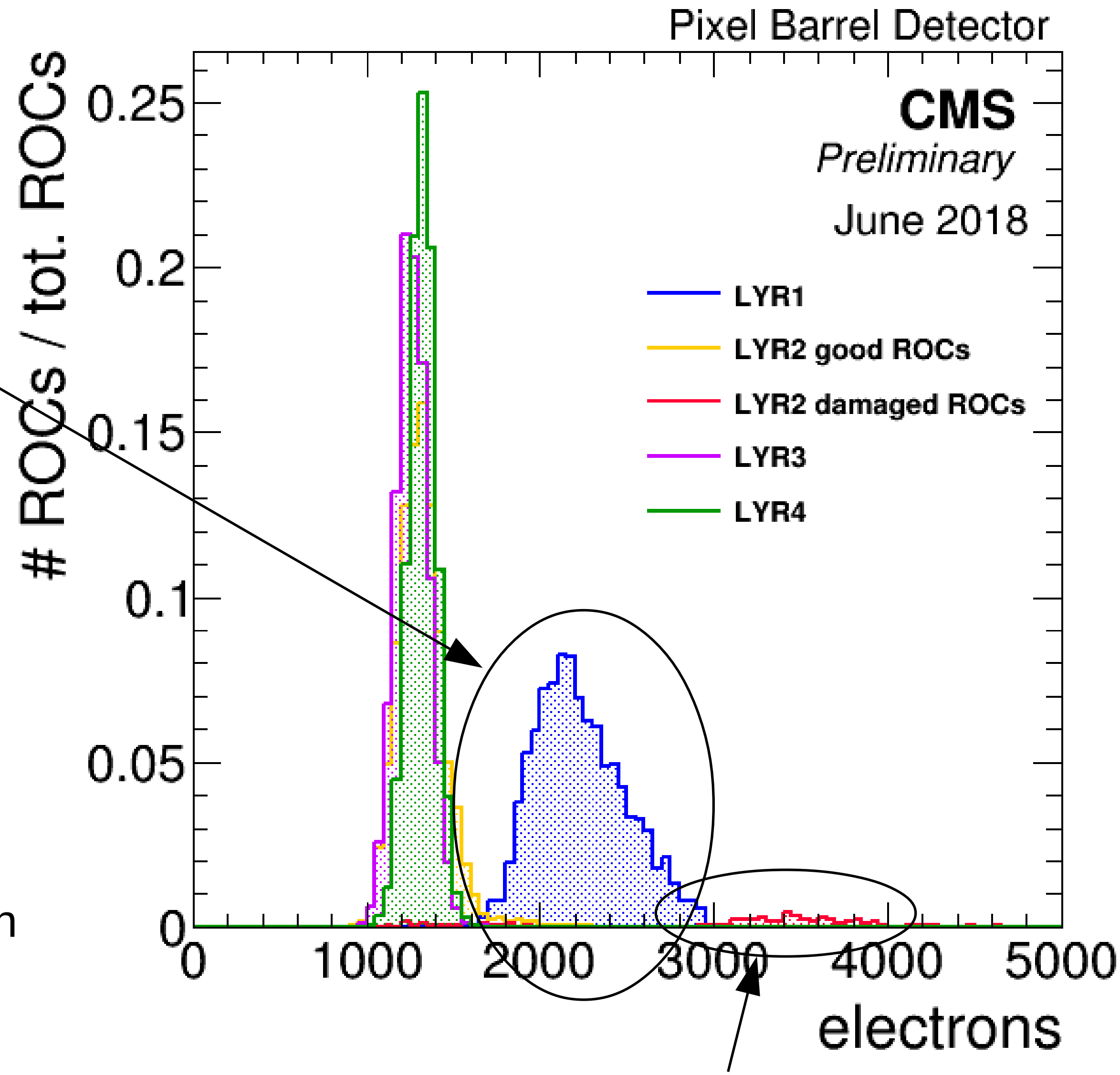
Layer-1 readout chip crosstalk

crosstalk issue

- large crosstalk has been observed
  - ➔ extra hits appear correlated with real hits
  - ➔ effect is highly rate dependent
- higher thresholds needed in order to operate the chip efficiently
- two main sources of the problem identified recently
  - dominant contribution can be mitigated by optimized programming sequence
  - better shielding in the ROC design will further improve the situation

plans for the future

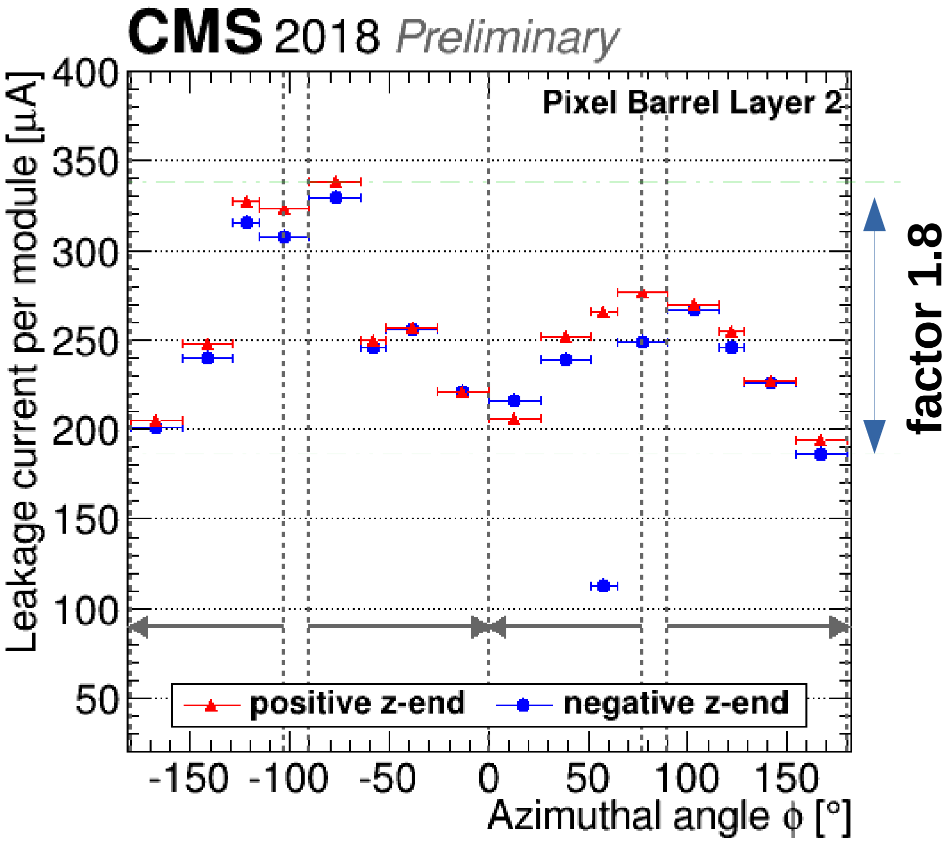
- crosstalk problem will be addressed in the next version of the read-out chip
- problem will be gone after LS2



pre-amplifier damage in 2017 during DCDC crisis

Leakage Currents

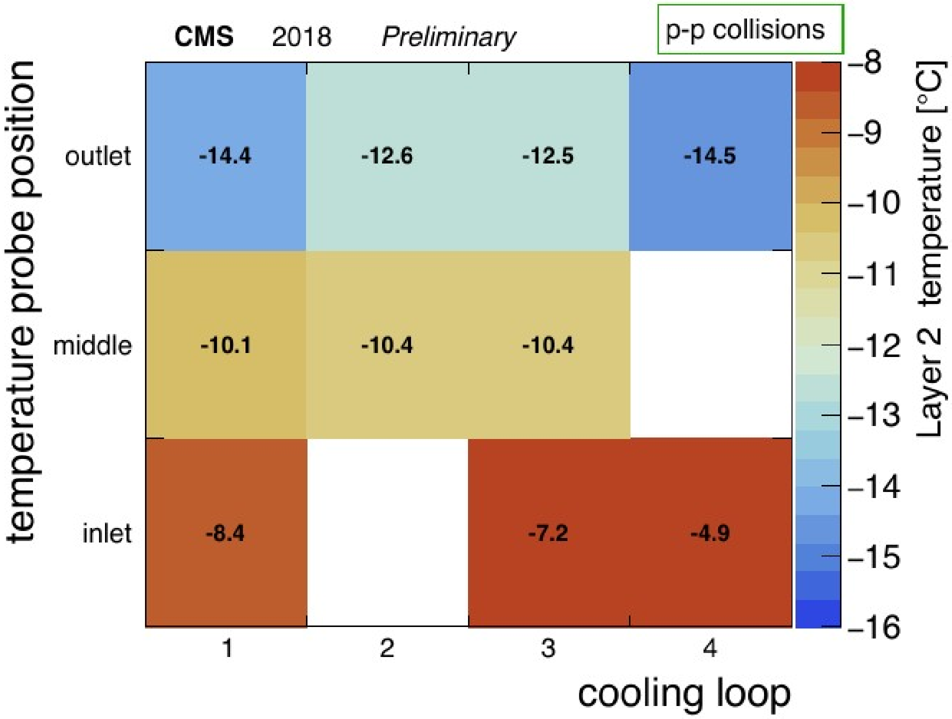
observation: strongly varying leakage currents within the same layer



hypothesis: inhomogeneous cooling?

challenges:

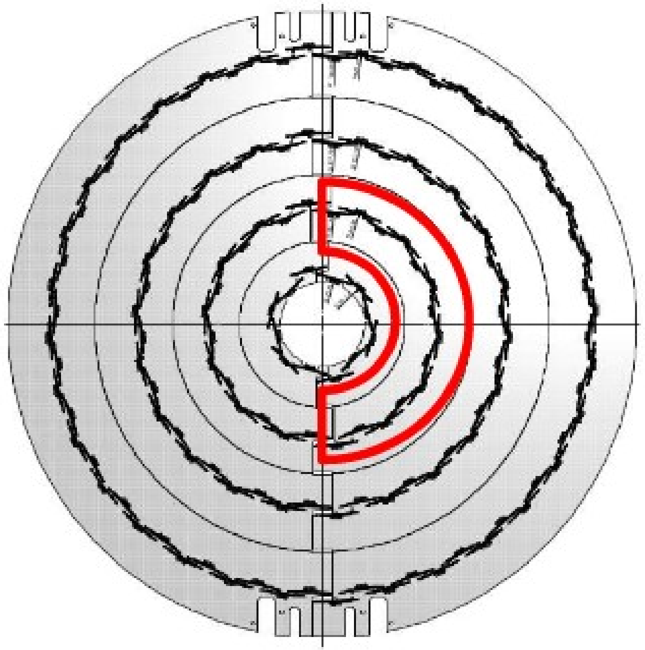
- measured leakage currents always sum of 4 or 8 modules in layer 2
- only 2-3 temperature probes along a cooling pipe (covering Δφ=90°)
- position of the probes not known precisely

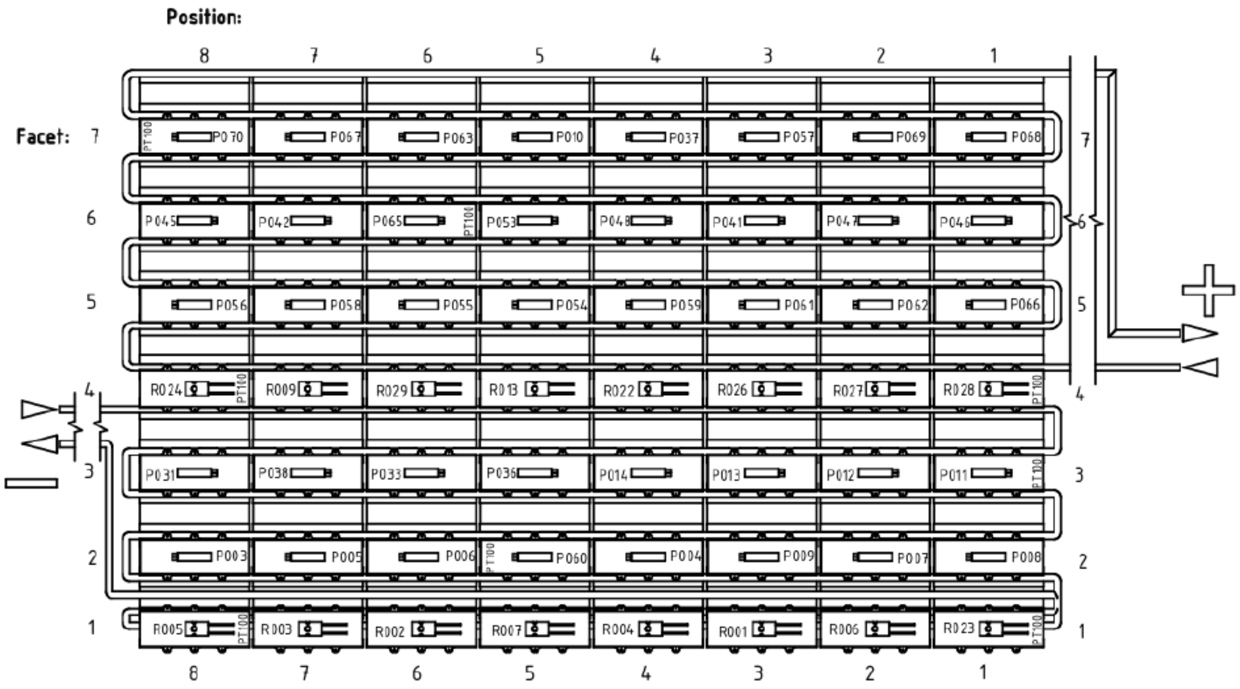


thermal mock-up fully instrumented with temperature probes ideal tool to characterize the cooling performance!

Thermal Characterization

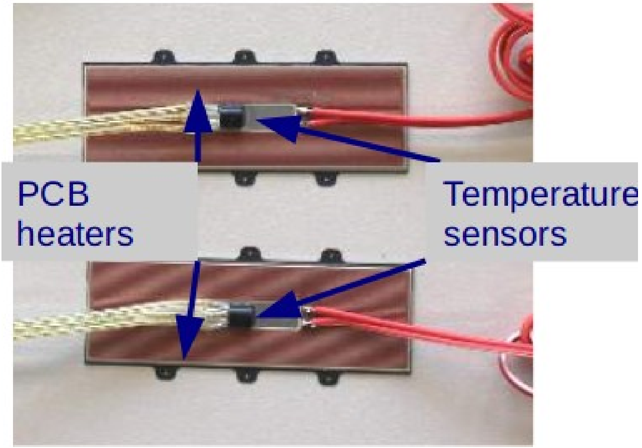
1:1 rebuild of layer 2 half-shell with heater modules



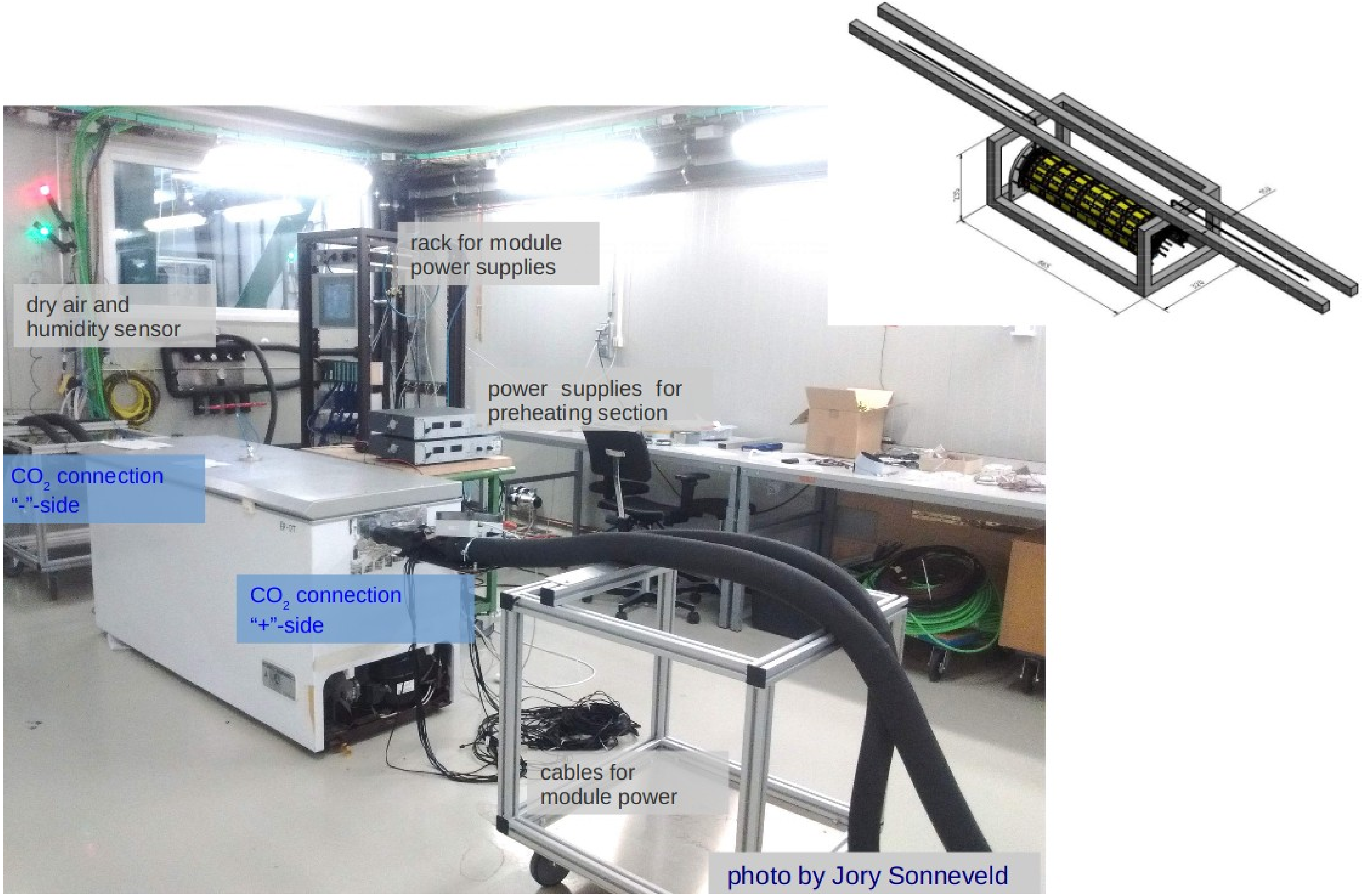


Facet: \ Position:	8	7	6	5	4	3	2	1
7	P070	P067	P063	P010	P037	P057	P069	P068
6	P045	P042	P065	P053	P048	P041	P047	P046
5	P056	P058	P055	P054	P059	P061	P062	P066
4	R024	R009	R029	R013	R022	R026	R027	R028
3	P031	P038	P033	P036	P014	P013	P012	P011
2	P003	P005	P006	P060	P004	P009	P007	P008
1	R005	R003	R002	R007	R004	R001	R006	R023

- adjustable heat load for groups of modules
- temperature sensor on top of each module
- adjustable preheating on a section of the CO2 pipe in front of the mock-up
- PLC and arduino based readout



Thermal Characterization



rack for module power supplies

dry air and humidity sensor

power supplies for preheating section

CO_2 connection "-"-side

CO_2 connection "+"-side

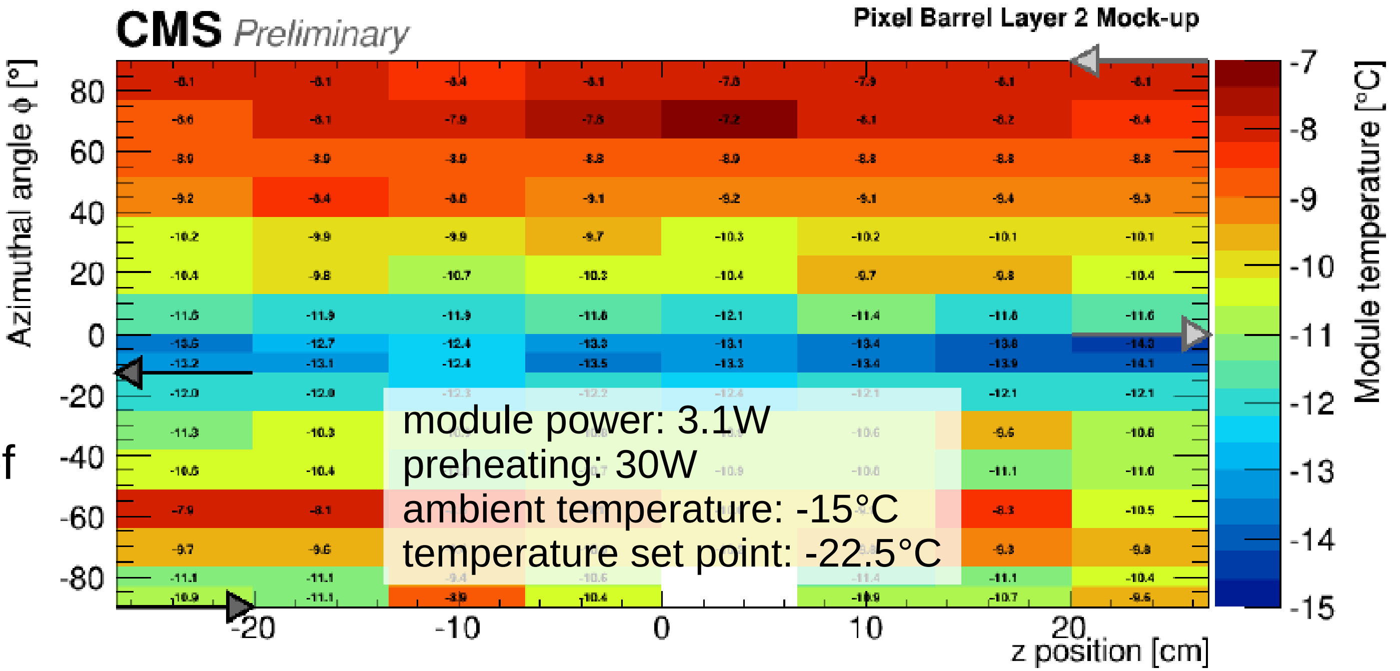
cables for module power

photo by Jory Sonneveld

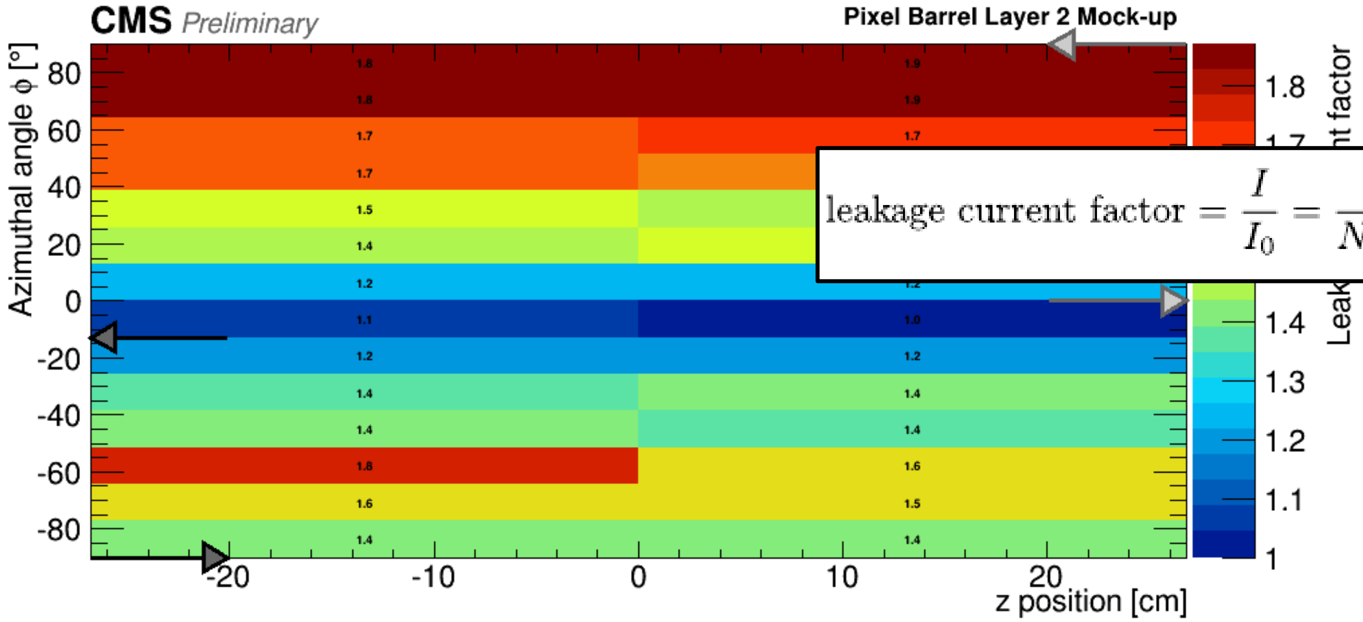
Thermal Characterization

- temperature variation: -15°C → -7°C
- cooler at the outlet
- expected behavior of CO2 cooling

prediction of relative factor of leakage currents based on detailed measurement in thermal mock-up



module power: 3.1W
preheating: 30W
ambient temperature: -15°C
temperature set point: -22.5°C

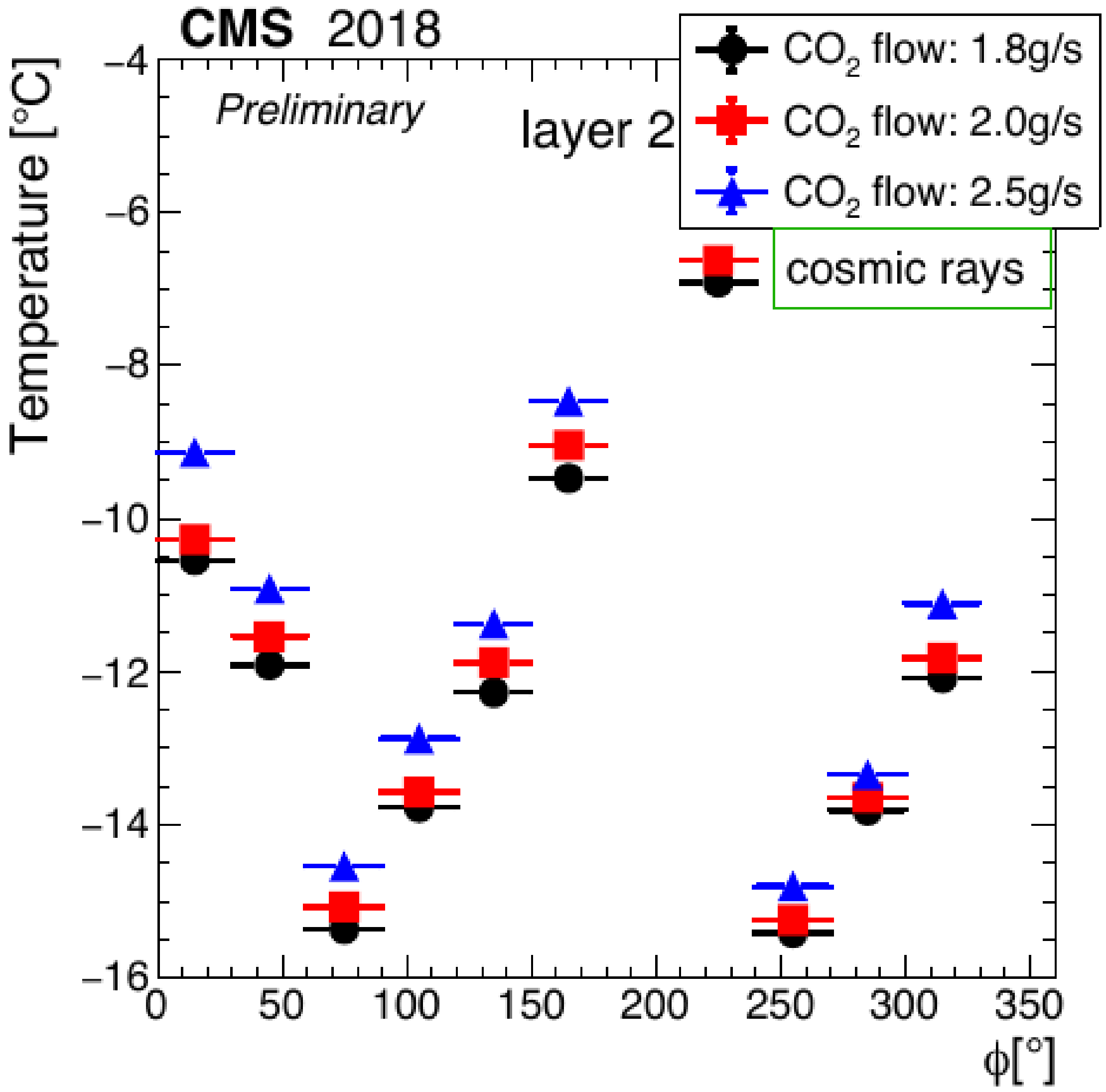


$$\text{leakage current factor} = \frac{I}{I_0} = \frac{1}{N_{\text{modules}}} \sum_i \frac{T_i^2}{T_0^2} \exp\left[-\frac{\Delta E}{2\,k_B} \left(\frac{1}{T_i} - \frac{1}{T_0} \right) \right]$$

factor 1.8 observed in detector consistent hypothesis temperature effect

Experience with CO2 Cooling

- large temperature gradient observed
- not expected, but reproduced with thermal mock-up
- very stable and reliable operation during 2017 and 2018
- adjusted (reduced) the flow over the last two years three times to optimize the cooling performance
- thermal mock-up of a part of a layer as an inevitable tool in understanding the (counter-intuitive) characteristics of the cooling

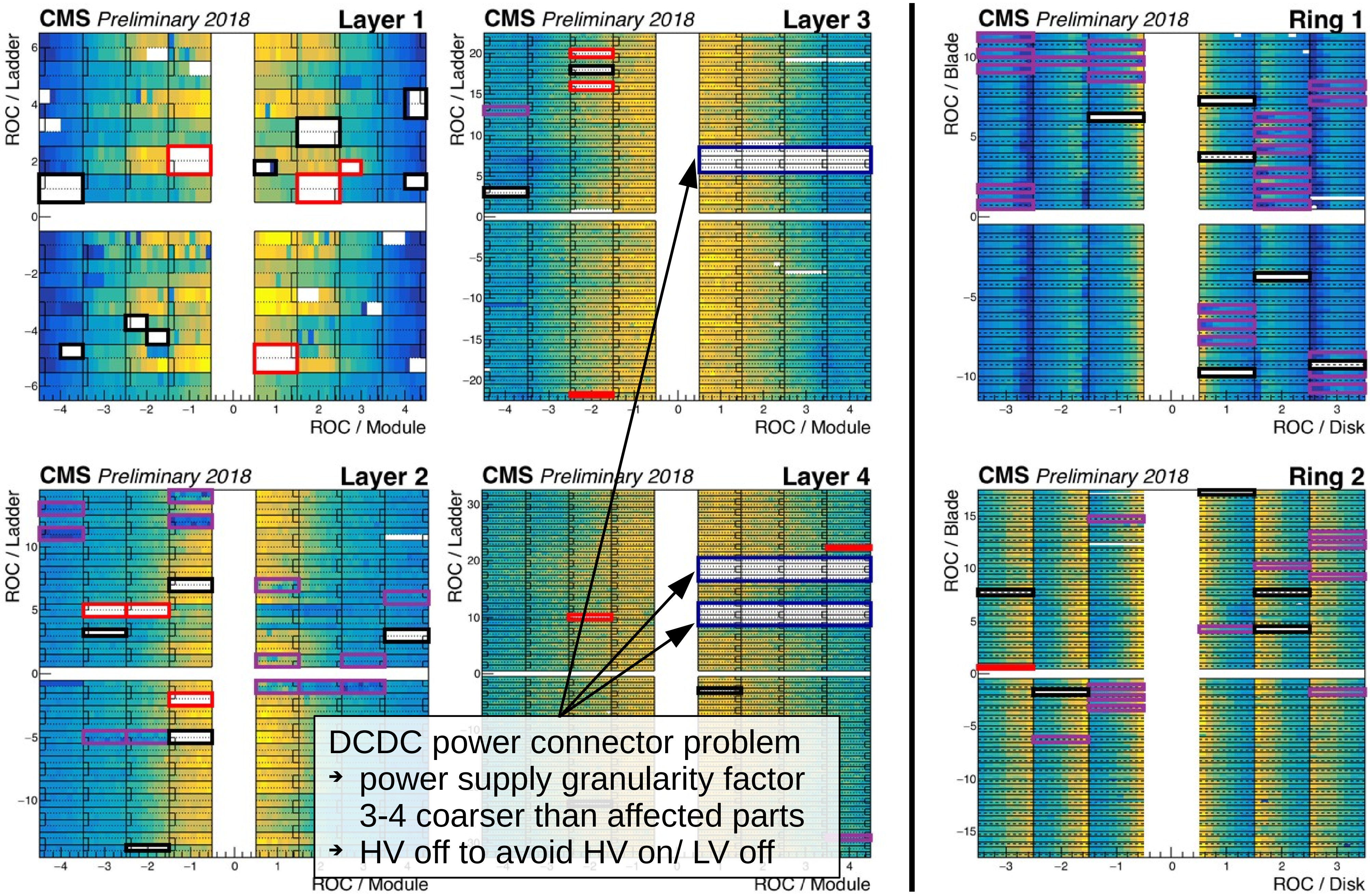


important lessons learned:

- 2-phase CO2 is a very efficient coolant, but it is not easy to warm up the detector if there is no heat dissipation from active components
- annealing? safety?
- heating wires should be considered for each CO2 cooled system

Detector Performance
and
Radiation Effects

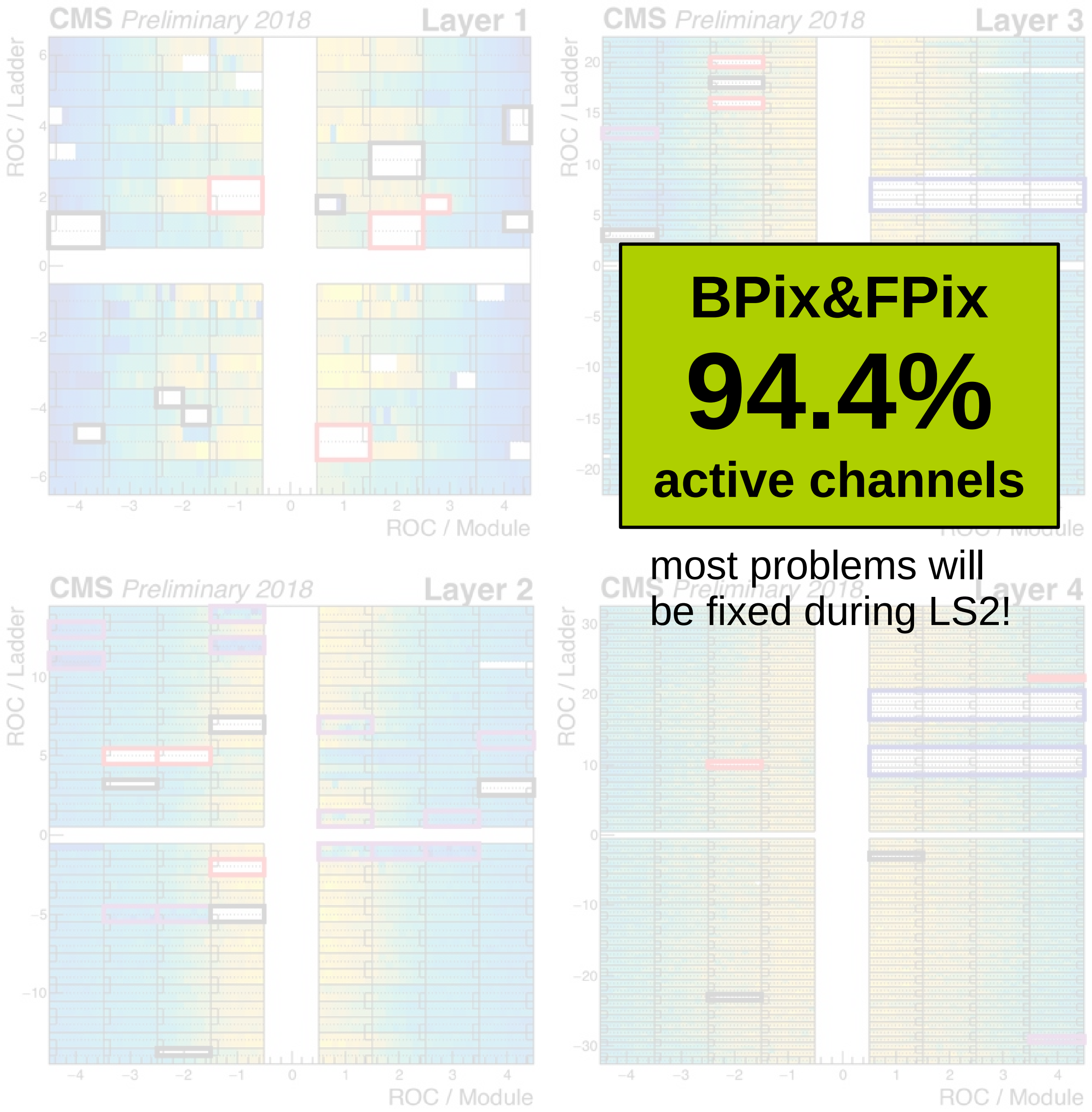
Detector Status by the end of 2018

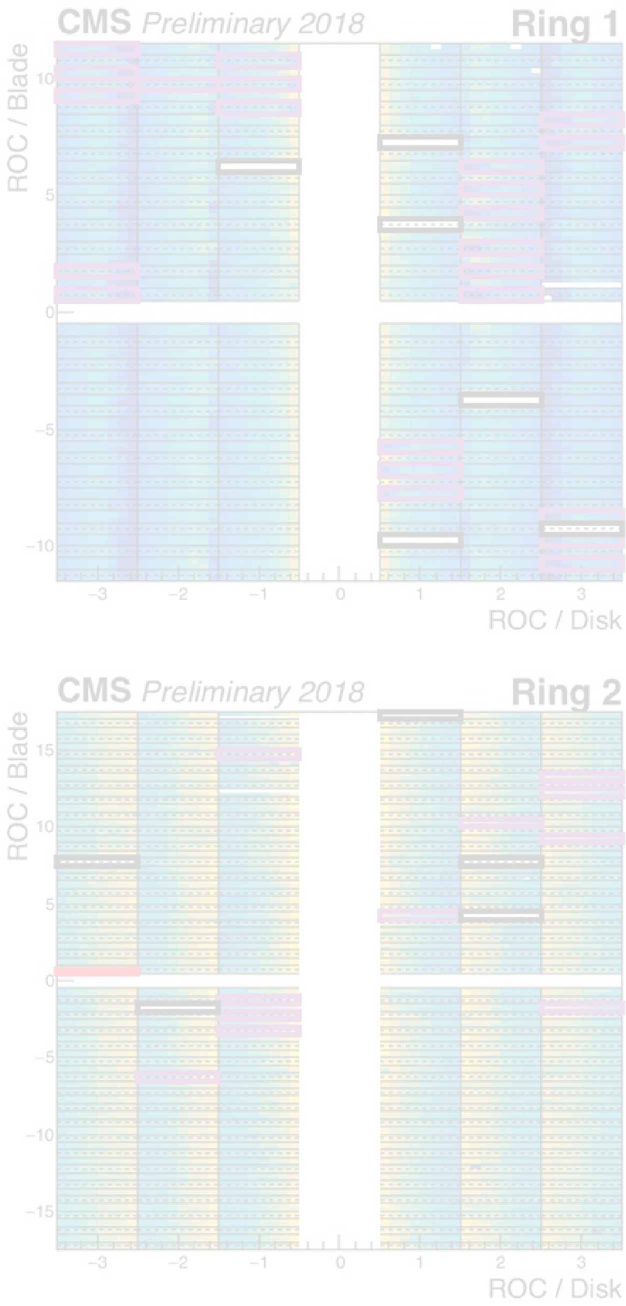


DCDC power connector problem

- → power supply granularity factor 3-4 coarser than affected parts
- → HV off to avoid HV on/ LV off

Detector Status by the end of 2018





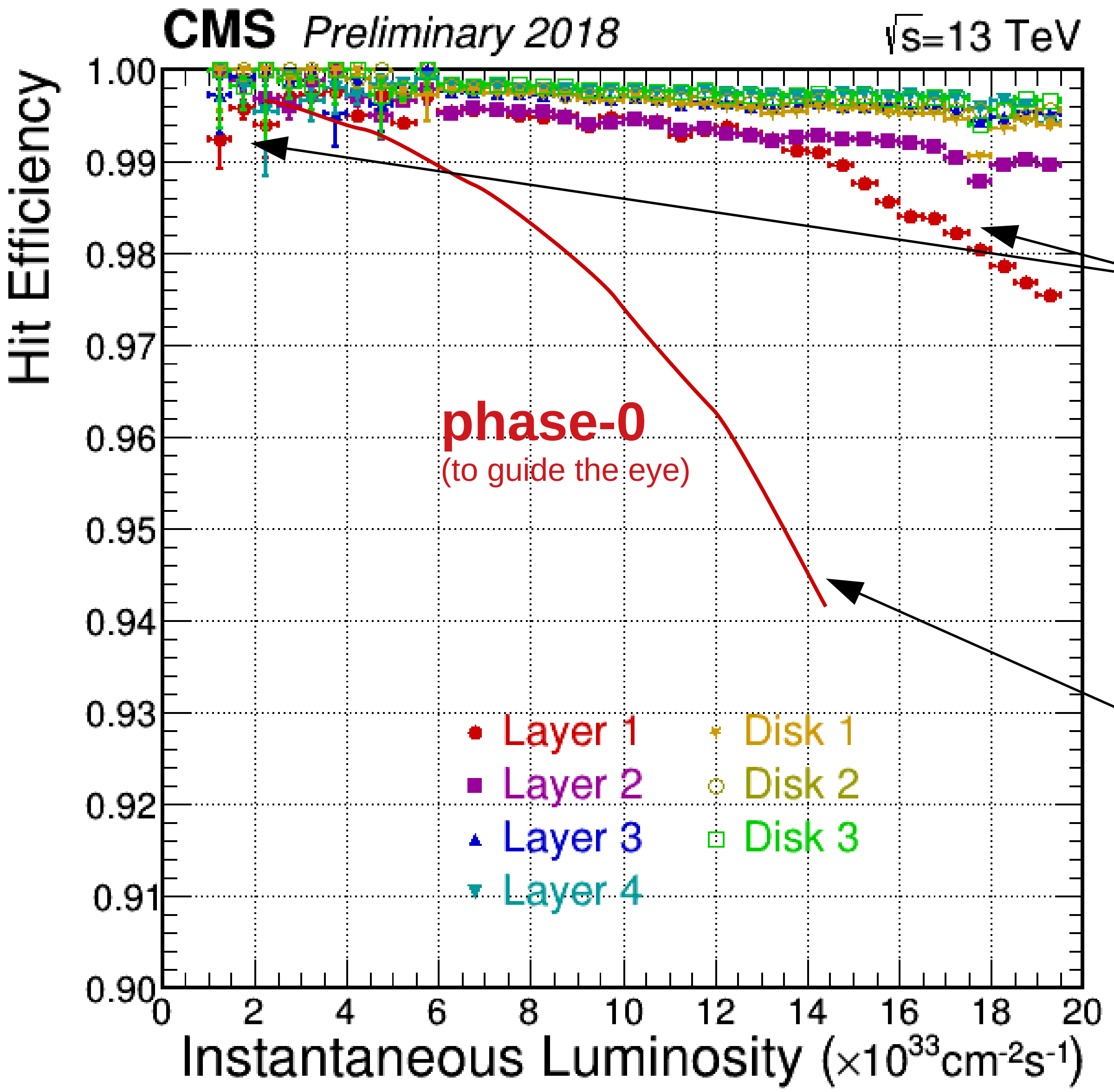
BPix&FPix

94.4%

active channels

most problems will be fixed during LS2!

Hit Efficiency

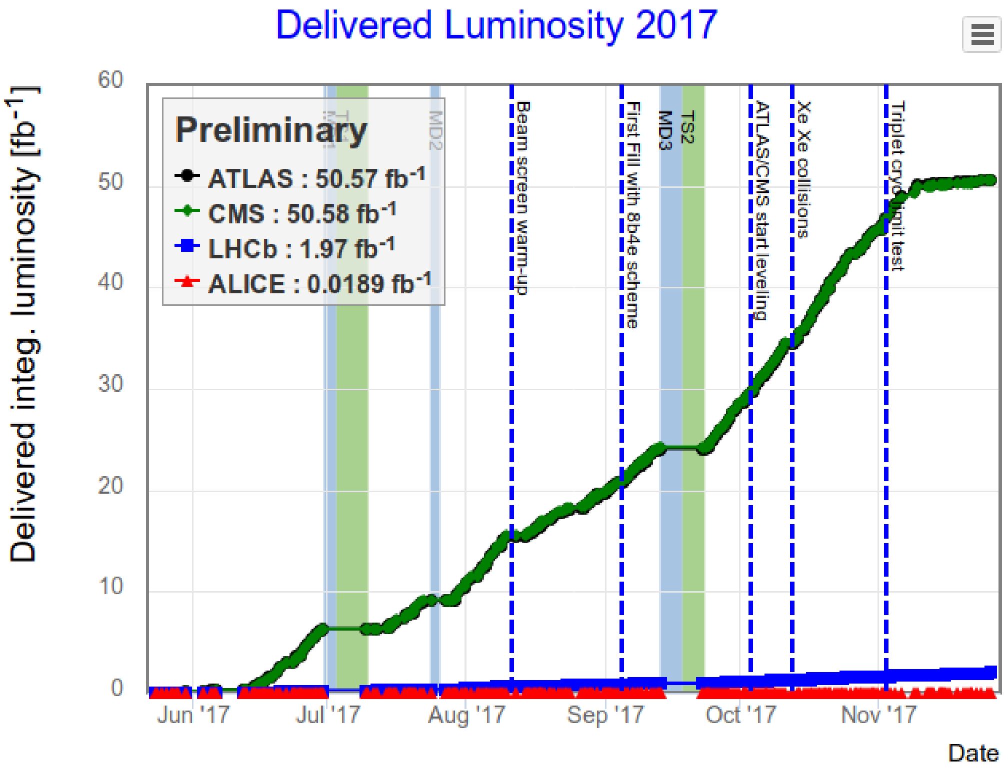


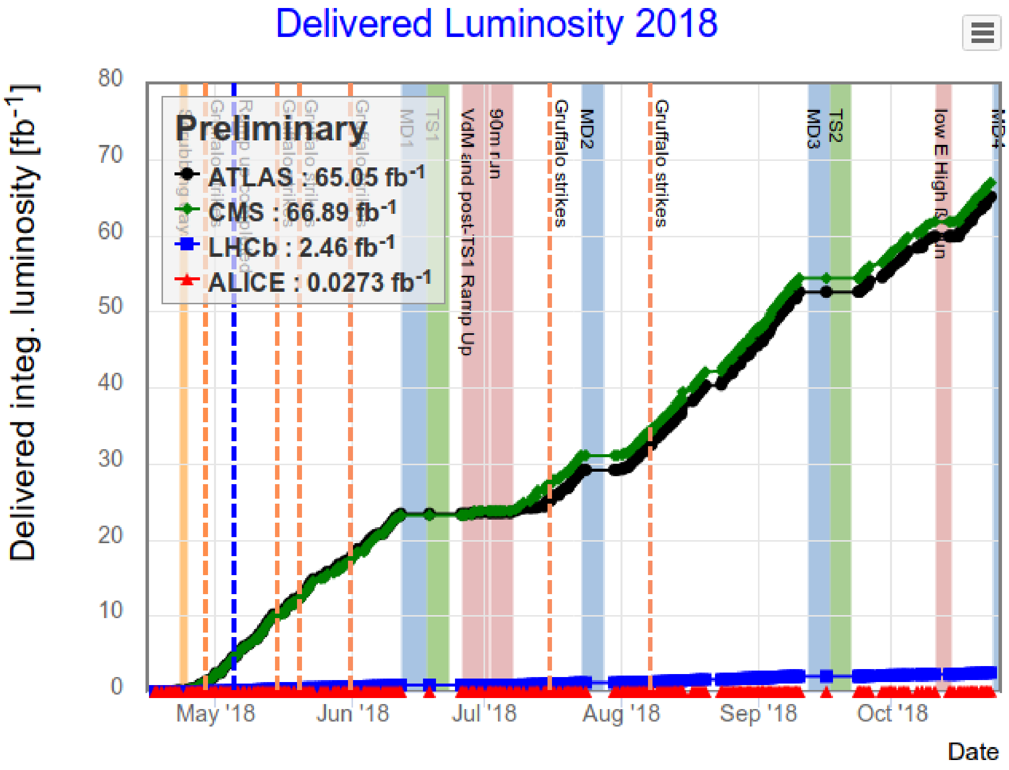
- inefficiency in layer 1 for luminosities > 1.4e34 cm^{-2}s^{-1} and <1e33 cm^{-2}s^{-1} understood
- will be further improved in new version of PROC600

note:
r_{L1}(phase-0)=43mm
r_{L1}(phase-1)=29mm

phase-1 ROCs exceed performance of phase-0 by far

Collected Dose in 2017&2018

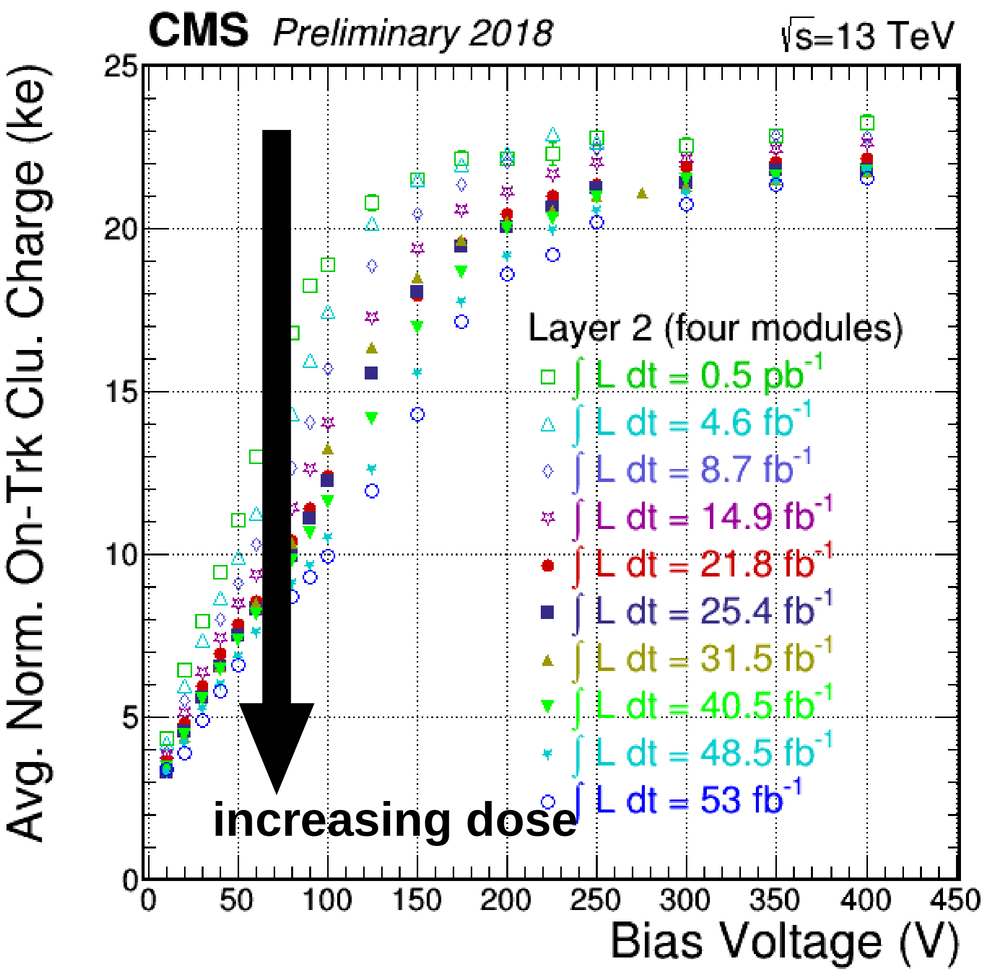


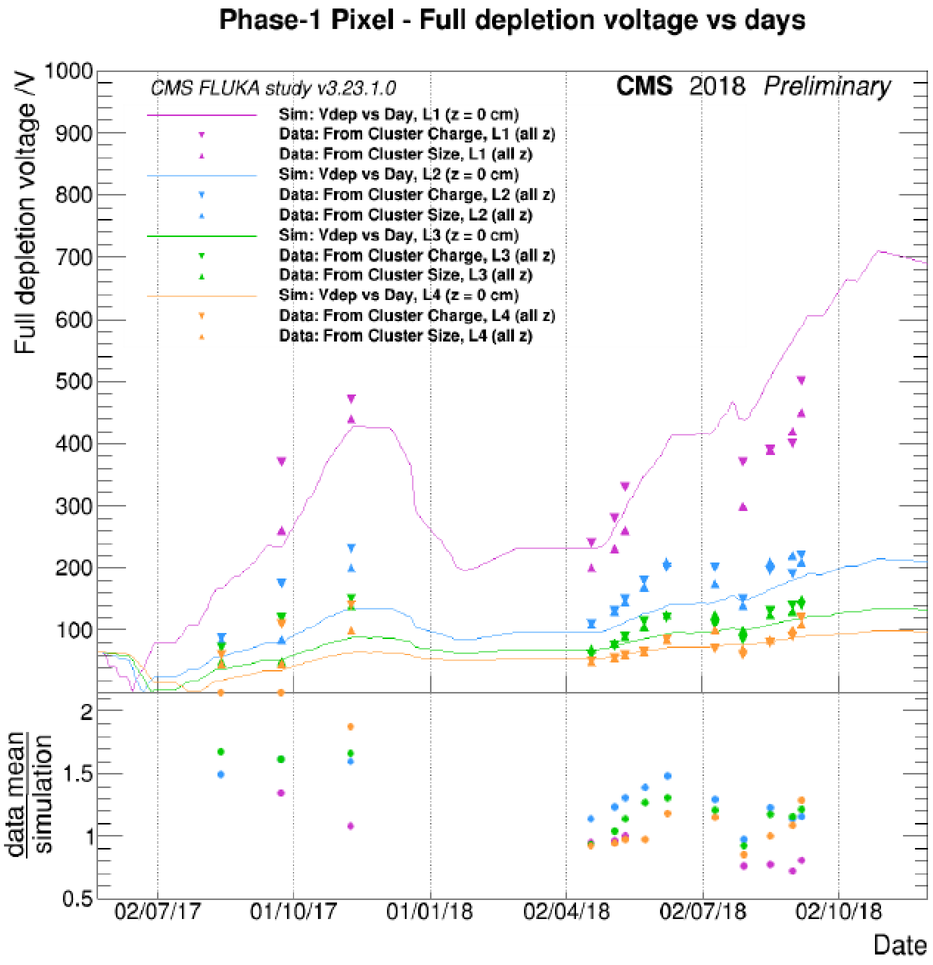


~120fb^{-1} (end of Run-2)	fluence [10^{14} n_{eq}/cm^2]	dose [Mrad Si]
layer 1 (r=29mm)	8.4	40.1
layer 2 (r=66mm)	1.5	8.5
layer 3 (r=109mm)	0.9	5.2
layer 4 (r=160mm)	0.6	2.8

- limit for ASICS: 150Mrad
- “limit” for sensor: $15 \cdot 10^{14}$ n_{eq}/cm^2
- Run-3: at least 220 fb^{-1} more = $15 \cdot 10^{14}$ n_{eq}/cm^2 (layer 1) → **$23.4 \cdot 10^{14}$ n_{eq}/cm^2** at the end of Run-3 without exchange

Monitoring and Prediction of Radiation Effects



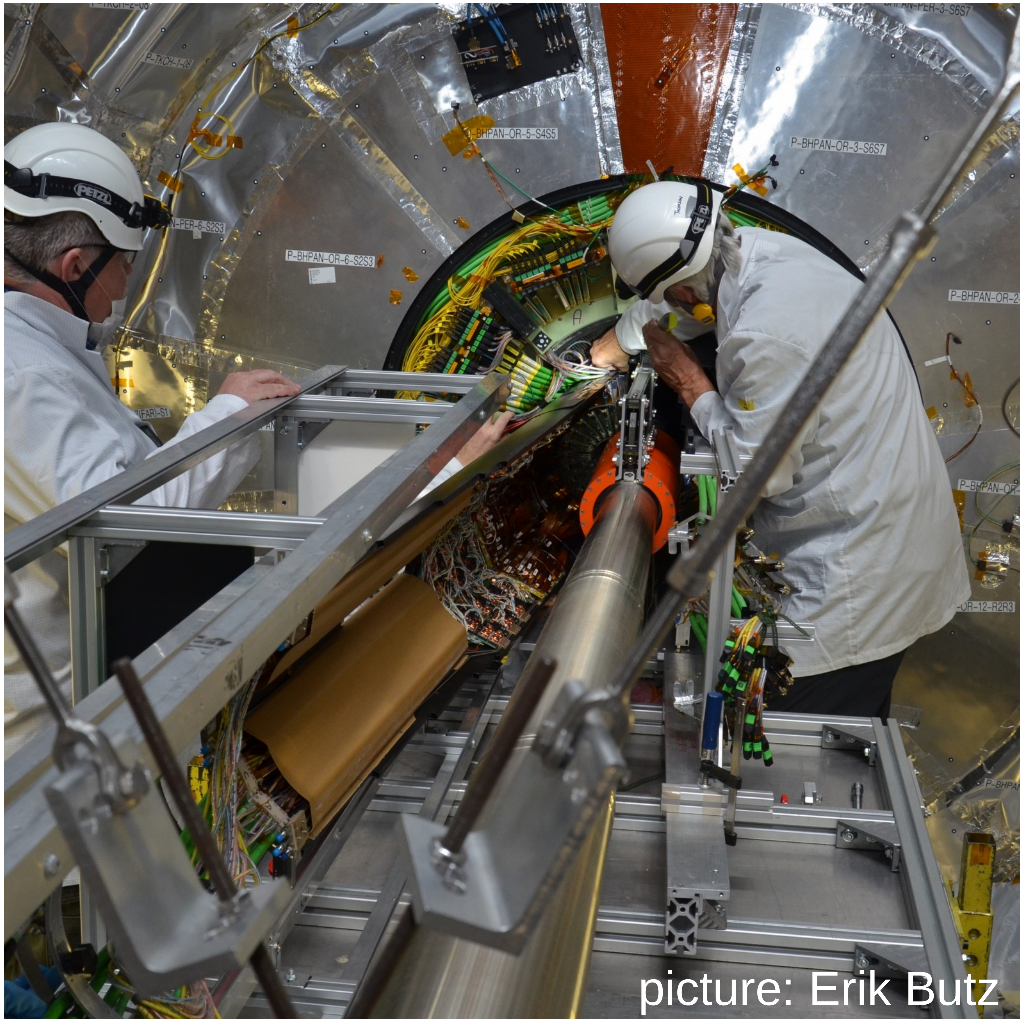


- every 1-2 weeks: bias scan on representative subset of modules in order to monitor radiation effects on sensor
- simulation based on Hamburg-model (effective space charge) to predict evolution
- very valuable tool for detector operation

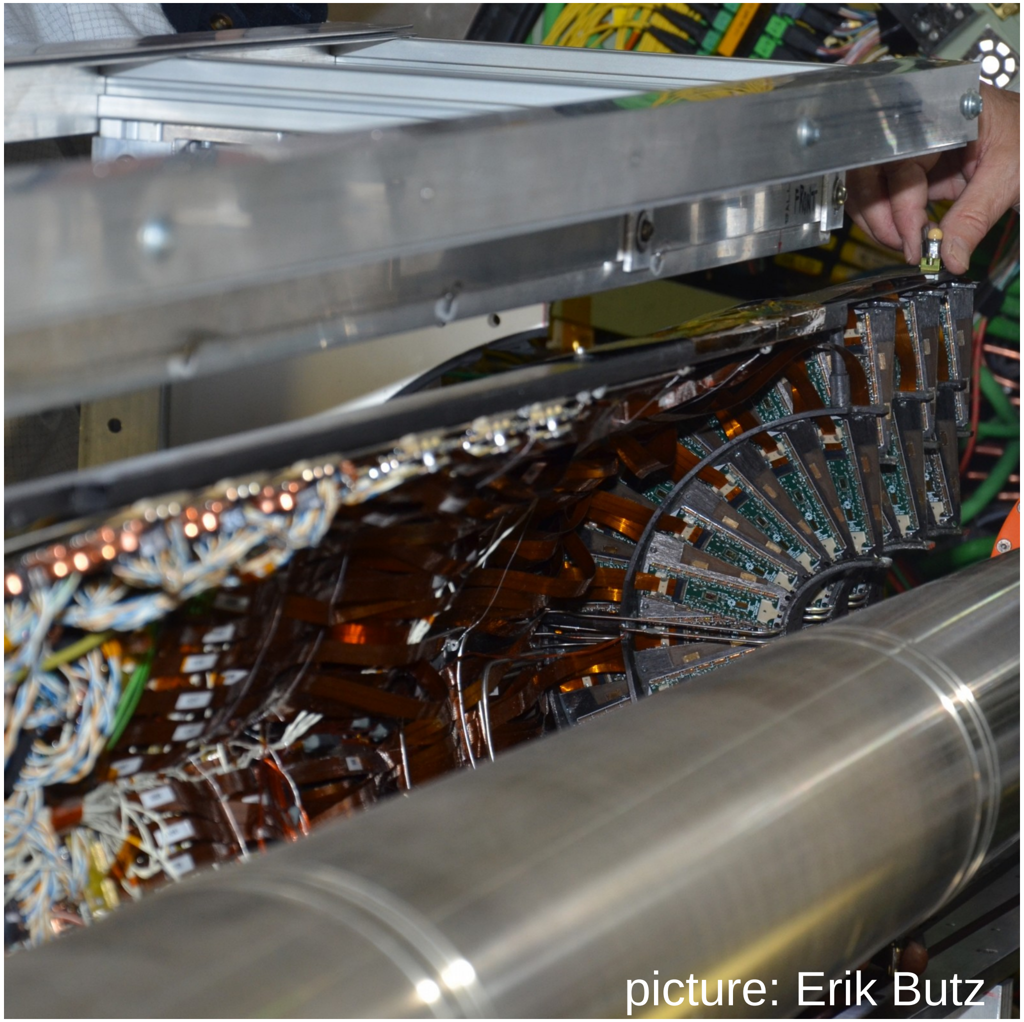
Detector Extraction
and
Scheduled Work

Detector Extraction 2019

FPix -z extraction (11.01.2019)



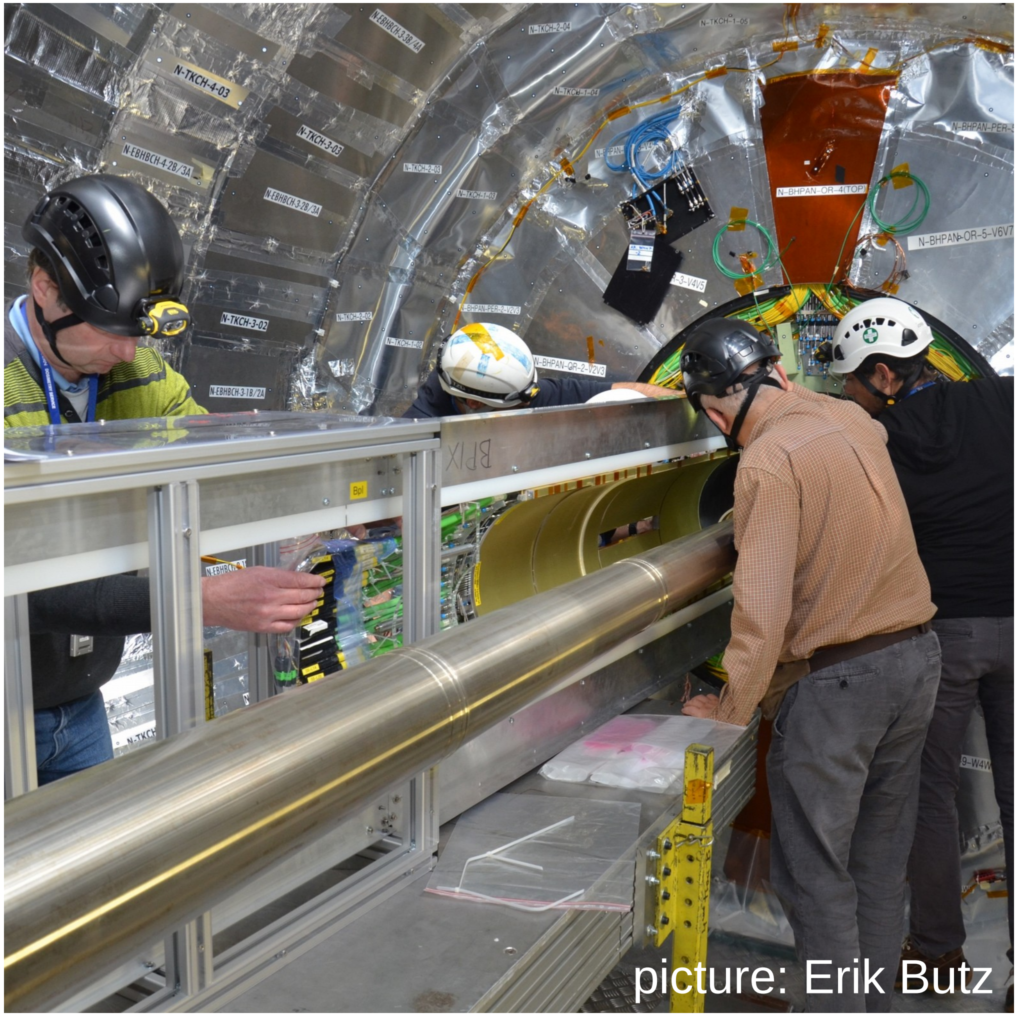
picture: Erik Butz



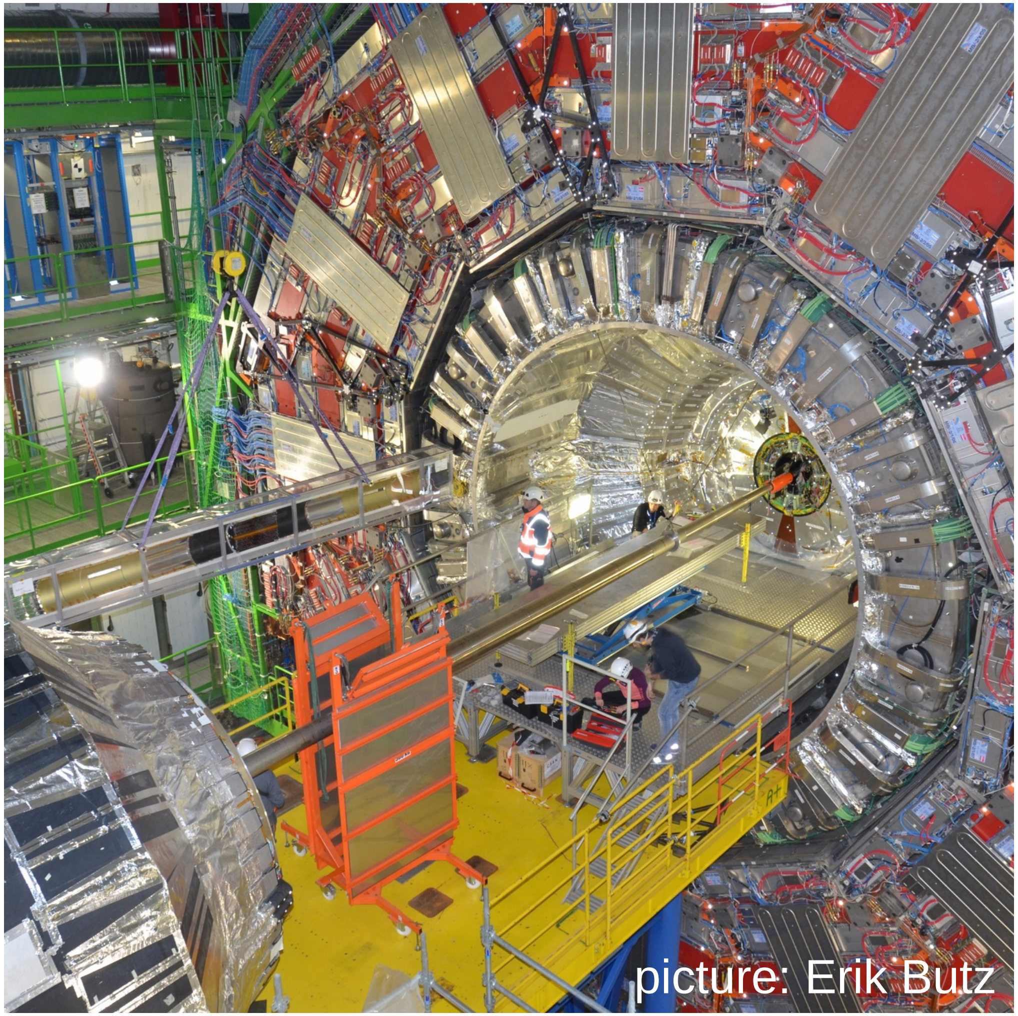
picture: Erik Butz

Detector Extraction 2019

BPix extraction (15.01.2019)



picture: Erik Butz

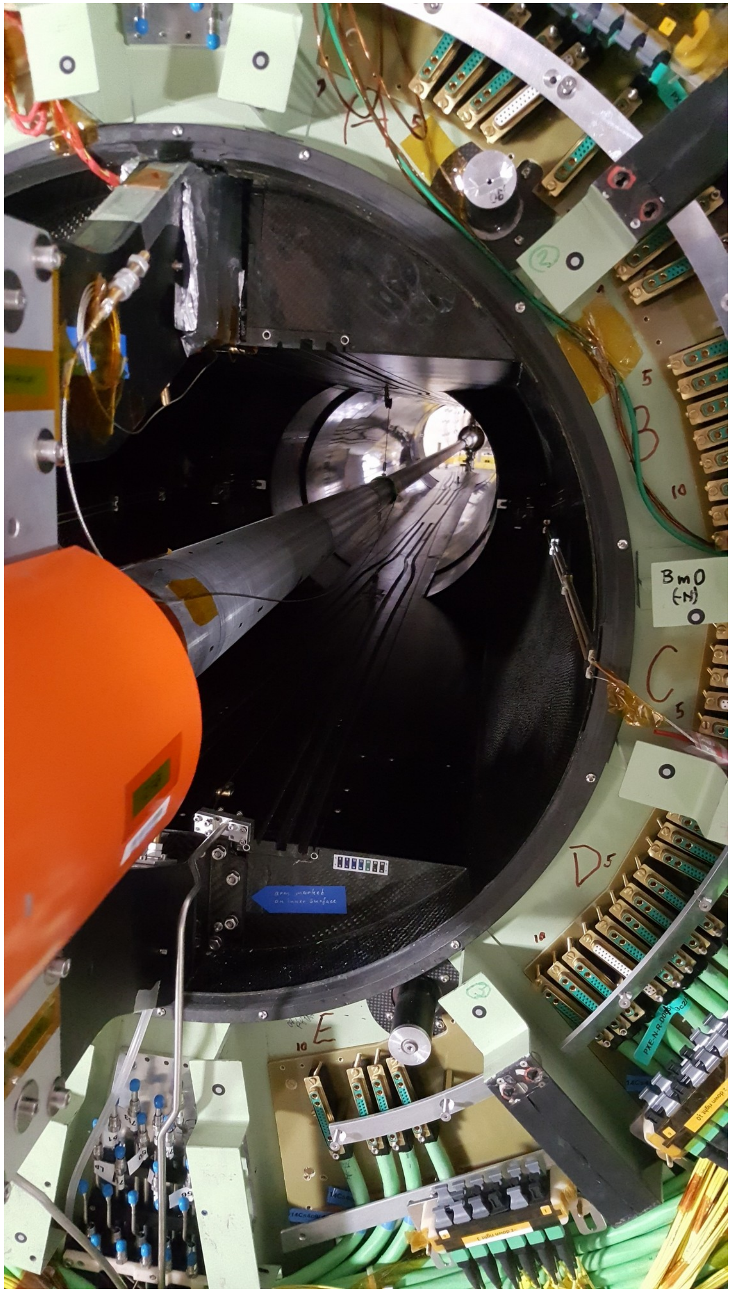


picture: Erik Butz

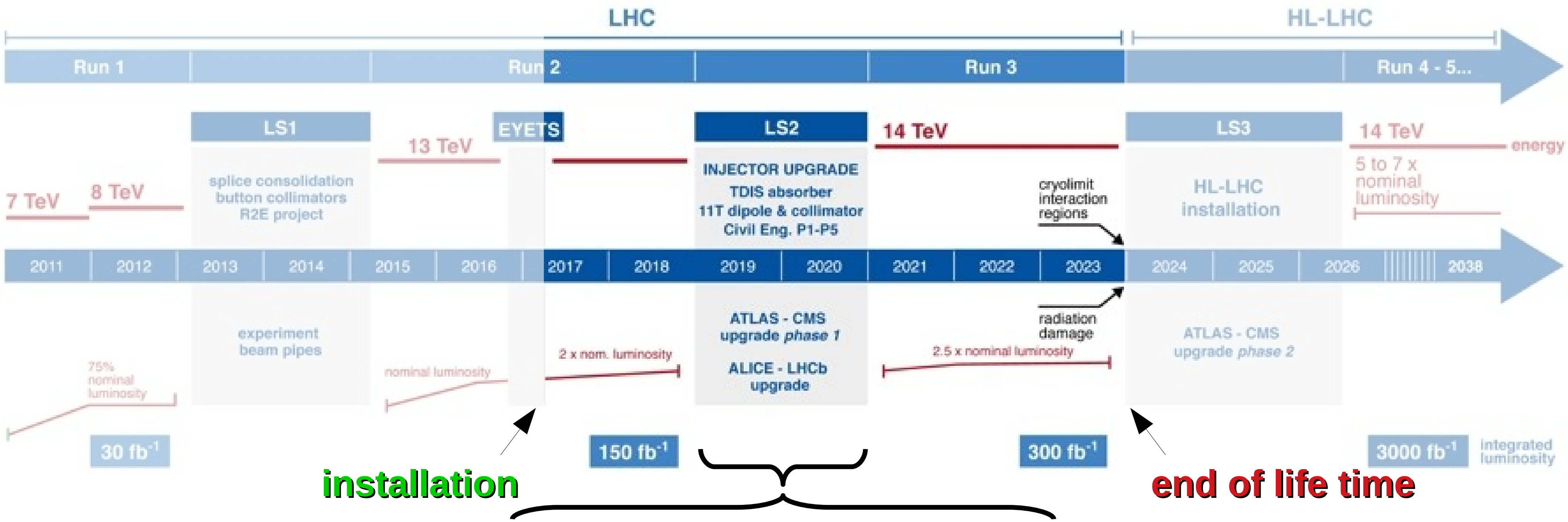
Detector Extraction 2019

picture: Erik Butz

Detector Extraction 2019



Plans during LHC Long Shutdown 2 (LS2)



general detector maintenance

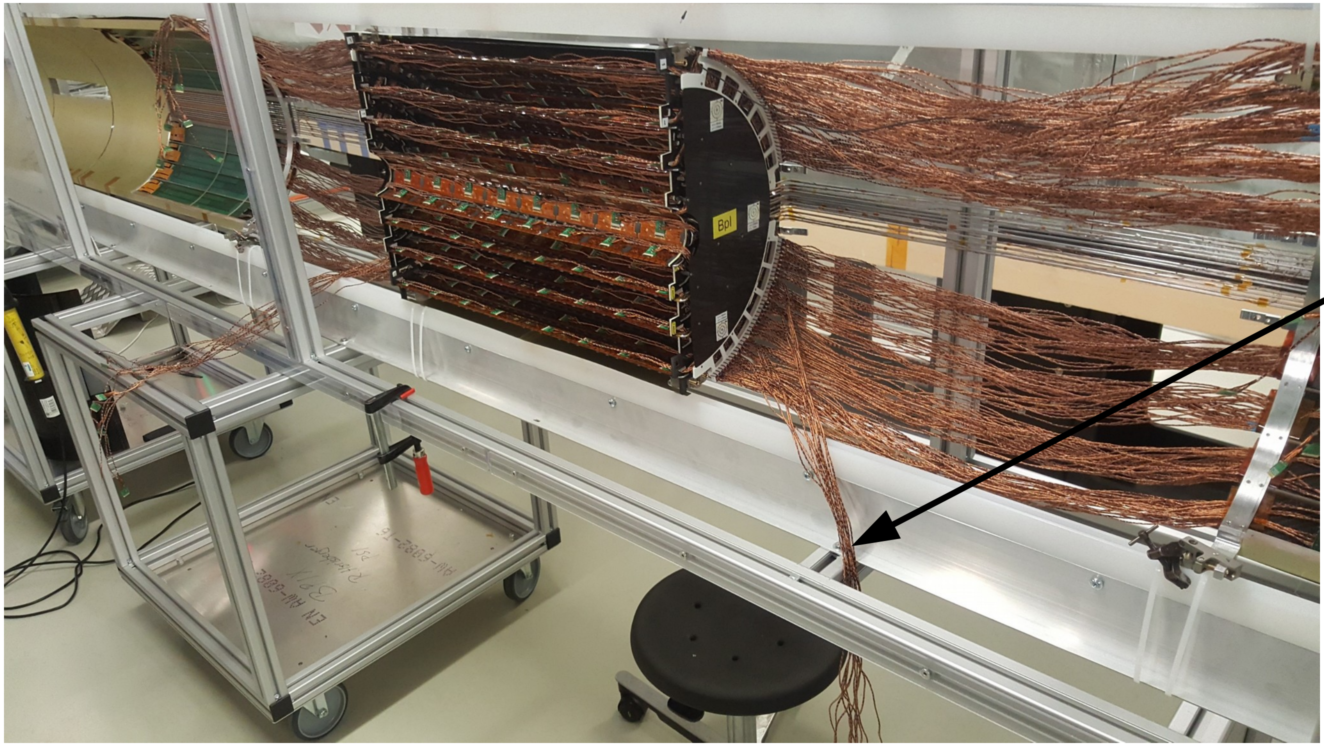
- replace all DC-DC converters with improved version
- fix problematic connections
- replace damaged modules in BPix (mostly layer 2)
- upgrade power supplies to be able to go to 800V (was 600V)

layer 1 replacement

- new version of the TBM
  - solves SEU problematic
  - allows to adjust timing difference between PROC600/psi46dig
- new version of the ROC
  - eliminates crosstalk → lower thresholds
  - mitigates sources of inefficiencies

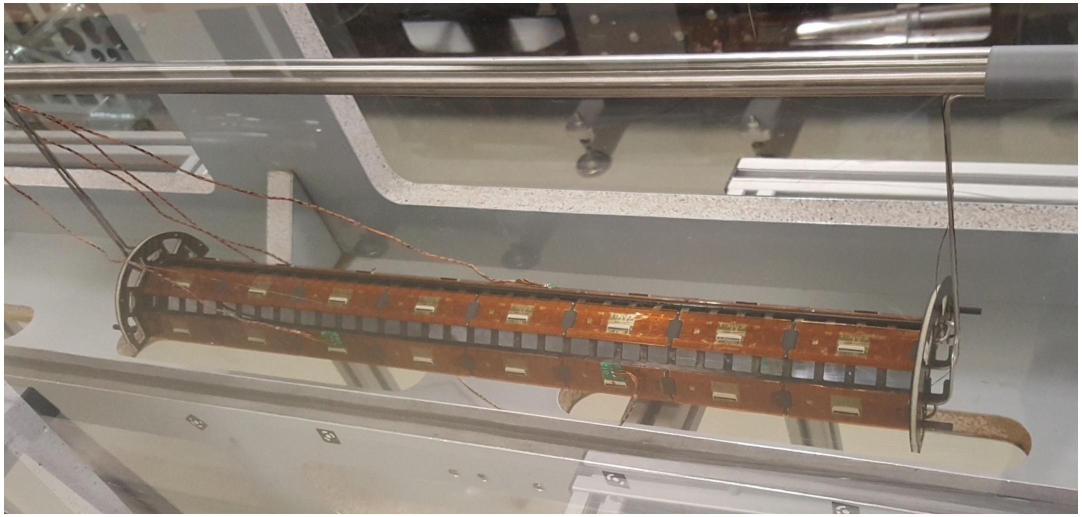
CMS Pixel detector will be in a significantly improved state at the beginning of LHC Run-3

Work has started...



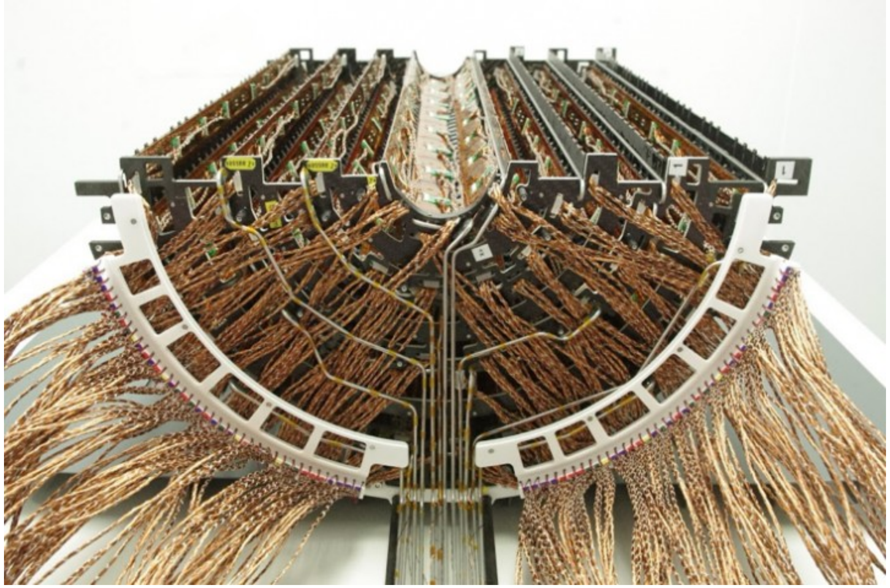
disconnected L1 module cables

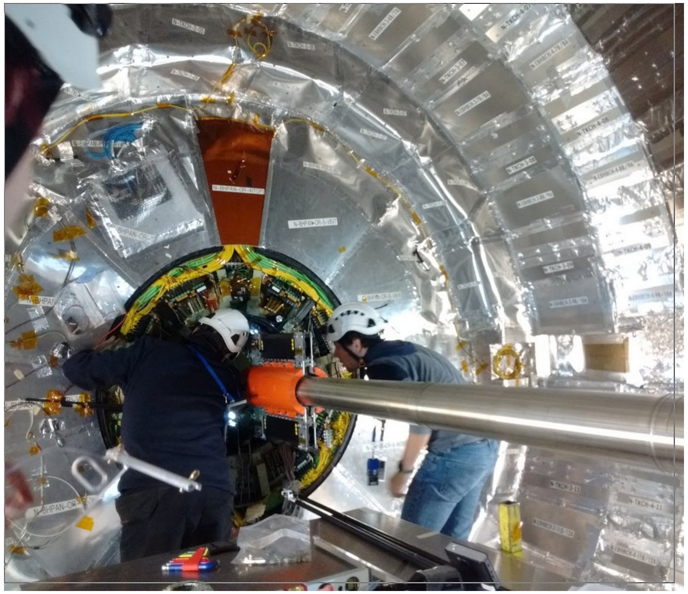
unmounted layer 1 (first half)



Conclusions

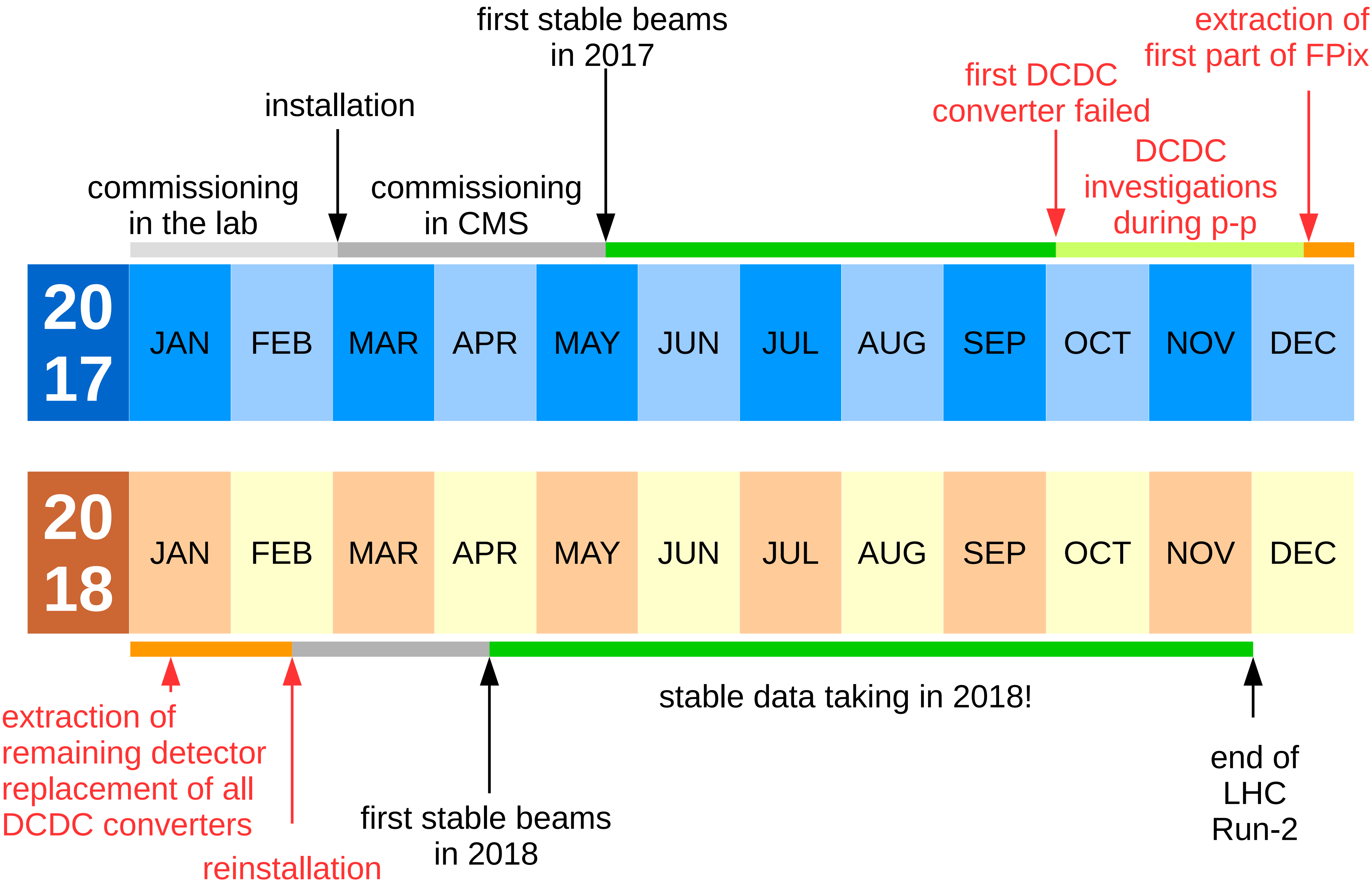
- successful commissioning and operation of the CMS phase-1 pixel detector since 2017
- unforeseen extraction at the end of 2017 due to massive DCDC failure
- very smooth running in 2018
- gathered very valuable experience with key technologies of modern silicon detectors
- significant improvements planned for LS2 to get the detector in the best possible shape for its remaining lifetime





Backup

Timeline of the last two years



commissioning
in the lab

installation

commissioning
in CMS

first stable beams
in 2017

first DCDC
converter failed

DCDC
investigations
during p-p

extraction of
first part of FPix

2017

JAN FEB MAR APR MAY JUN JUL AUG SEP OCT NOV DEC

2018

JAN FEB MAR APR MAY JUN JUL AUG SEP OCT NOV DEC

extraction of
remaining detector
replacement of all
DCDC converters

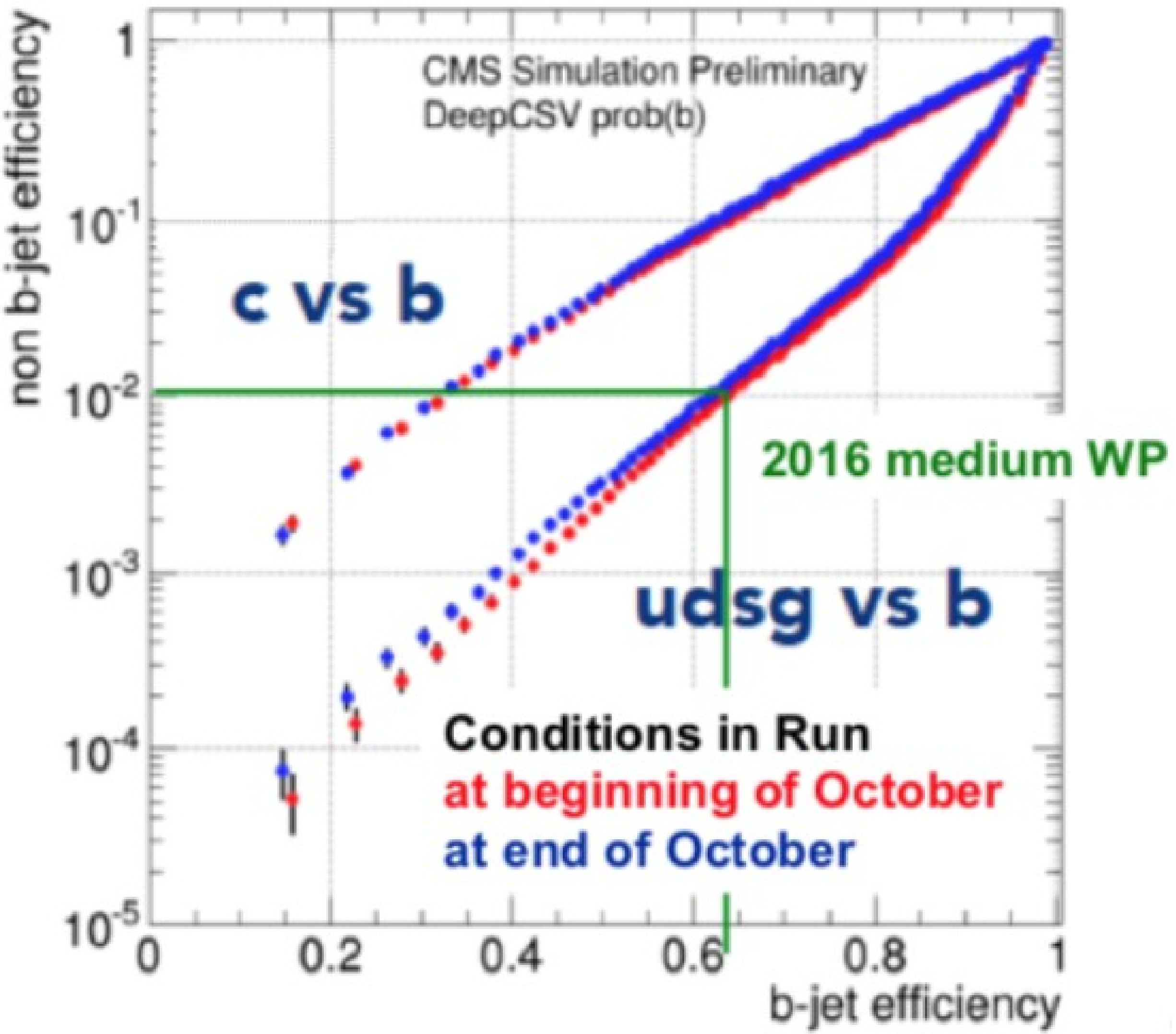
reinstallation

first stable beams
in 2018

stable data taking in 2018!

end of
LHC
Run-2

CMS Pixel Detector – Physics Impact



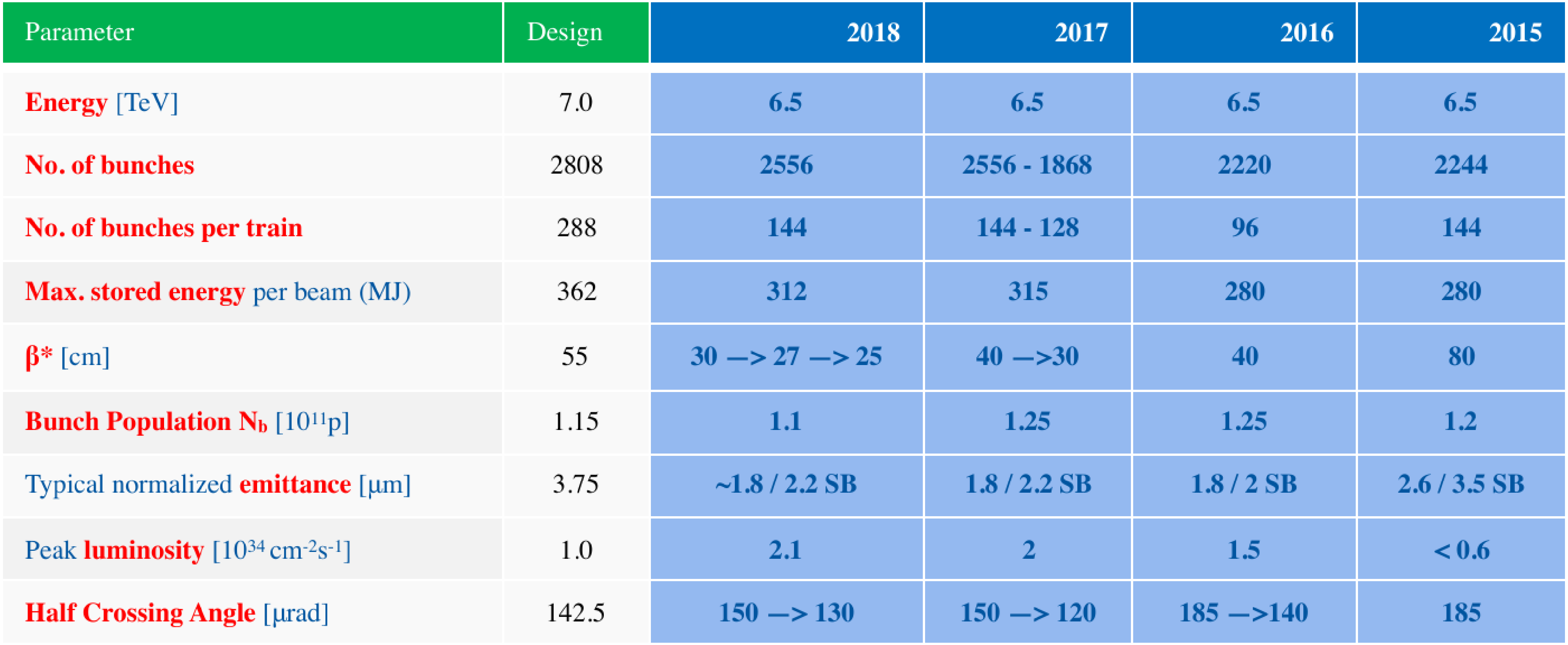
c vs b

2016 medium WP

udsg vs b

Conditions in Run
at beginning of October
at end of October

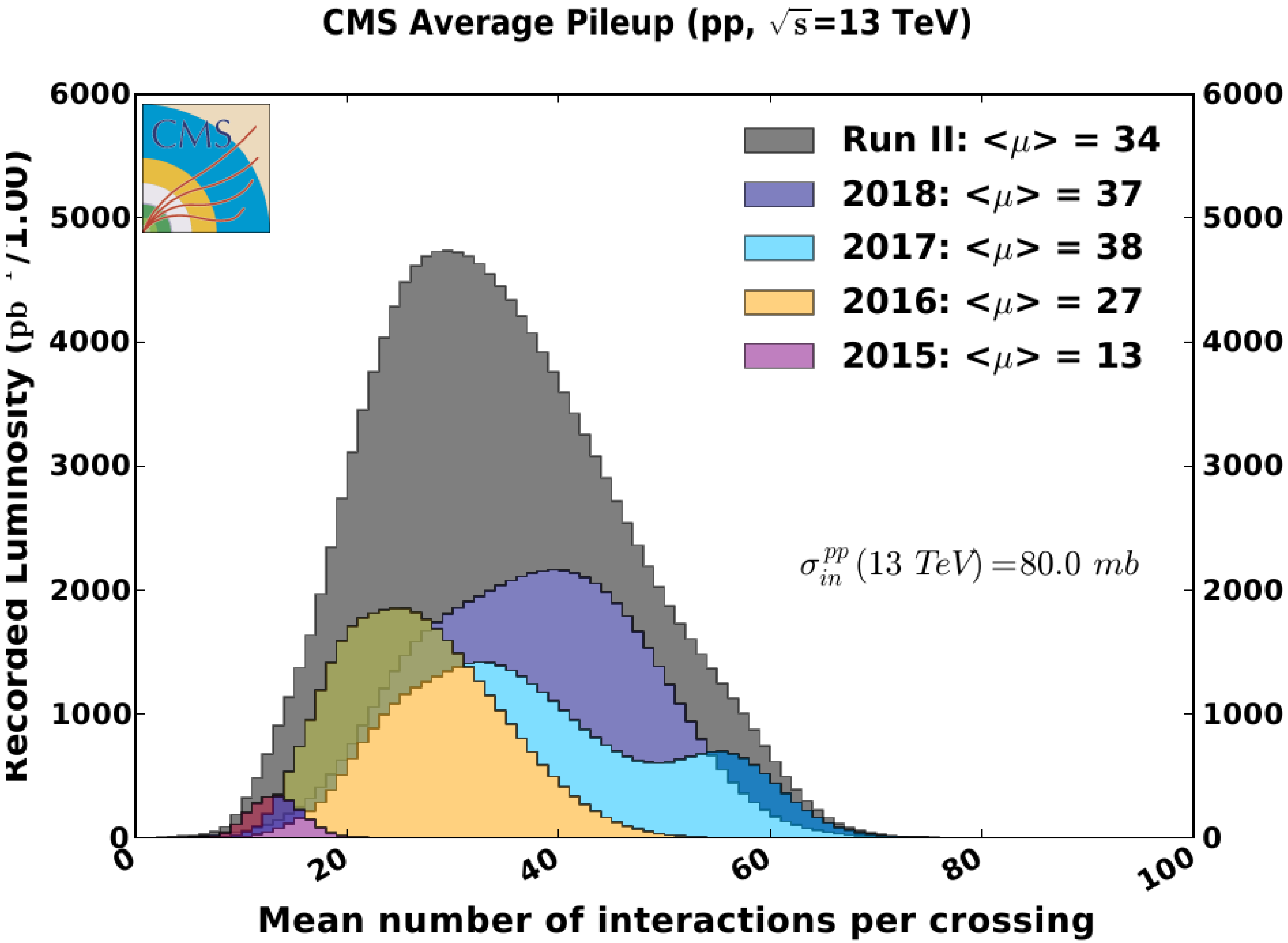
LHC Parameters during Run-2



Parameter	Design	2018	2017	2016	2015
Energy [TeV]	7.0	**6.5**	**6.5**	**6.5**	**6.5**
No. of bunches	2808	**2556**	**2556 - 1868**	**2220**	**2244**
No. of bunches per train	288	**144**	**144 - 128**	**96**	**144**
Max. stored energy per beam (MJ)	362	**312**	**315**	**280**	**280**
β^* [cm]	55	**30 —> 27 —> 25**	**40 —>30**	**40**	**80**
Bunch Population N_b [10^{11}p]	1.15	**1.1**	**1.25**	**1.25**	**1.2**
Typical normalized **emittance** [µm]	3.75	**~1.8 / 2.2 SB**	**1.8 / 2.2 SB**	**1.8 / 2 SB**	**2.6 / 3.5 SB**
Peak **luminosity** [10^{34} cm^{-2}s^{-1}]	1.0	**2.1**	**2**	**1.5**	**< 0.6**
Half Crossing Angle [µrad]	142.5	**150 —> 130**	**150 —> 120**	**185 —>140**	**185**

https://indico.cern.ch/event/751857/contributions/3259373/attachments/1783143/2910577/belen-Evian2019.pdf

Pile-up Distribution during Run-2



Projected LHC Parameters in Run-3

Parameters at the end of a fill

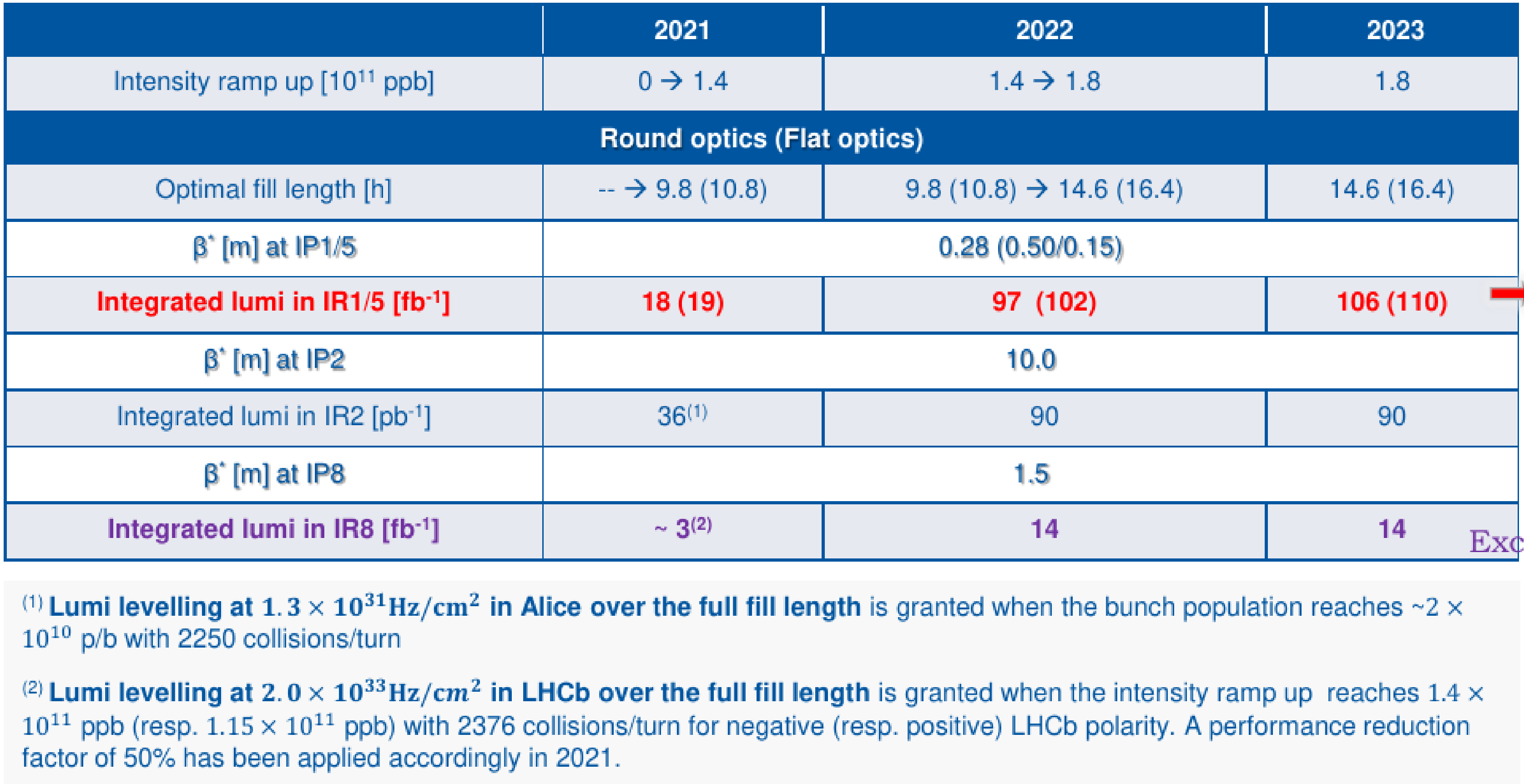
ROUND OPTICS	2021	2022	2023	Comment
Beam energy [TeV]	7.0			7 TeV is being re-discussed for Run III
Collisions at IP1/5 & IP2/IP8	2736/2736 & 2250/2376			Possible heat-load limitation not included
Bunch length [ns]	1.0			1.0 ns after ~10 h of SB, then kept constant
Normalized emittance [μm]	2.5			
β* [m] at IP1/5	0.28			Telescopic optics
Half X-angle [mrad] at IP1/5	162 (9.4 σ_{beam})			V/H
Levelling time @ $2 \times 10^{34} Hz/cm^2$ [h]	**0.0 → 5.0**	**5.0 → 11.9**	**11.9**	**Burn off calculated with 110 mb (IR8 included)**
Optimal fill length [h]	-- → 9.8	9.8 → 14.6	14.6	Assuming a turn around time of 4 h
Bunch charge [10^{11} ppb]	0 → 0.89	0.89 → 0.97	0.97	
β* [m] at IP2/IP8	10.0/1.5	10.0/1.5	10.0/1.5	β* @ IP2/8 is kept constant over the full Run
Half X-angle [mrad] at IP2/8	200/250	200/250	200/250	V/H at IP2/8 (V-Xing in IR8 under discussion)
Half || sep. @ IP2 [σ_{coll}]	0 → 1.60(1)	1.60 → 1.64	1.64	For $1.3 \times 10^{31} \mathrm{Hz/cm^2}$ & 200-70=130 μrad Xing
Half || sep. @ IP8 [σ_{coll}]	0 → 0.13(2)	0.13 → 0.38	0.38	For $2.0 \times 10^{33} \mathrm{Hz/cm^2}$ & 250+135=385 rad Xing (worst case)

(1) **Lumi levelling at $1.3 \times 10^{31} \mathrm{Hz/cm^2}$ in Alice over the full fill length** is granted when the intensity ramp up reaches ~2×10^{10} ppb with 2250 collisions/turn

(2) **Lumi levelling at $2.0 \times 10^{33} \mathrm{Hz/cm^2}$ in LHCb over the full fill length** will be granted towards the end of 2021 @ 1.4×10^{11} ppb for negative LHCb polarity assuming 2376 collisions/turn [and earlier for positive polarity, with 115 μrad internal crossing, when the intensity ramp up reaches 1.15×10^{11} ppb].

https://indico.cern.ch/event/751857/contributions/3259414/attachments/1782259/2914150/nkarast_evianRunIII.pdf

Projected LHC Parameters in Run-3



	2021	2022	2023
Intensity ramp up [10^{11} ppb]	0 → 1.4	1.4 → 1.8	1.8
Round optics (Flat optics)			
Optimal fill length [h]	-- → 9.8 (10.8)	9.8 (10.8) → 14.6 (16.4)	14.6 (16.4)
β* [m] at IP1/5	0.28 (0.50/0.15)		
Integrated lumi in IR1/5 [fb^{-1}]	**18 (19)**	**97 (102)**	**106 (110)**
β* [m] at IP2	10.0		
Integrated lumi in IR2 [pb^{-1}]	36(1)	90	90
β* [m] at IP8	1.5		
Integrated lumi in IR8 [fb^{-1}]	**~ 3(2)**	**14**	**14**

➡ 411 (421)

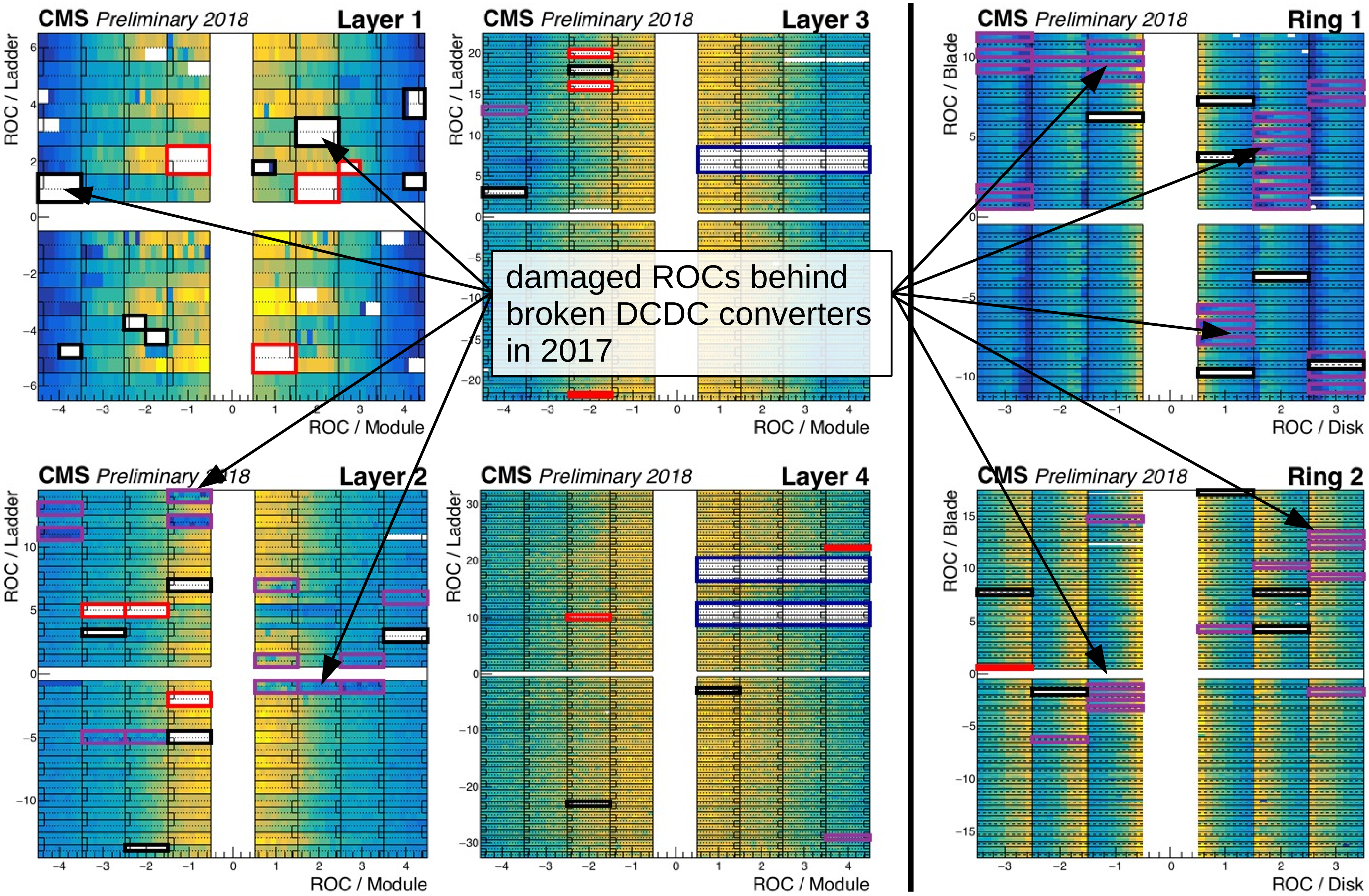
Exceeds target

(1) **Lumi levelling at $1.3 \times 10^{31}\text{Hz/cm}^2$ in Alice over the full fill length** is granted when the bunch population reaches ~2 × 10^{10} p/b with 2250 collisions/turn

(2) **Lumi levelling at $2.0 \times 10^{33}\text{Hz/cm}^2$ in LHCb over the full fill length** is granted when the intensity ramp up reaches 1.4 × 10^{11} ppb (resp. 1.15 × 10^{11} ppb) with 2376 collisions/turn for negative (resp. positive) LHCb polarity. A performance reduction factor of 50% has been applied accordingly in 2021.

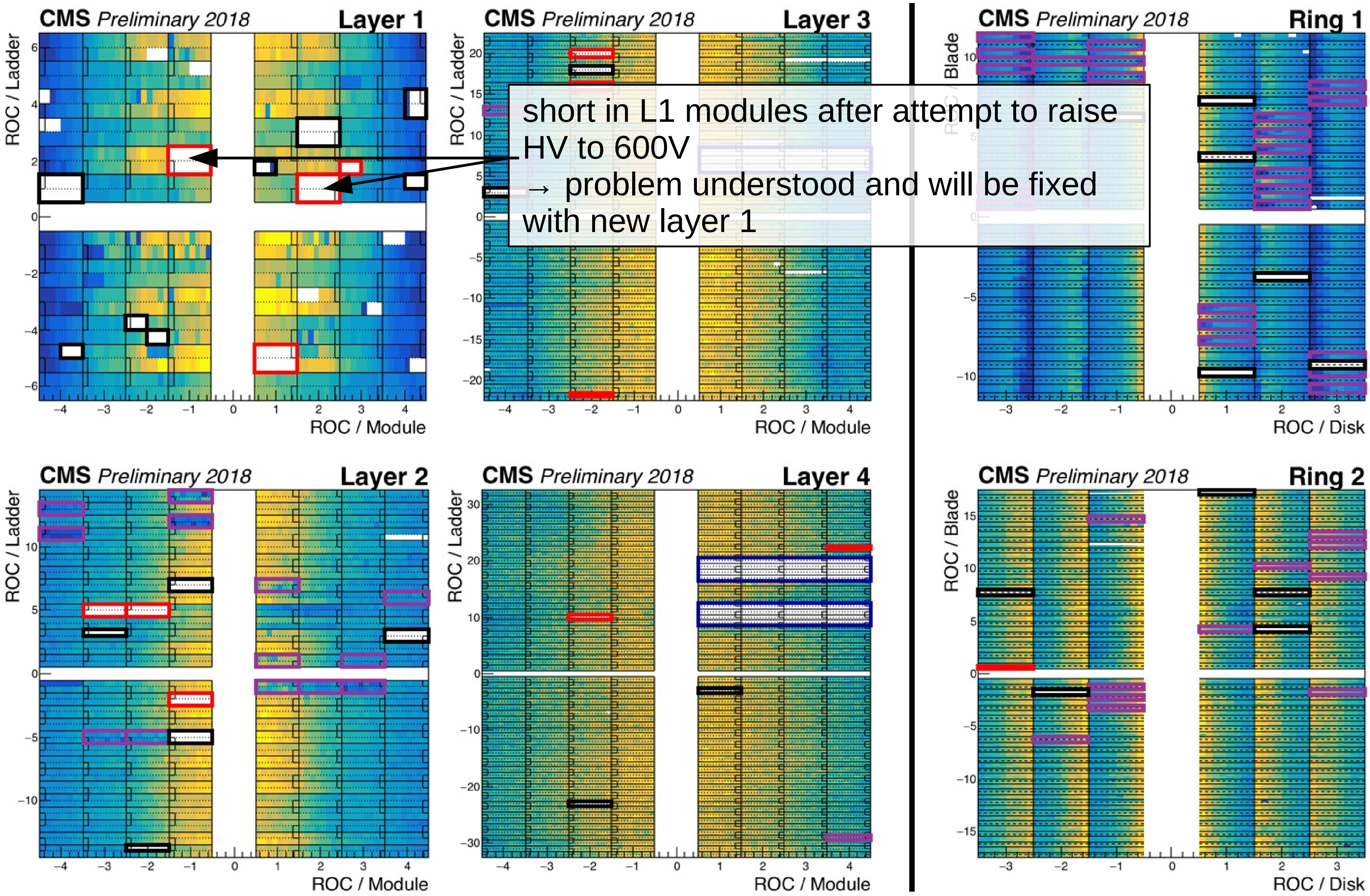
https://indico.cern.ch/event/751857/contributions/3259414/attachments/1782259/2914150/nkarast_evianRunIII.pdf

Detector Status by the end of 2018



damaged ROCs behind broken DCDC converters in 2017

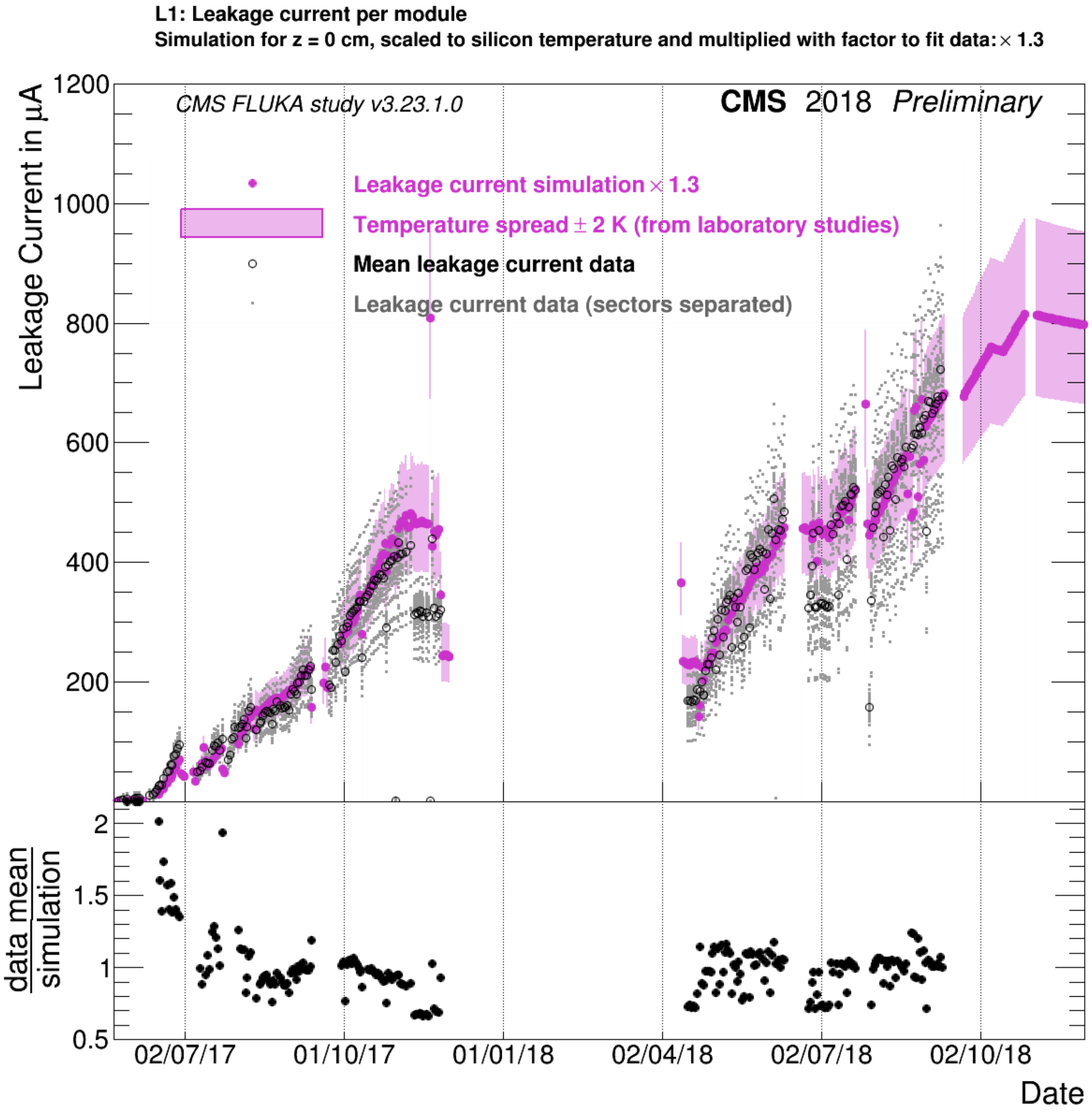
Detector Status by the end of 2018



short in L1 modules after attempt to raise HV to 600V

→ problem understood and will be fixed with new layer 1

Monitoring and Prediction of Radiation Effects



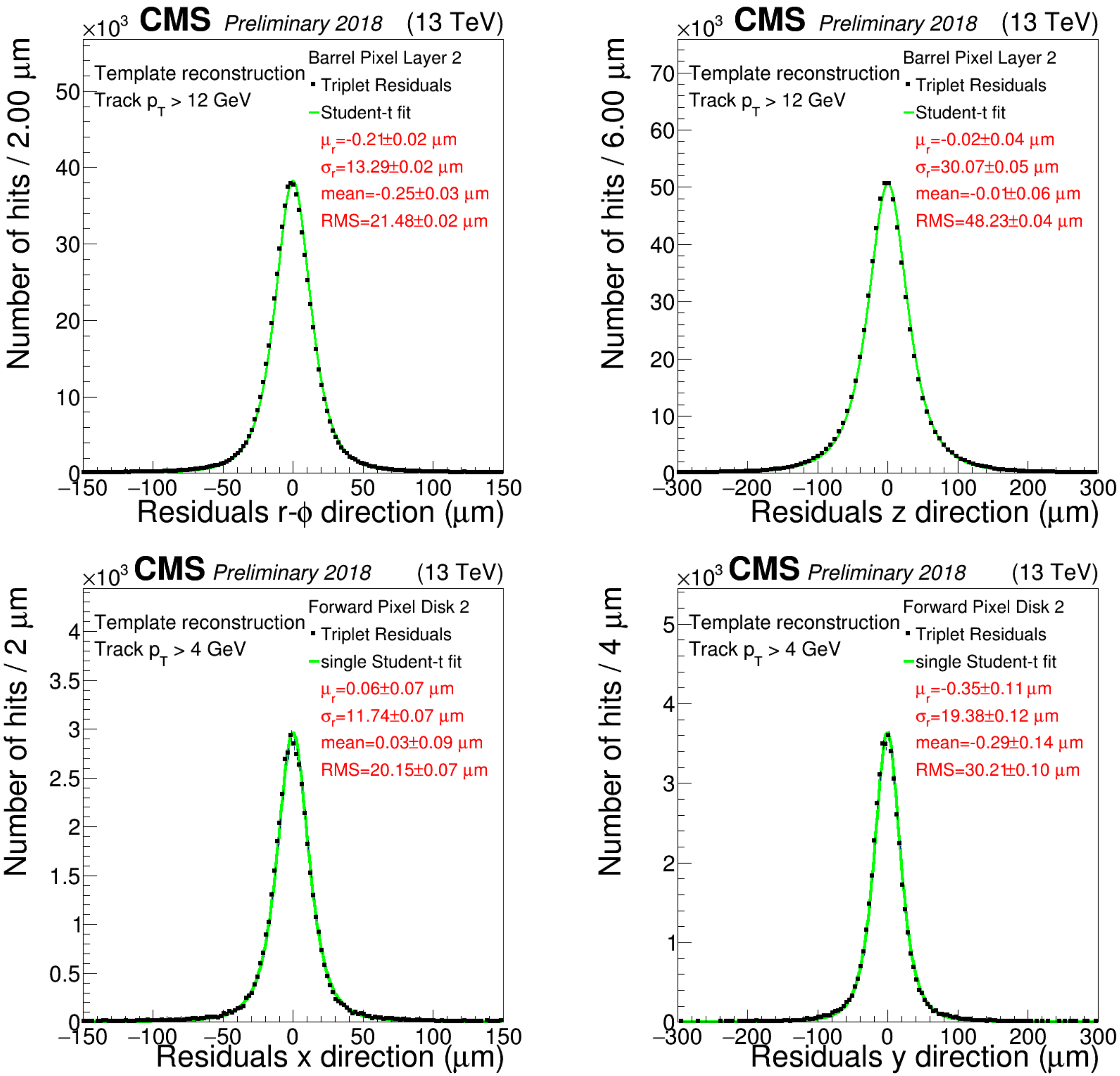
leakage currents modeling

- impressively well matching prediction (except a constant factor!)
- assumption: silicon temperature ~-8.5°C
- reasonable comparing with data from thermal mock-up
- thermal mock-up again one of the main ingredients to understand temperatures inside of the detector
- ongoing work: further improvements of the temperature model

Residuals/ Resolution

BPix L2

FPix D2



13 µm (r-φ)
30 µm (z)

pixel size:
150x100µm^2

12 µm (x^{mod}),
19 µm (y^{mod})

excellent hit resolution