Development of n^+-in-p silicon microstrip and pixel sensors for HL-LHC in Japan and understanding their performance with TCAD simulations

Y. Unno (KEK)

In retrospect, a better title would be ...

Development of silicon tracking sensors for high radiation environment in Japan and understanding their performance with TCAD simulations

Y. Unno (KEK)

Contents

- Beginning of radiation-tolerant silicon tracking sensors
  - Understanding of radiation damages
  - Visualization of the hot spots – microdischarge
  - Application to silicon microstrip sensor of LHC
- Towards further radiation-tolerant silicon tracking sensors
  - Dawn of p-type sensor
  - Towards very high voltage operation
  - R&D of n^+-in-p strip and pixel sensors for HL-LHC
  - Understanding with Technology CAD simulation

Radiation Damage Studies

- Aiming silicon tracking sensor for high radiation environment
  - the 1st study of radiation damage in our field… 30 yrs ago
    - T. Kondo et al, Radiation Damage Test of Silicon Microstrip Detectors
    - Proc. of the 1984 Summer Study on the Design and Utilization of SSC, June 23-July 13, 1984, Snowmass, Colorado, pp. 612-614
- The messages were
  - It was shown that silicon is rad-hard, little pulse-height change, cooling needed,
    - although the prevailing opinion was that silicon vertex detectors were not possible at 10^{33} luminosity.

Radiation Damage Studies

- Since then, radiation damage studies are continued in Japan, Europe, US., and elsewhere
  - Two papers were then published in 1988
  - T. Ohsugi, ... T. Kondo, … K. Yamamoto .., “Radiation Damage in Silicon Microstrip DetectorsT”, Nucl. Instr. Meth. A265(1988)105
  - M. Nakamura,…T. Kondo, "Radiation Damage Test of Silicon Multistrip Detectors", Nucl. Instr. Meth. A270(1988)42, using the irradiated sensor by 800 GeV protons

Increase of leakage current

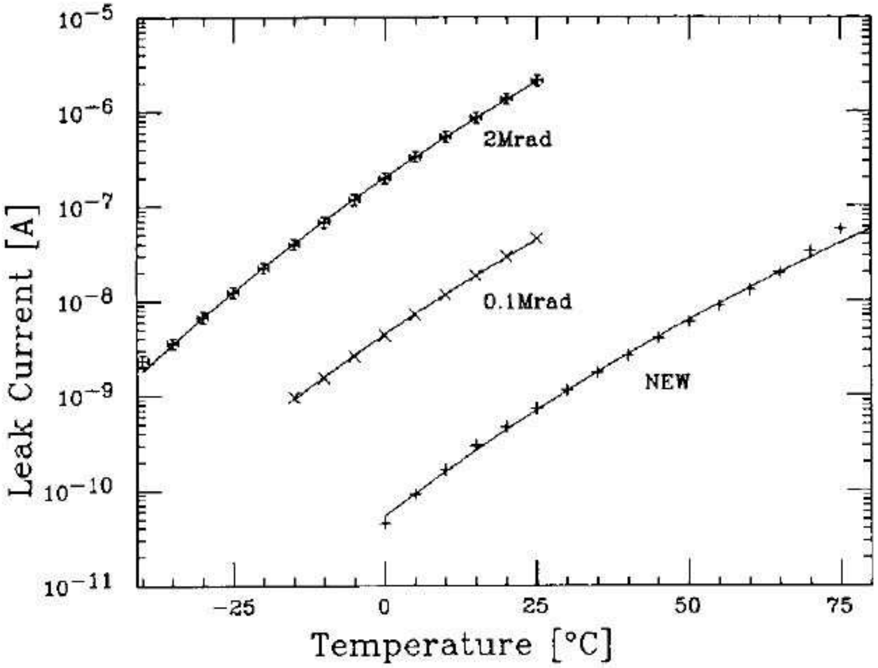


Fig. 5. Temperature dependence of the leakage current. The solid lines are the best fits using the formula given in the text.

Also, temperature dependence of bulk leakage current

$$J_g(T) \propto T^2 \exp(-\frac{E_{ef}}{2k_B T})$$

$$E_{ef} = 1.20\,\mathrm{eV}$$

- Radiation Damage in Silicon Microstrip Detectors
  - T. Ohsugi, ... T. Kondo, … K. Yamamoto .., Nucl. Instr. Meth. A265(1988)105

Type inversion of the silicon

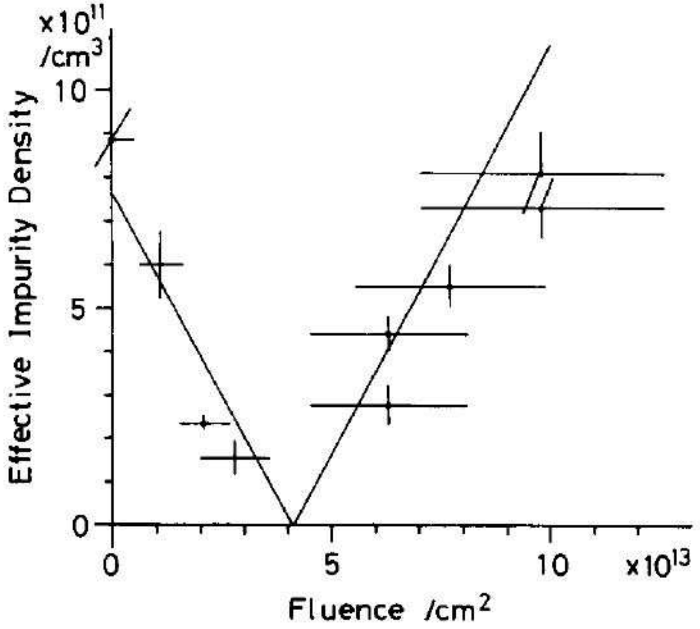


Fig. 25. Estimated effective impurity density as a function of proton fluence.

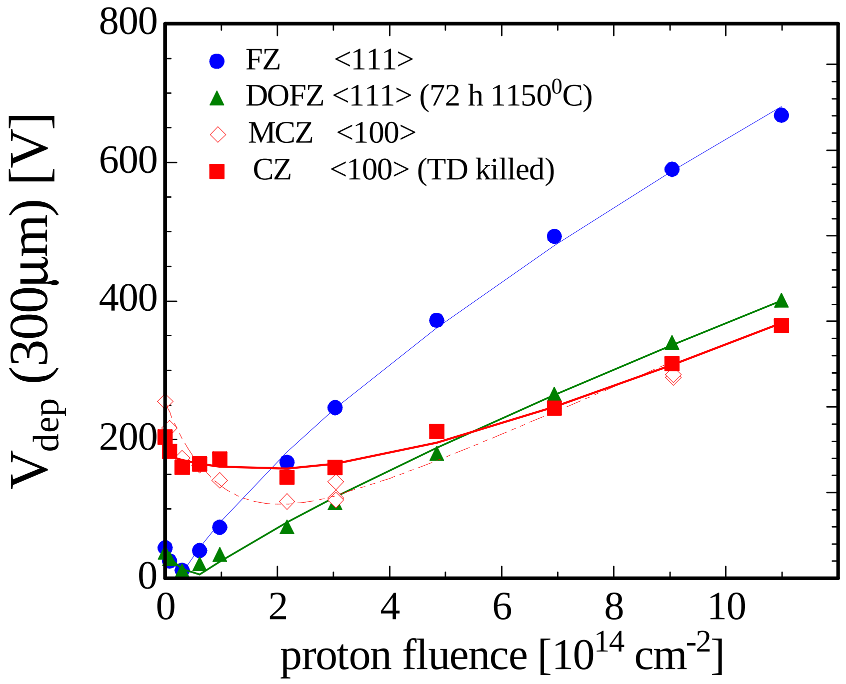
Abstract:
……. The effective impurity density decreases with fluence up to ~4x10^{13}/cm^2, but for greater fluences, it increases. **This may indicate the type conversion** of the bulk silicon ………

- M. Nakamura,…T. Kondo, "Radiation Damage Test of Silicon Multistrip Detectors", Nucl. Instr. Meth. A270(1988)42, using the irradiated sensor by 800 GeV protons

Evolution of depletion voltage

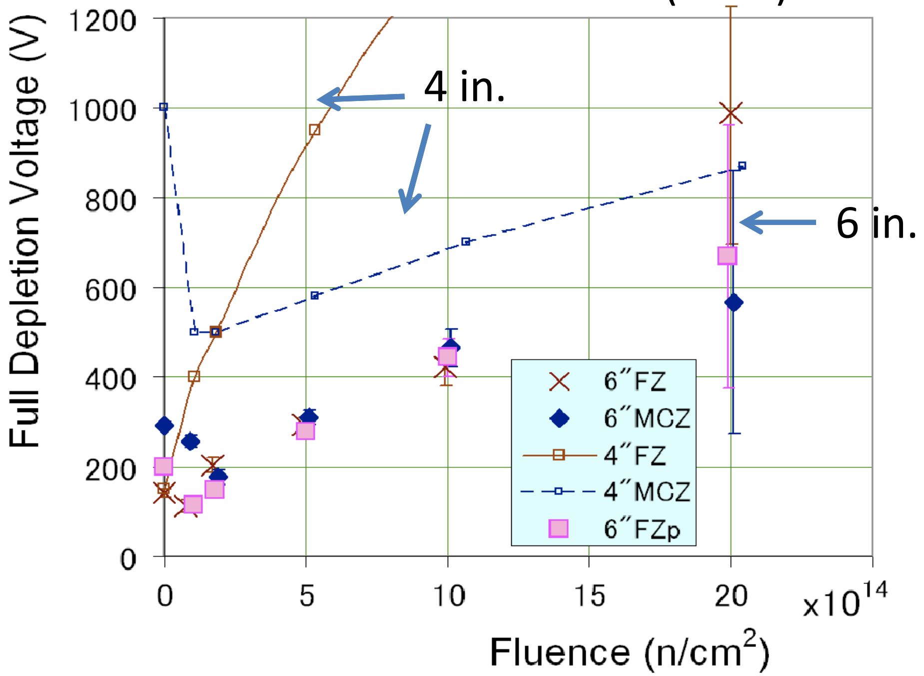
- A thorough study of the radiation damages has been made by RD50 collaboration. But, also done elsewhere…
  - E.g. Michael Moll, Ph.D Thesis, 1999.

24 GeV/c proton irradiation
(n-type silicon)



70 MeV proton irradiation
(p-type silicon)

K. Hara et al.,
IEEE Trans. Nucl. Scie. 56 (2009) 468

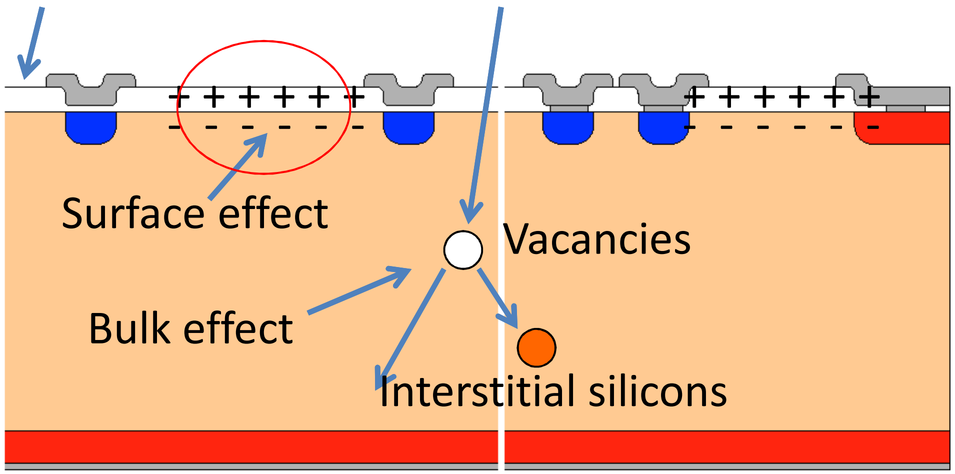


4 in.

6 in.

6 in. FZ is as same as DOFZ or MCZ

Radiation damage – Surface effect



SiO_2 passivation

Incident particles

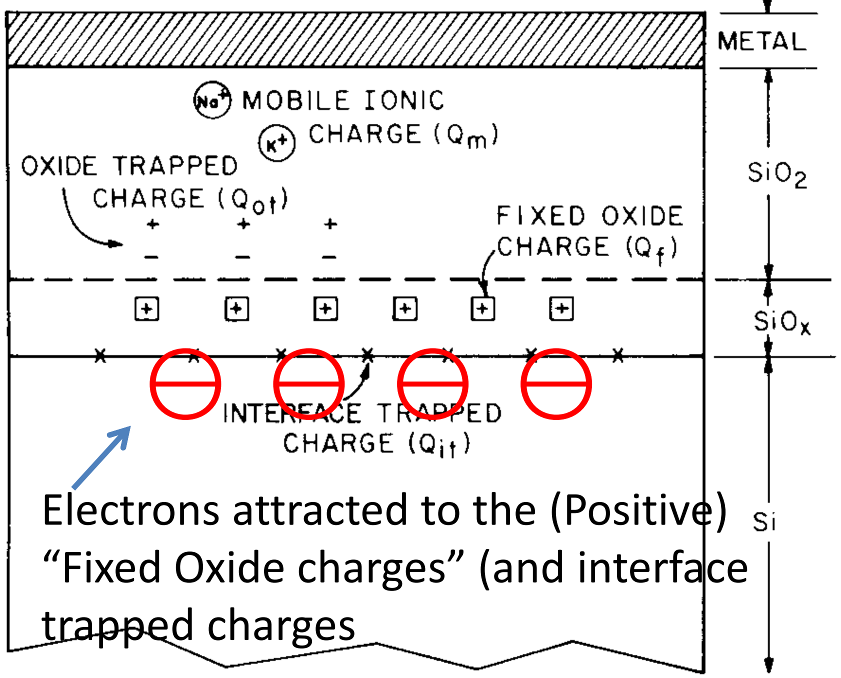
Surface effect

Vacancies

Bulk effect

Interstitial silicons

S.M. Sze, Physics of Semiconductor Devices, 2nd ed., p380



Electrons attracted to the (Positive) "Fixed Oxide charges" (and interface trapped charges

- The interfacial region is a single-crystal silicon followed by a monolayer of SiO_x, incompletely oxidized silicon, then a strained region of SiO_2 roughly 10-40 A deep.
- Interface trap (Q_{it}) and fixed oxide charges (Q_f) exist, (as a consequence of thermal oxidation)
- Oxide trapped charges (Q_{ot}) can be created by radiation and moved to be Q_f.
- **Q_f are "positve" and attract electrons in the Si-SiO_2 interface**.

High Voltage Operation

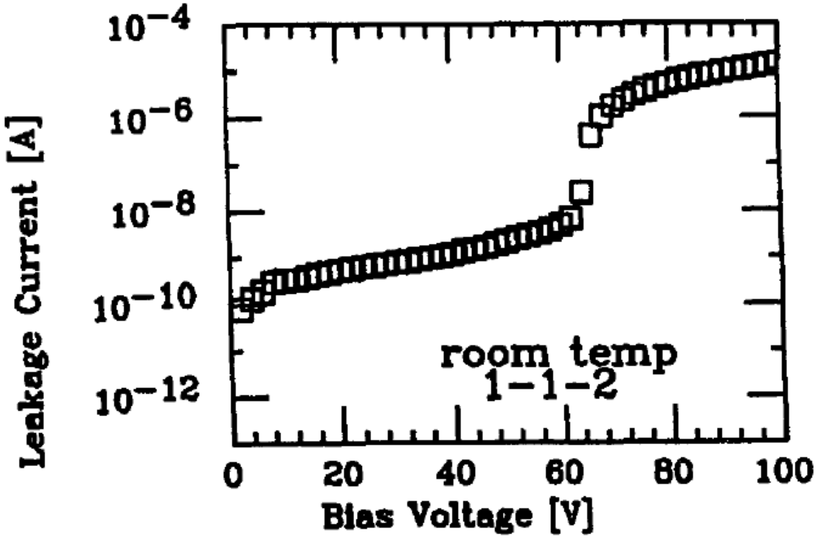
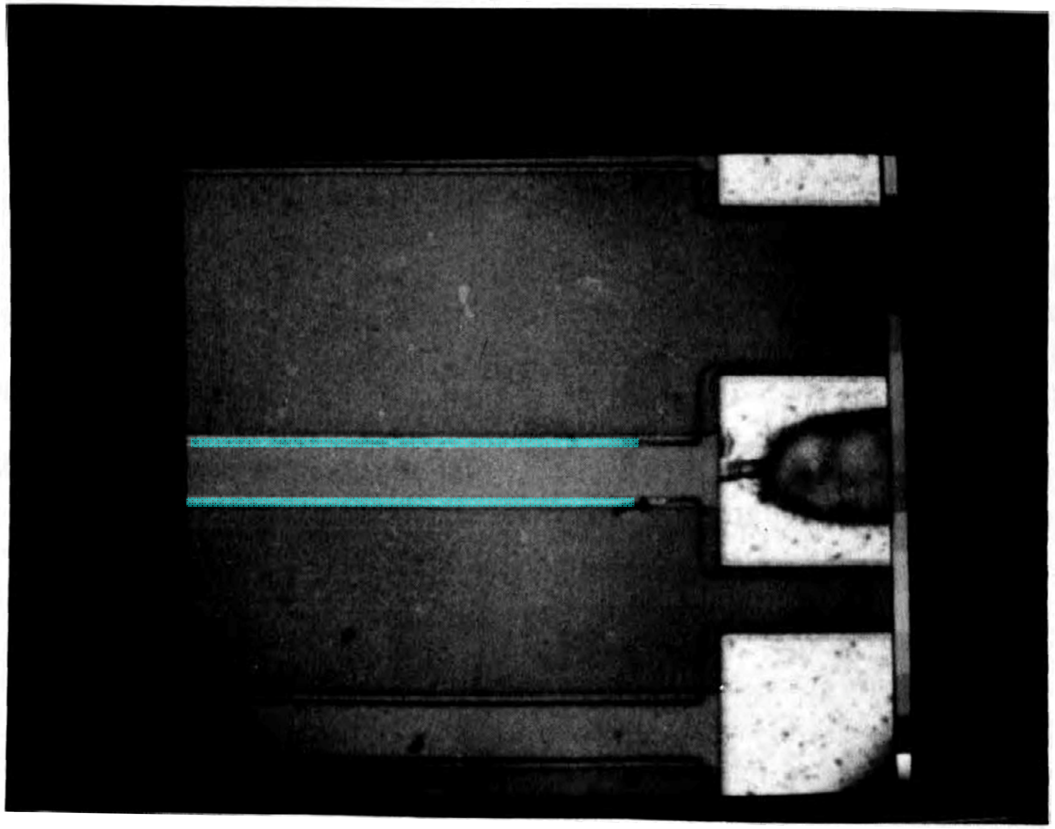


Fig. 1. Leakage current as a function of the bias voltage when the potential is across the integrated capacitor on the p-strip.



- To cope with the increase of full depletion voltage,
  - High bias voltage → High electric field → avalanche breakdown
  - *Breakdown field* ~ 30 V/µm in silicon
- 1st visualization with an infra-red sensitive camera

T. Ohsugi, Y. Unno, et al., Nucl. Instr. Meth. A432 (1994) 22

Understanding High Field

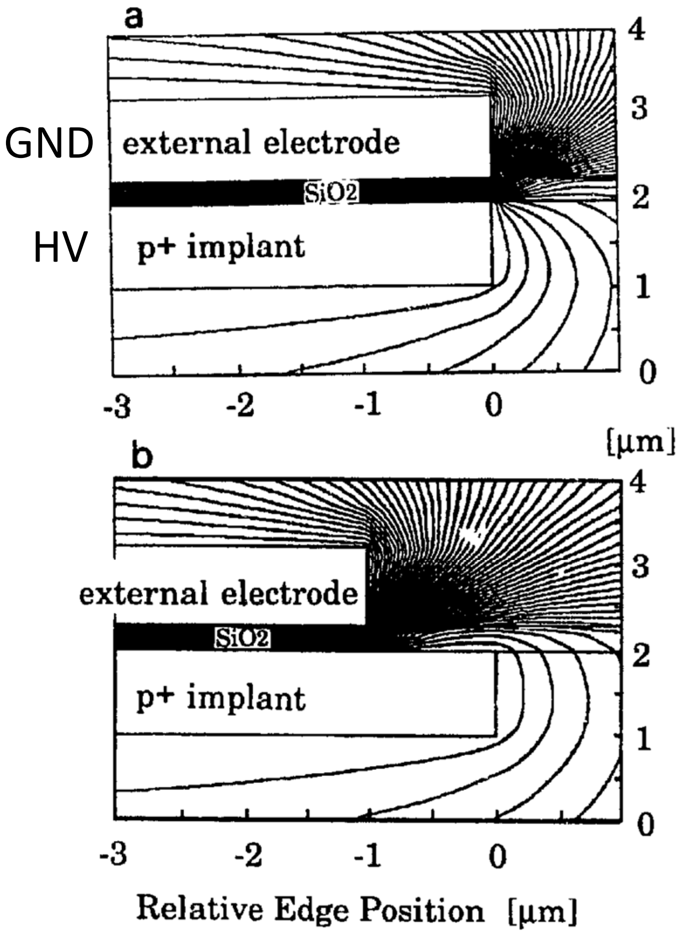


Fig. 4. Equipotential lines calculated around the edge of the implant and the external electrode. (a) is for the geometry of the edge of the external electrode placed just on the edge of the implant. (b) is for the geometry of the edge of the external electrode stepped back by 1 μm from the edge of the implant.

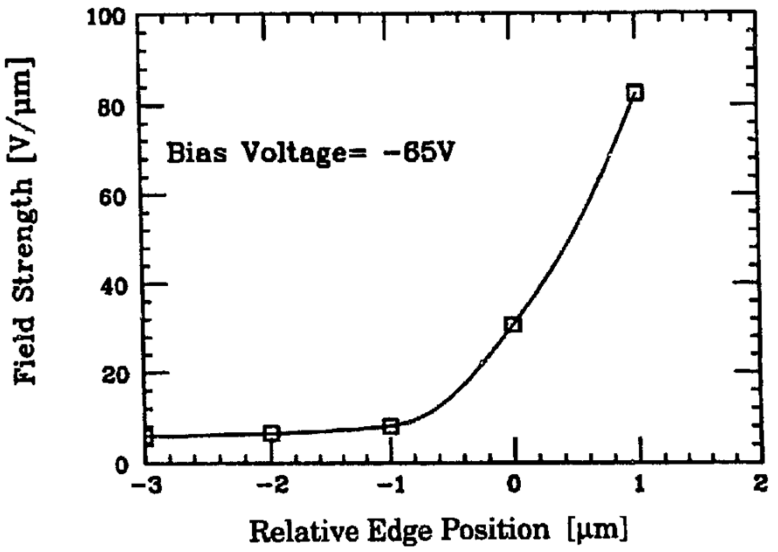


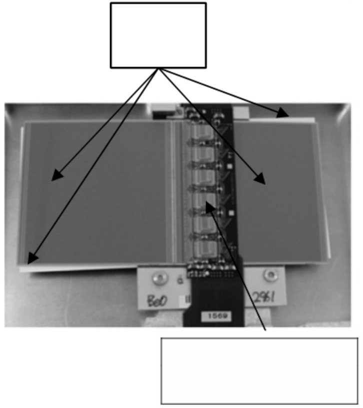
Fig. 5. The highest field strength calculated at around the implant is plotted as a function of the edge separation of the external electrode and the implant. The positive value of the horizontal axis means that the external electrode overhangs on the implant.

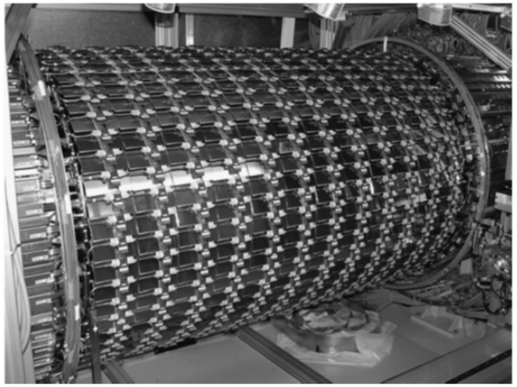
- With a simple electric field calculation, we could understand where the breakdown occurred.

T. Ohsugi, Y. Unno, et al., Nucl. Instr. Meth. A432 (1994) 22

ATLAS98 Strip Sensor for LHC

A.Ahmad et al., Nucl. Instr. Meth. A578 (2007) 98-118





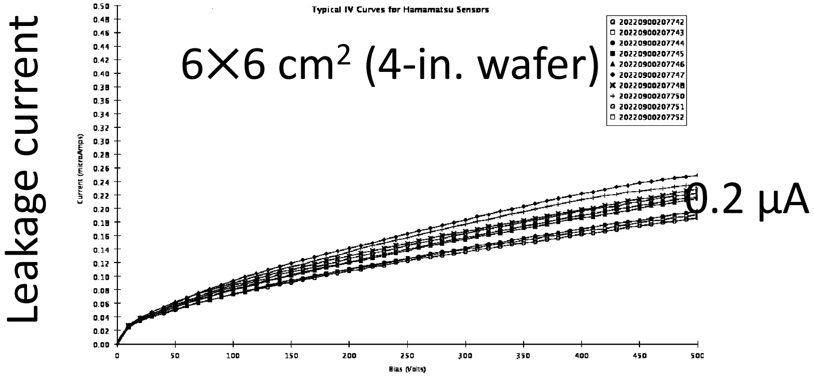
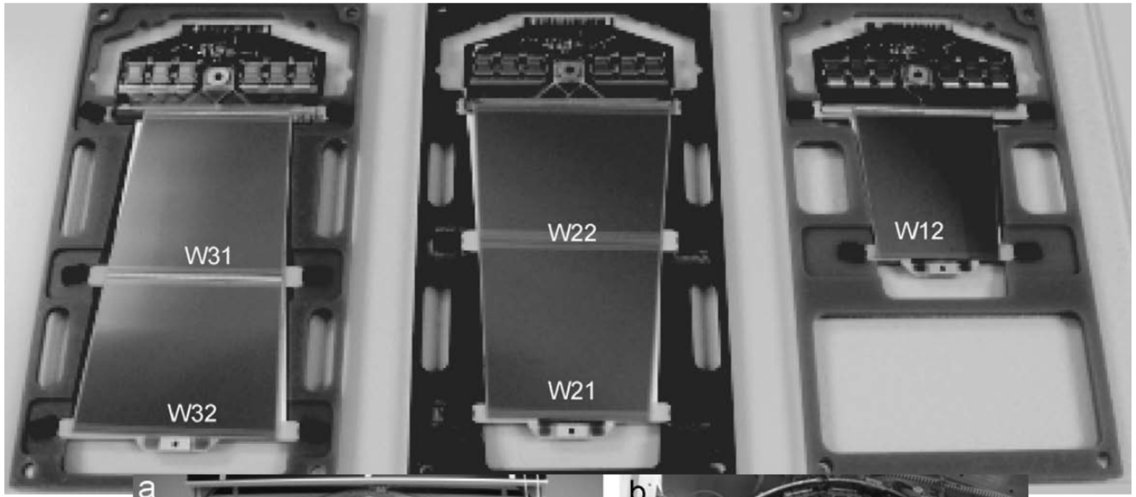
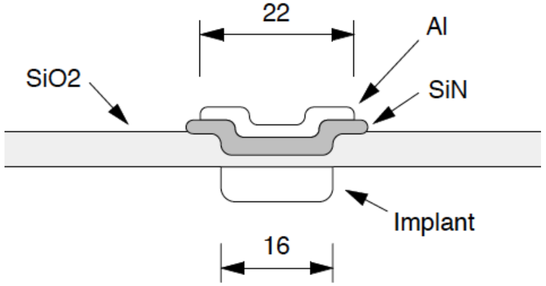
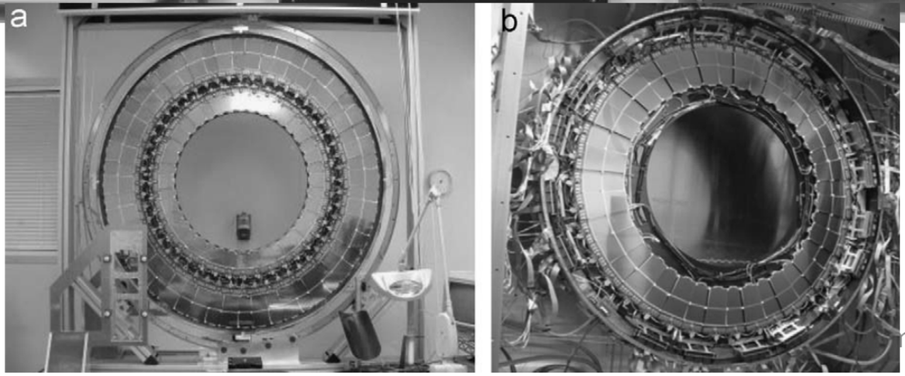


Fig. 12. Typical I–V curves (current in mA versus voltage) of Hamamatsu barrel sensors, measured at 20 1C.





ATLAS98 wide-metal



- Strip structure
  - Wide metal for p+-implant at GND
- Wafer orientation
  - <111> and a fraction with <100>

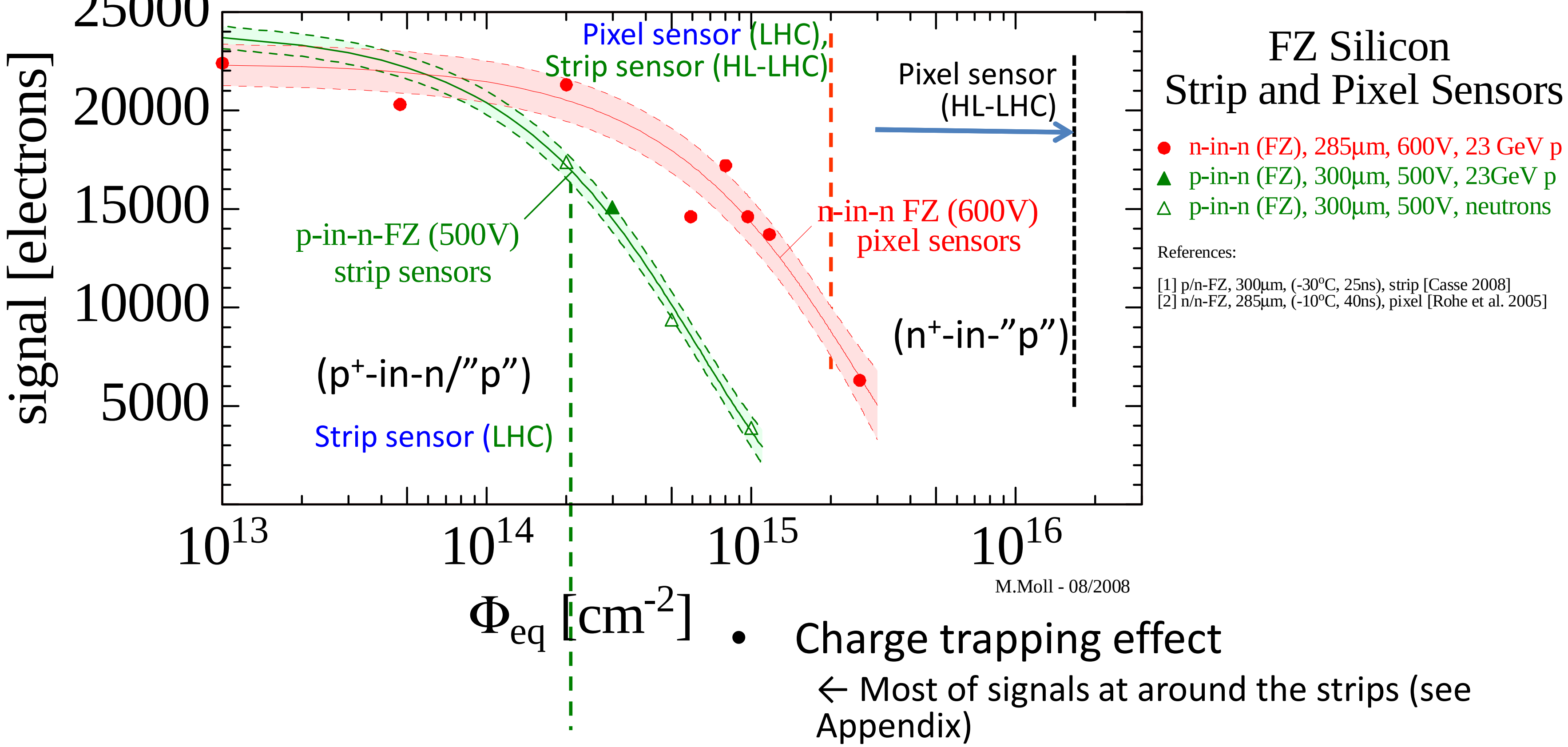
Choice of LHC Experiments

Experiment	Type	Wafer
ALICE pixel	p^+-in-n	standard FZ
ATLAS pixel	n^+-in-n	oxygenated
ATLAS strips	p^+-in-n	standard FZ <111> (some <100>)
CMS pixel	n^+-in-n	standard FZ
CMS strips	p^+-in-n	standard FZ <100>
LHCb VELO	n^+-in-n	standard FZ

- Compromise between the radiation tolerance and the cost
- p^+-in-n:
  - single-side process (lower cost)
  - requires full depletion, high voltage operation
- n^+-in-n
  - double-side process (higher cost)
  - works under partial depletion, less requirement for high voltage op.

High Voltage Operation at LHC (and HL-LHC)

RD50 collaboration,
ATLAS collaboration, ...



- Charge trapping effect

  ← Most of signals at around the strips (see Appendix)

- Depleted region
  - p$^+$-in-n → p$^+$-in-p (requires "full depletion")
  - n$^+$-in-n → n$^+$-in-p (works under "partial depletion")

The dawn of “n^+-in-p” Sensor

S. Terada, Y. Unno, et al., Nucl. Instr. Meth. A383 (1996) 159-165

- A p-type sensor was developed for a cost-effective alternative to “n^+-in-n” sensor.

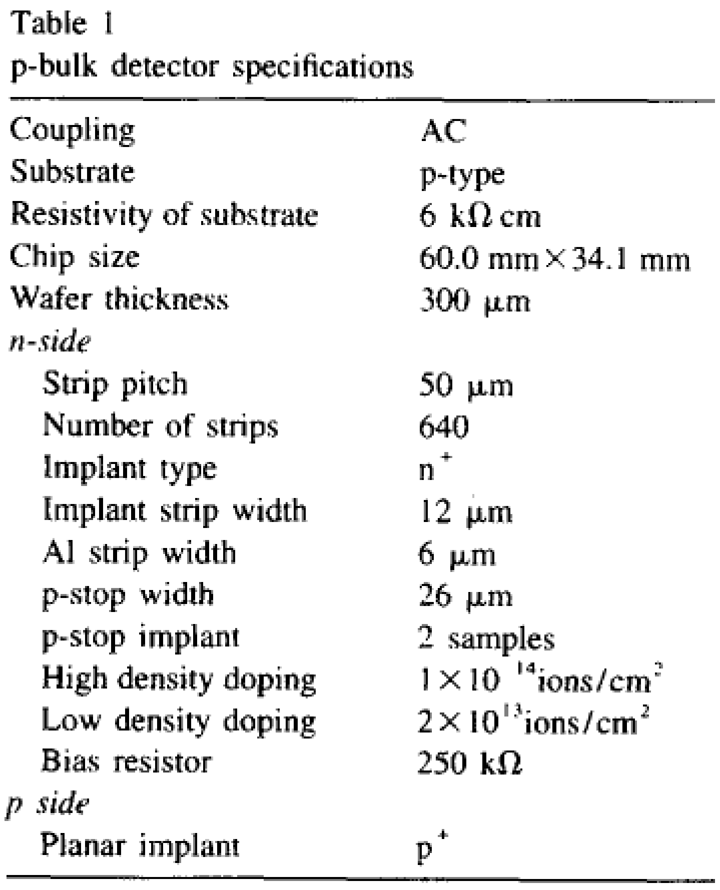


Table 1
p-bulk detector specifications

Coupling	AC
Substrate	p-type
Resistivity of substrate	6 kΩ cm
Chip size	60.0 mm × 34.1 mm
Wafer thickness	300 μm
n-side	
Strip pitch	50 μm
Number of strips	640
Implant type	n^+
Implant strip width	12 μm
Al strip width	6 μm
p-stop width	26 μm
p-stop implant	2 samples
High density doping	1×10^{14} ions/cm^2
Low density doping	2×10^{13} ions/cm^2
Bias resistor	250 kΩ
p side	
Planar implant	p^+

A hypothesis of “Acceptor removal” was proposed to explain the change of full depletion voltage along the fluence.

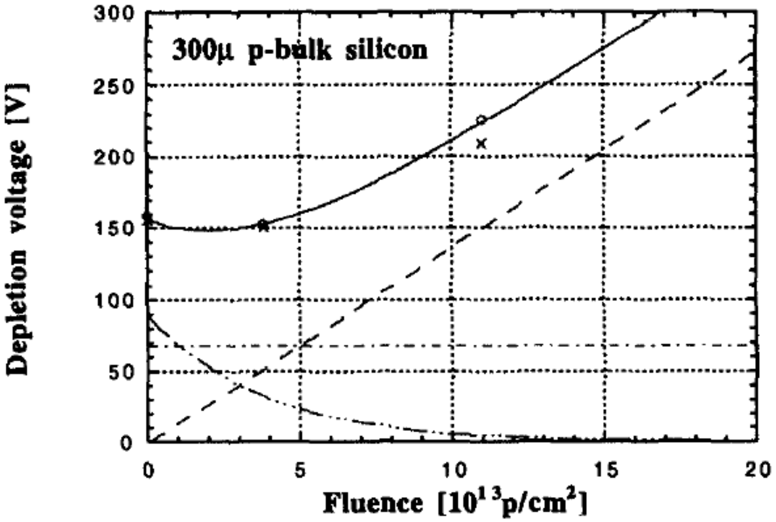
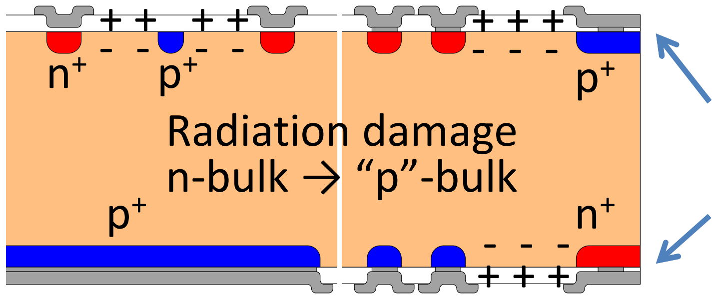


Fig. 8. Variation of the full depletion voltage of the p-bulk silicon strip detectors: data points (circle: high density p-stop, cross: low density p-stop), the curve (solid) combining the three hypotheses (acceptor creation (dashes), persistent acceptor component (dot–dash), and acceptor removal (double-dot–dash).

Cost-effective n^+-in-p planar sensor

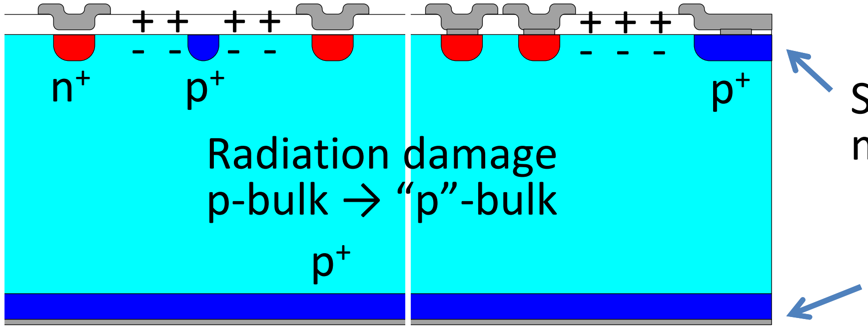
n^+-in-n



Double-side mask process

(LHC pixel sensors of ATLAS, CMS)

n^+-in-p



Single-side mask process

Diffusion process

(ATLAS baseline strip and pixel sensors for outer layers of HL-LHC)

- for heavy radiation environments
- Bulk radiation damage
  - one way to "p" type
- n^+ readout
  - p-n junction allowing "partial" depletion
- Special in n^+ readout
  - conductive layer in the surface
    - ~MΩ/square
    - due to the electrons attracted to the oxide trap/fixed charges
  - the electron layer must be
    - interrupted (p-stop), or
    - cancelled (p-spray)

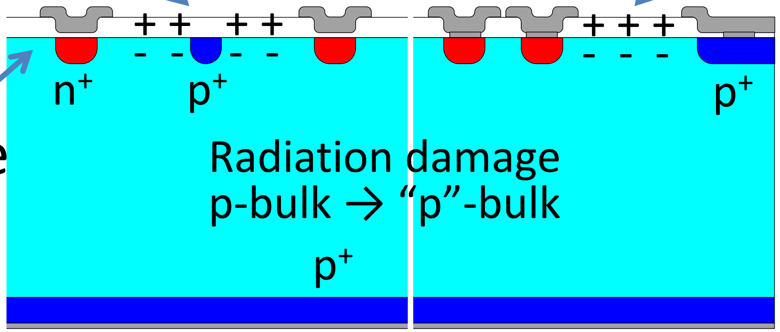
n$^+$-in-p sensors for HL-LHC

- n$^+$-implant isolation with p-stop structure.
- Operable to 1000 V bias voltage.
  - Suppressing "microdischarge" breakdown up to ~1000 V
- How?
  - Those 1, 2, 3, backed by 4
  - In addition, protection against beam splash: punch-through-protection (PTP) structure

② Optimization of p-stop structure

③ Optimization of edge width

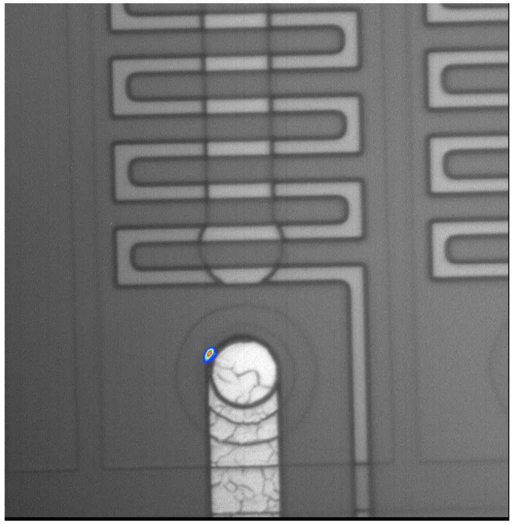
n-in-p

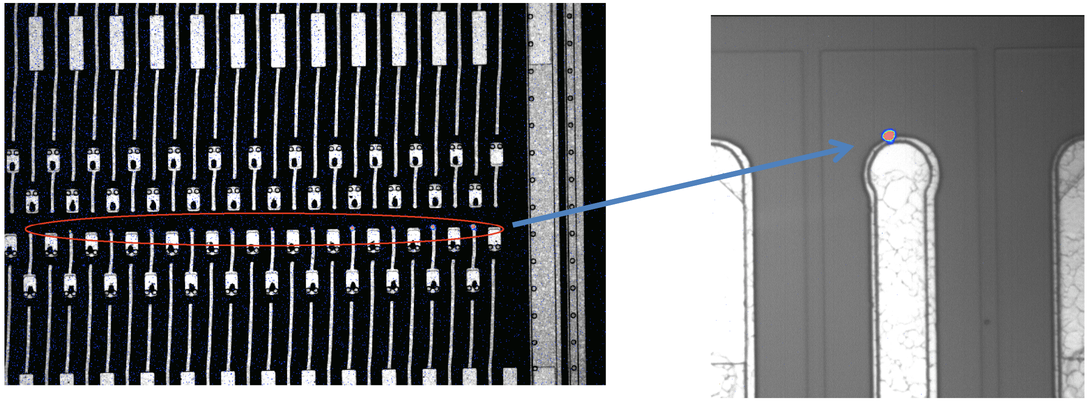


① Hardening the implant edges

④ Understanding the physics
← Technology CAD (TCAD) simulation

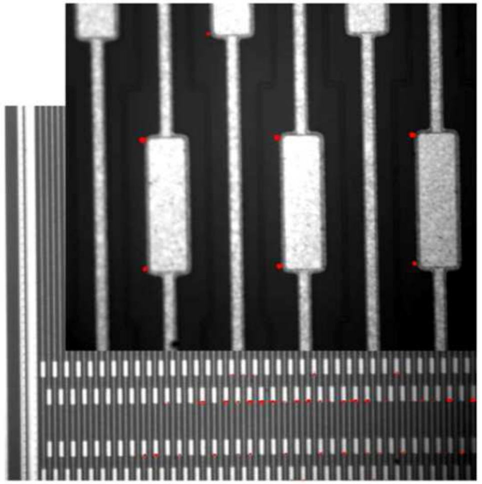
High Voltage Operation-Hot spot

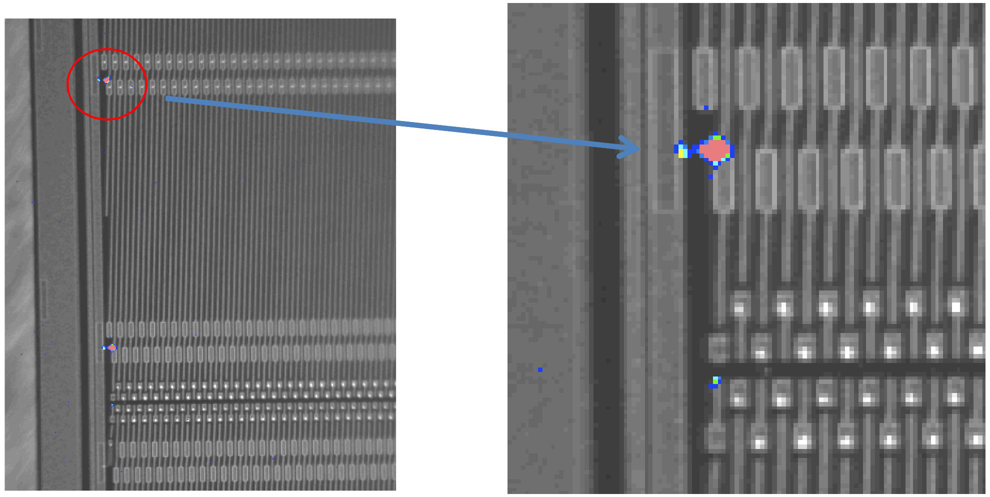




Seg4 の DC PAD ｽﾄﾗｲﾌﾟ 先端で発光（×5）

Seg4 の DC PAD ｽﾄﾗｲﾌﾟ 先端で発光（×100）





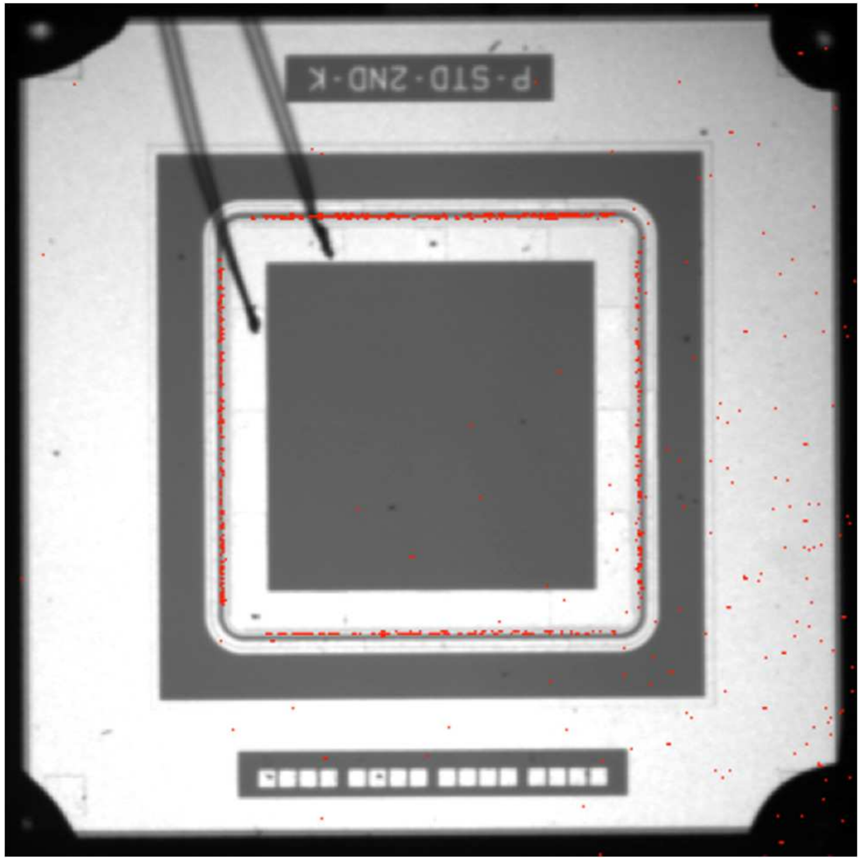
の AC PAD 角と Seg4 の DC PAD ｽﾄﾗｲﾌﾟ 先端で発光（×0.8）

Fig. 9. Hot spots observed at AC pad corners. The AC pad is 60 μm wide and 200 μm long.

Y. Unno et al., Nucl. Instr. Meth. A Supplement 636 (2011) S24

Y. Takahasi et al., http://dx.doi.org/10.1016/j.nima.2012.04.031

Microdischarge after Irradiation

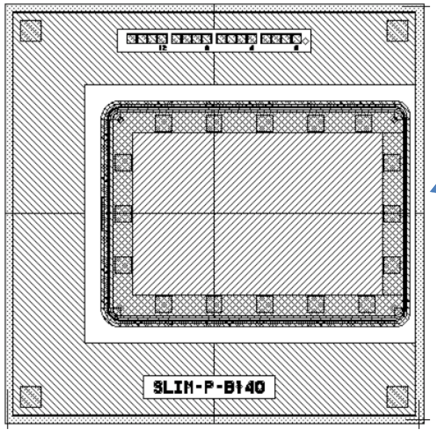


CYRIC proton irradiated
$1 \times 10^{14}\ n_{eq}/\text{cm}^2$
10 uA at 2000 V
-15 ° C

S. Mitsui et al.,
Nucl. Instr. Meth. A699 (2013) 36-40

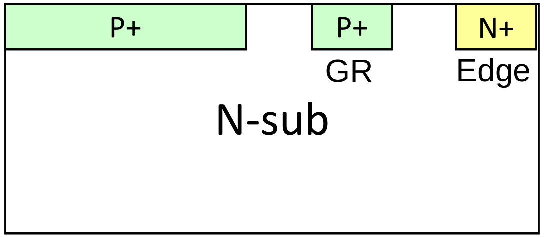
- Hot electron images confirm that
  - hot spots were observed first at the edge of the bias ring, and then at the inside of the edge metal.
  - the highest electric field is at the bias ring (n^+ implant), not at the edge ring (p^+ implant).

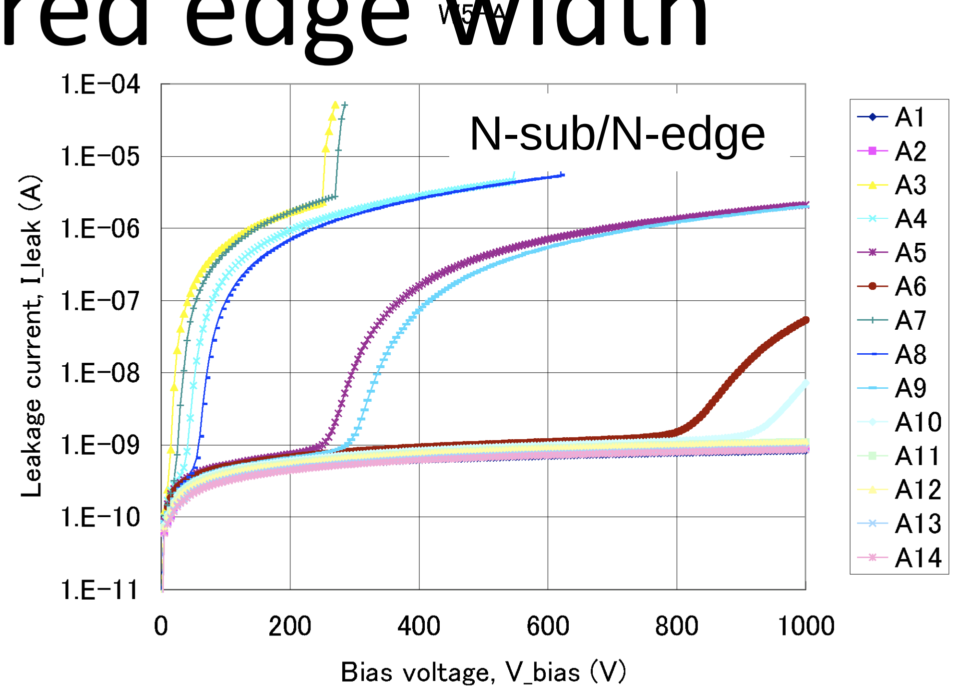
Study of required edge width

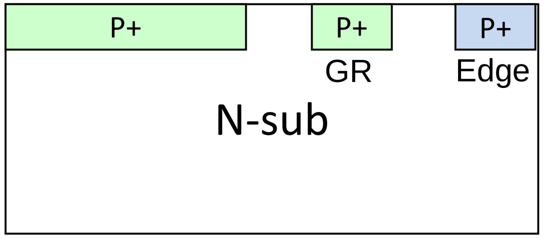


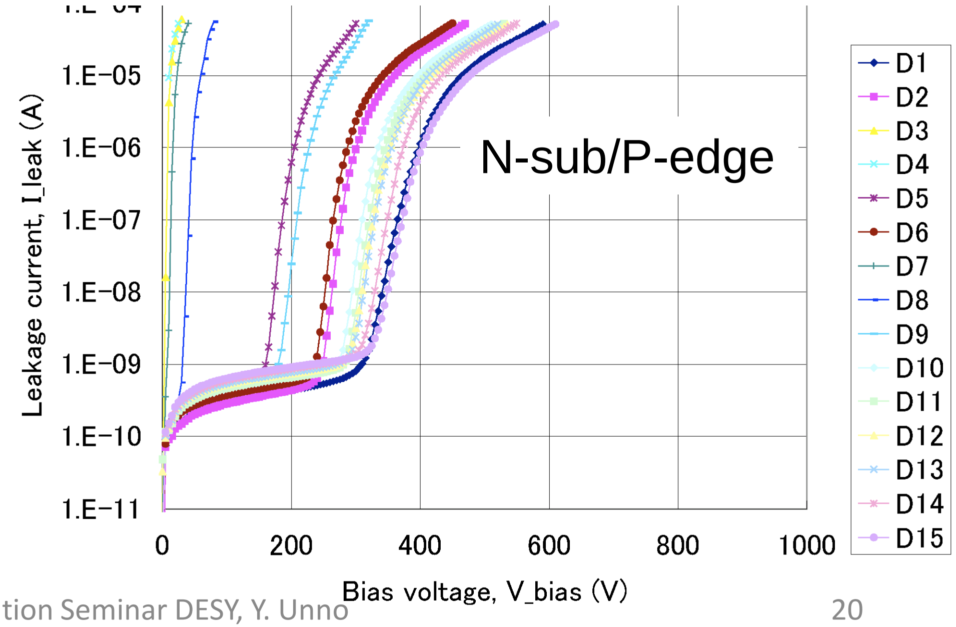
Width varied at one edge

- Results are from N-type wafer
- Thickness (as is, thinned)
  - 320 (W5), 200 (W7,13) µm
- Edge implantation
  - N+ or P+

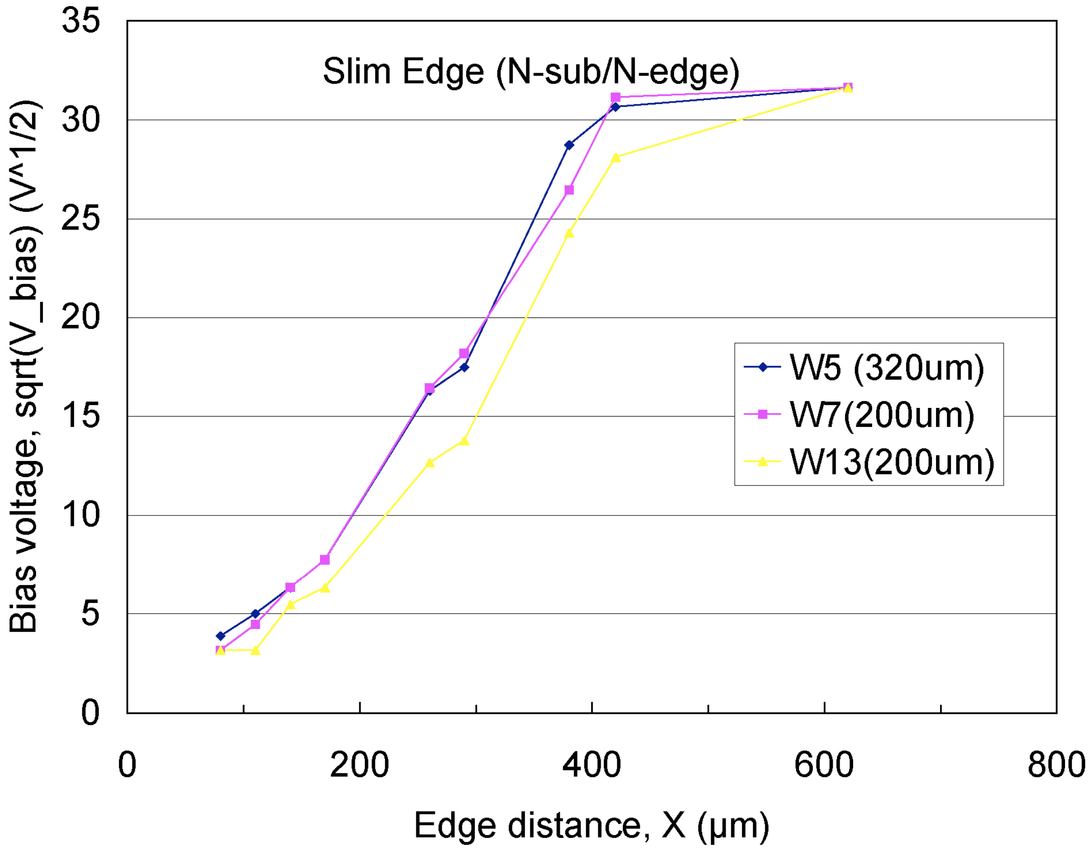


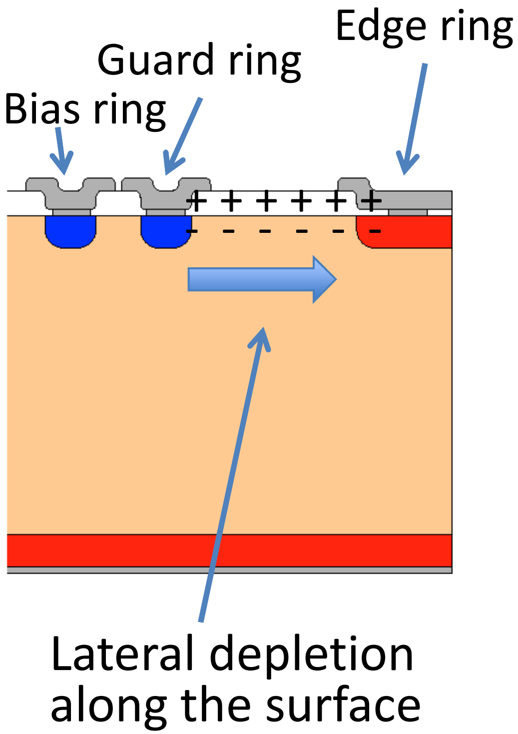






Underlying physics of the edge width





- Square root of V_bias is linearly dependent on the edge distance
  - Reflecting the depletion along the surface
- Distance can be ≤500 μm for the bias voltage up to 1 kV
- … Different story if the side wall is implanted e.g., - active edge

Required width after Irradiation

S. Mitsui et al, NIMA 699 (2013) 36-40

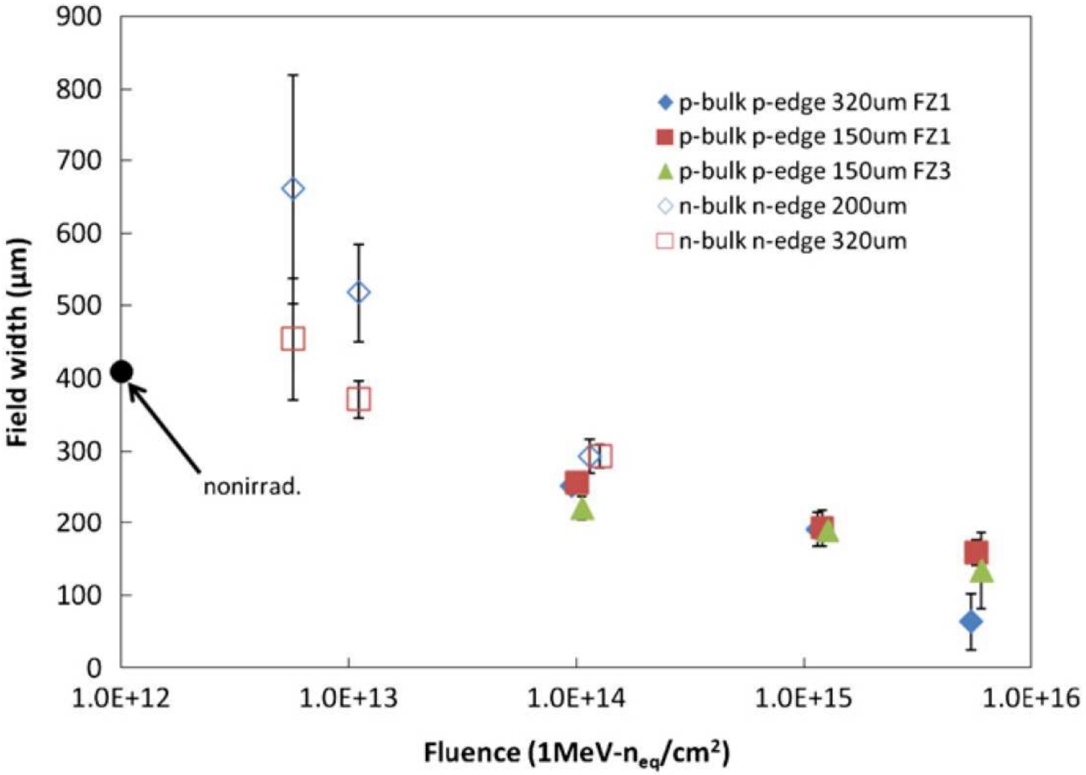
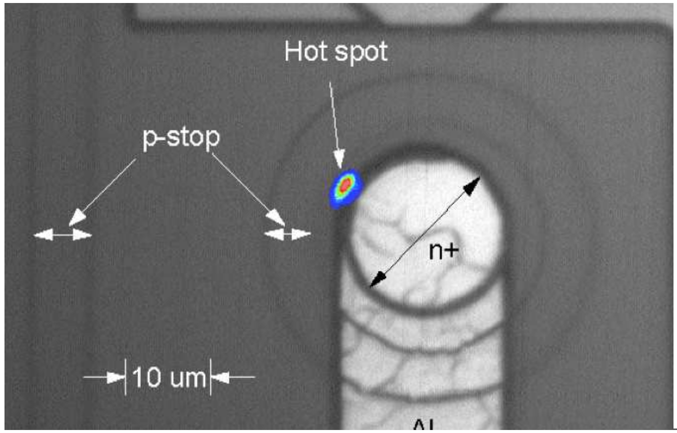


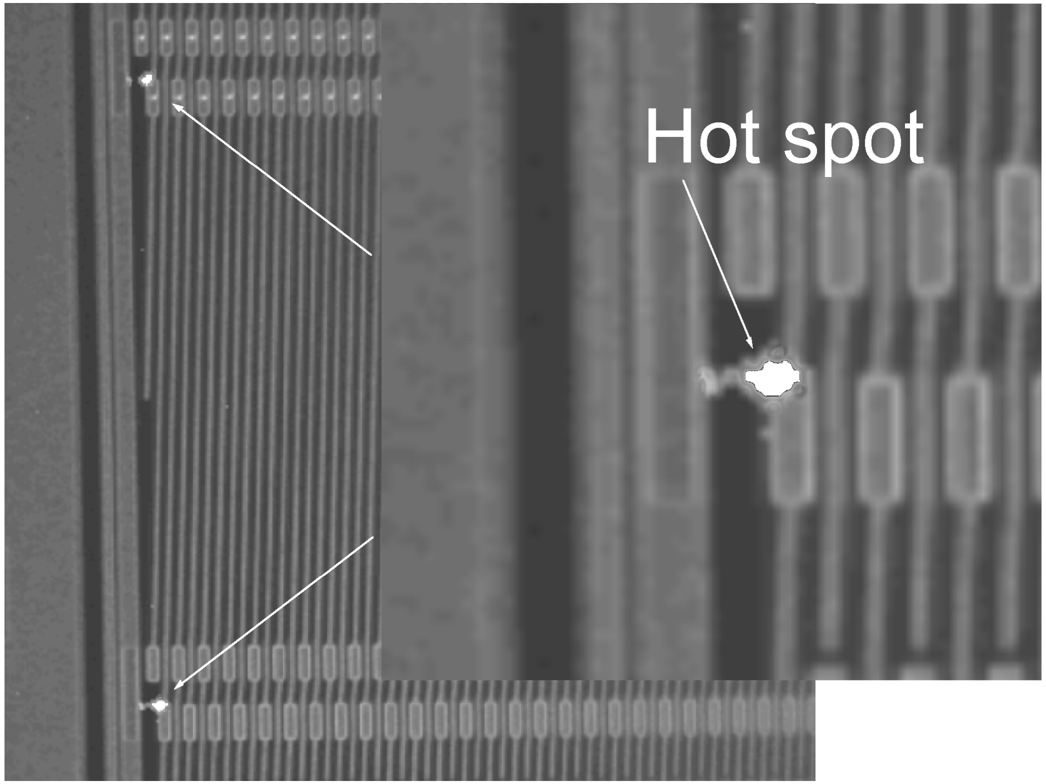
Fig. 5. Fluence dependence of field width hold up to 1000 V.

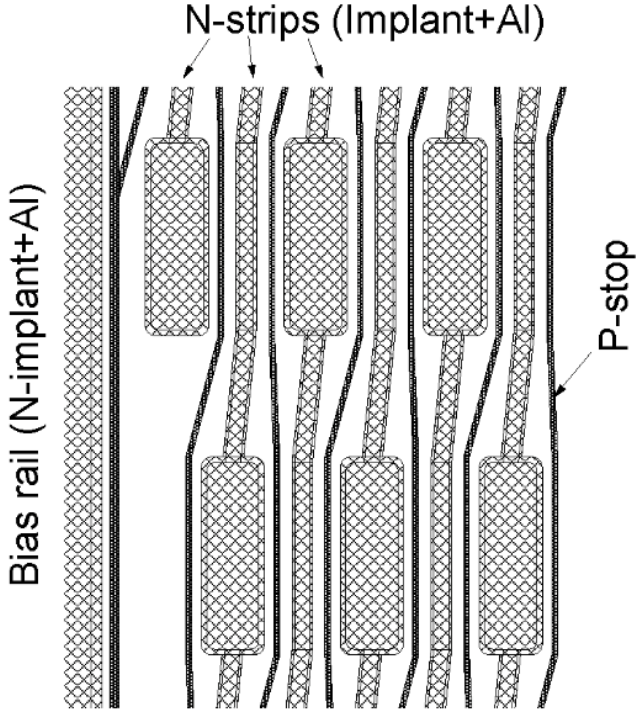
- Required width is ~450 µm to hold 1000 V.
  - At around 1x10^{13}, the required edge space is more than 450 µm, but also the depletion voltage is decreased less than that of non-irrad. and anyway it is much less than 1000 V.
  - At higher fluences, the required width is less than that of the non-irrad.

P-stop between n$^+$-implants



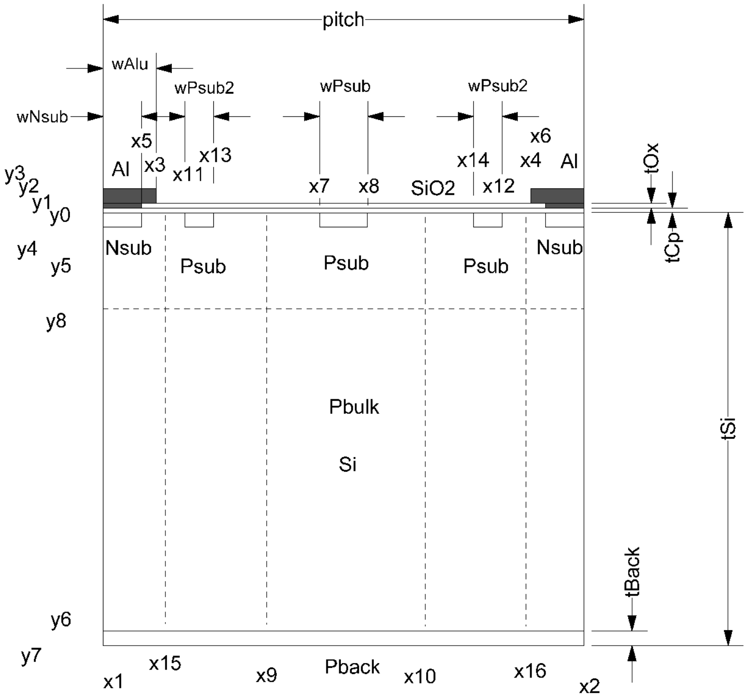
- Problems - Hot spots
  - IR image overlaid on visual image
  - Microdischarge = Onset of leakage current
- Optimization of the structures to reduce the electric fields?

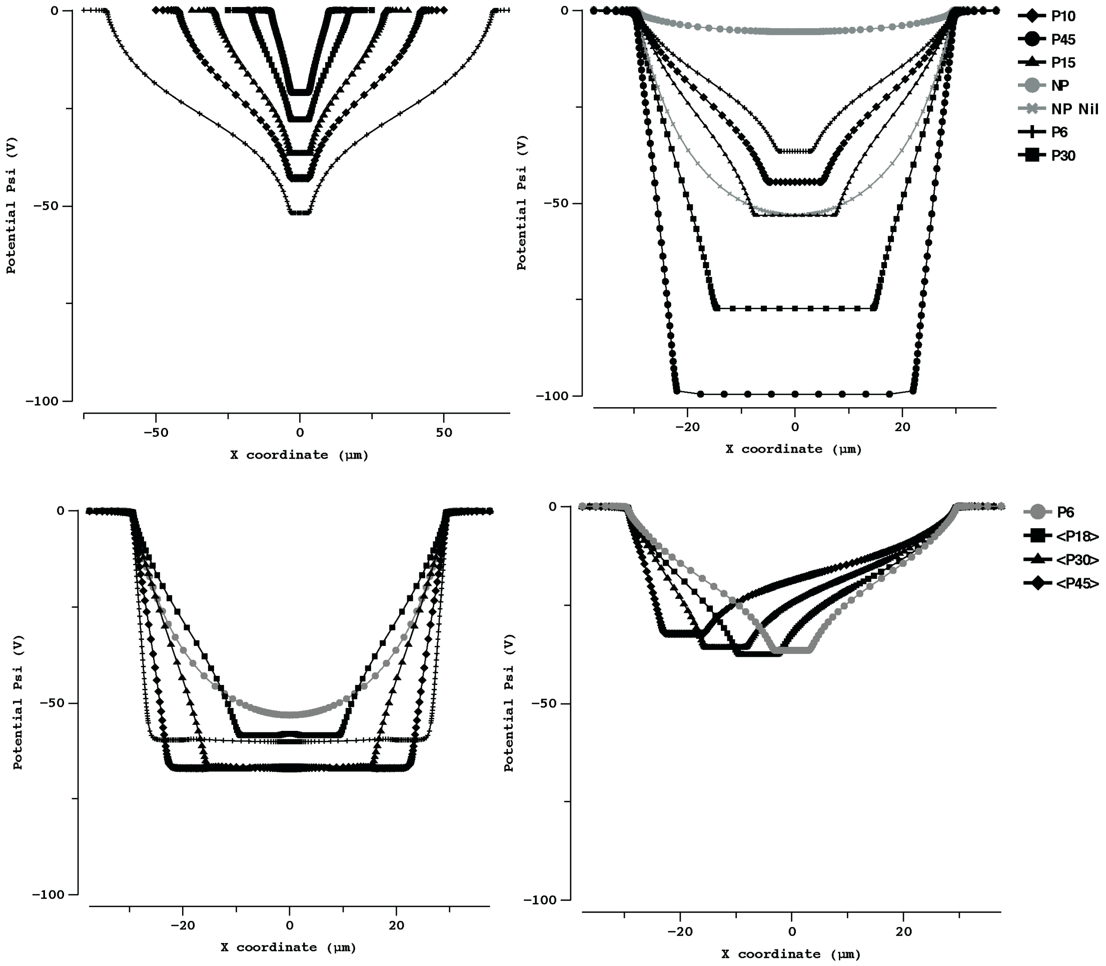




P-stop Structures Optimization

- TCAD simulations

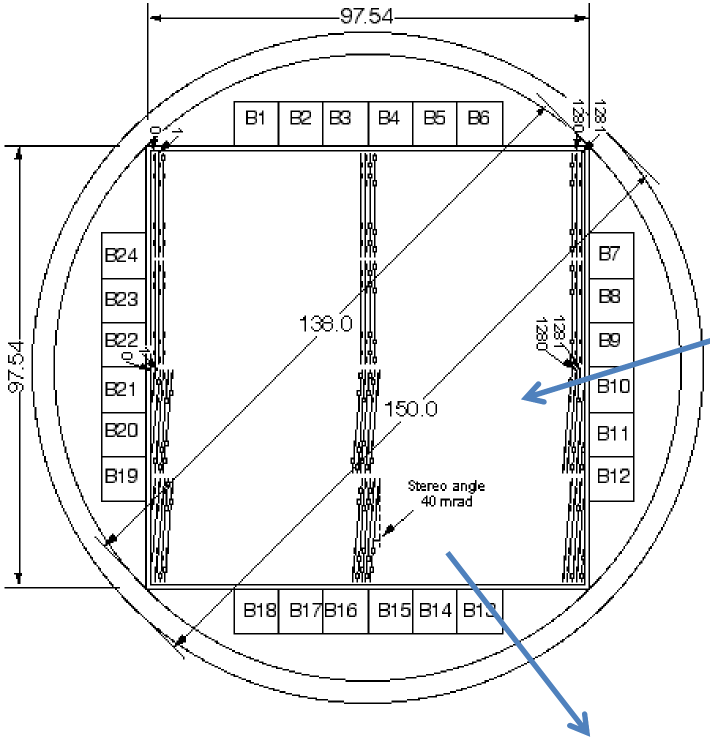




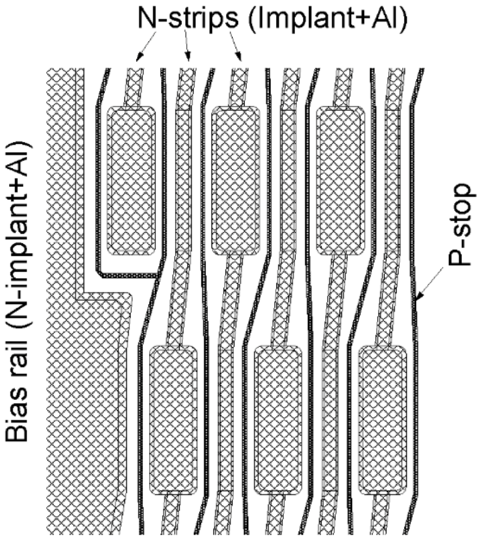
Y. Unno et al., Nucl. Instr. Meth. A636 (2011) S118–S124

… and comparison with test structures

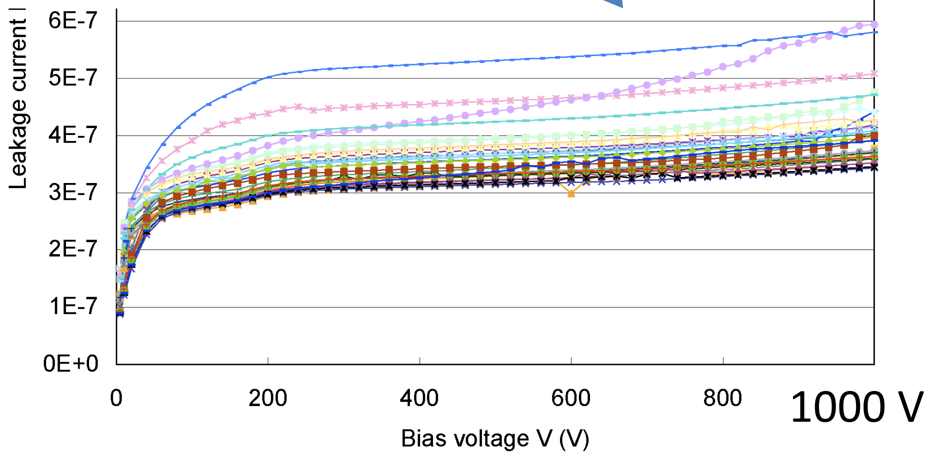
Optimization of the p-stop Structure



10 cm x 10 cm strip sensor in 6 in. wafer



Stereo strip section

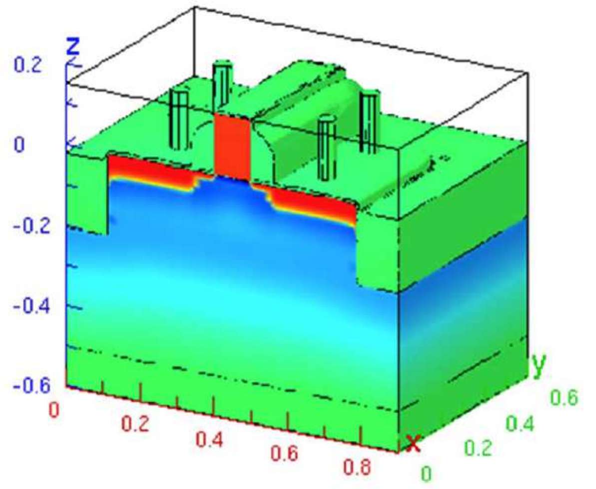


- P-stop
  - narrow
  - away from the n$^+$-implant maximally
  - at symmetric location
- n$^+$-implant
  - pitch not too narrow nor not too wide
- Once known, it is simple
  - like "Columbus's egg" (?)

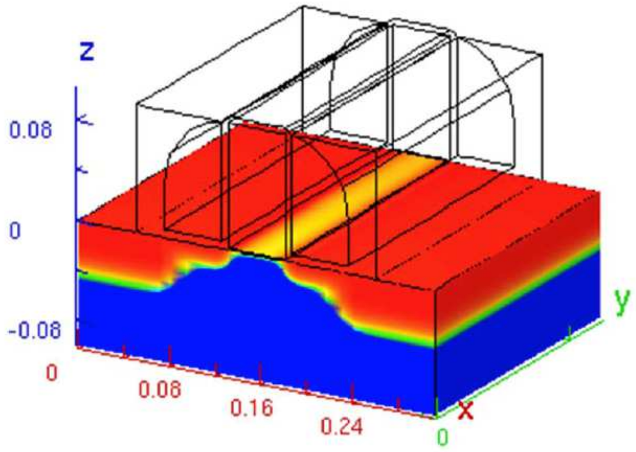
Technology CAD (TCAD)

- TCAD: Computer Aided Design for Semiconductor Technology
  - “Finite Element Analysis”, the numerical analysis method with modern computer, with “jungle” of semiconductor physics
- TCAD started to build the links between the
  - semiconductor physics and electrical behavior
  - to support circuit design
- Modern TCAD consists of
  - Process simulation, and
  - Device simulation
- Originated from the work of
  - Prof. Robert W. Dutton and his group at Stanford Univ.
- Widely used in semiconductor industry
  - to reduce the development cost and time
  - to understand the physics behind
    - that is even impossible to measure

MOS transistor



Process simulation



Device simulation

TCAD Simulation

- Semiconductor Technology Computer-Aided Design (TCAD) tool
  - ENEXSS 5.5, developed by SELETE in Japan
  - Device simulation part: HyDeLEOS
- (Effective) radiation damage approximation:
  - Increase of acceptor-like state → Effective doping concentration
  - Increase of leakage current → SRH model
  - Increase of interface charge → Fixed oxide charge

Bulk leakage current

After irradiation, the current increases as a function of fluence

$\Delta I / V \sim \alpha \times \phi (n_{eq}/cm^2)$

$\alpha \sim 4 \times 10^{-17}$ (A/cm) : damage constant

E.g.,

Volume = 75 µm x 1 µm x 150 µm = 1.13 x 10^{-8} cm^3

$\phi = 1 \times 10^{15}\ n_{eq}/cm^2$

$\Delta I \sim 45$ nA

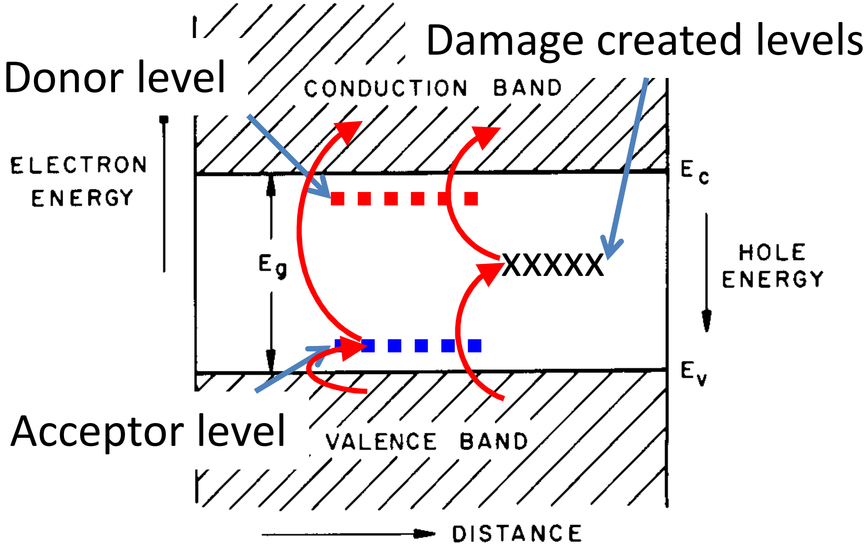


Fig. 6 Simplified band diagram of a semiconductor.

- Community has a view that
  - the leakage current increases with an introduction of levels near the middle of the forbidden band,
  - with the energy of band gap being half (of the full gap), the leakage current flows order of magnitude larger…
- Unfortunately, we have no freedom to change/add a program to the ENEXSS, but
  - we can simulate the leakage current by modifying the model parameters to an unrealistic world…

Shockley-Reed-Hall (SRH) Model

- Leakage current: SRH model
  - Generation-recombination of carriers (electrons and holes) by thermal effect
  - A_n, A_p : model parameters
    - Decrease them as though increasing temperature

$$U_{SRH} = \frac{n_i^2 - pn}{\tau_p\left(n + n_i\right) + \tau_n\left(p + n_i\right)}$$

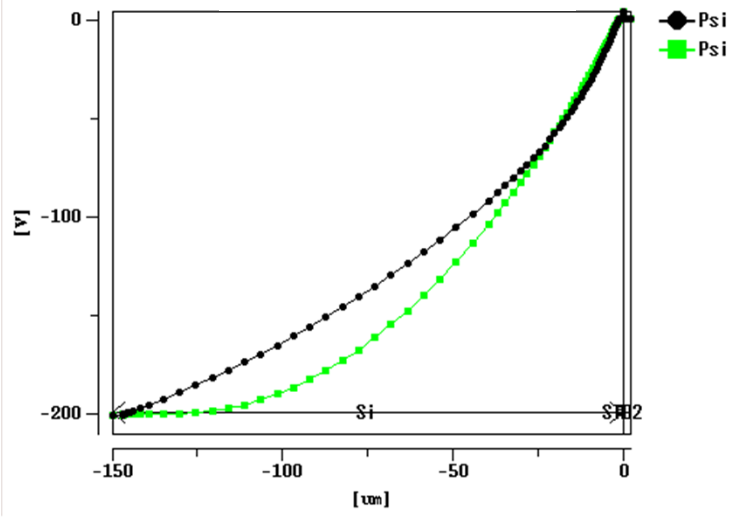
$$\tau_{n,p} = A_{n,p}\left(\tau_{\min}^{n,p} + \frac{\tau_{\max}^{n,p} - \tau_{\min}^{n,p}}{1 + \left(N / N_t^{n,p}\right)^{B_{n,p}}}\right)$$

n_i: intrinsic carrier density,

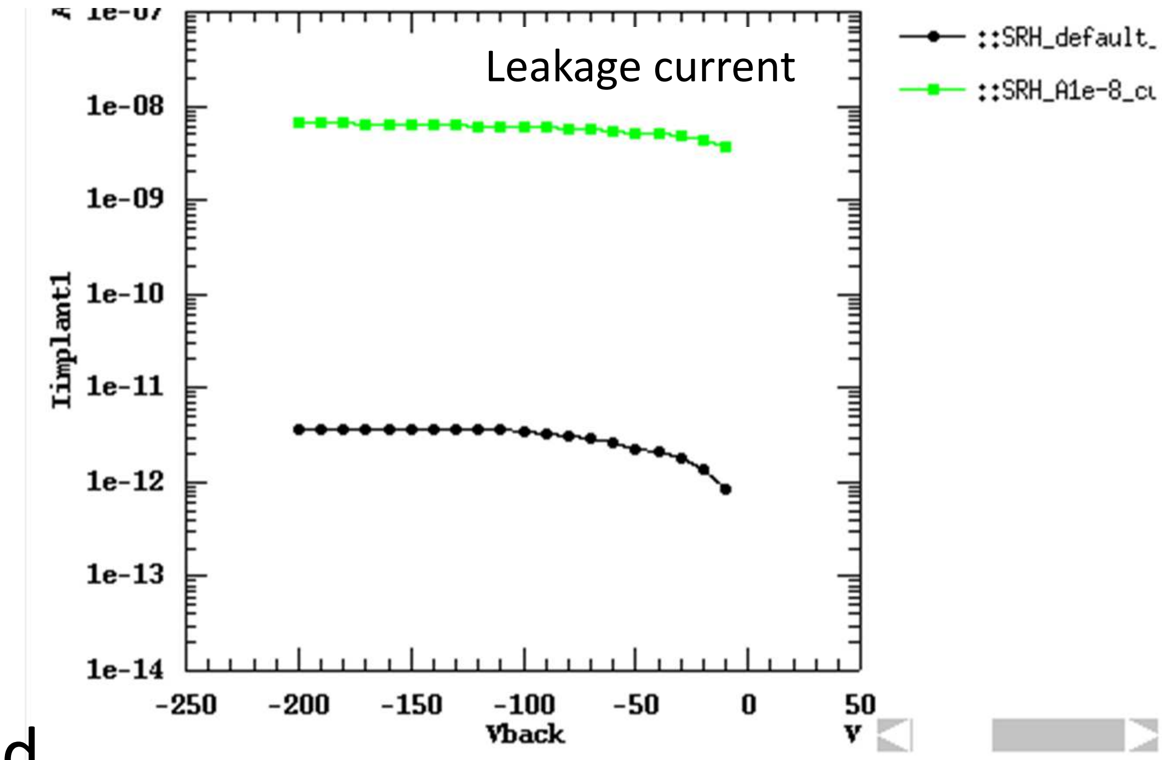
n, p: electron, hole carrier density

Radiation Damage Approximation

Potential in bulk

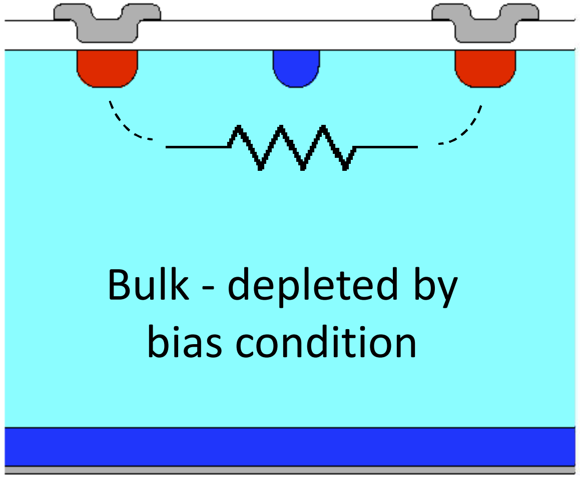


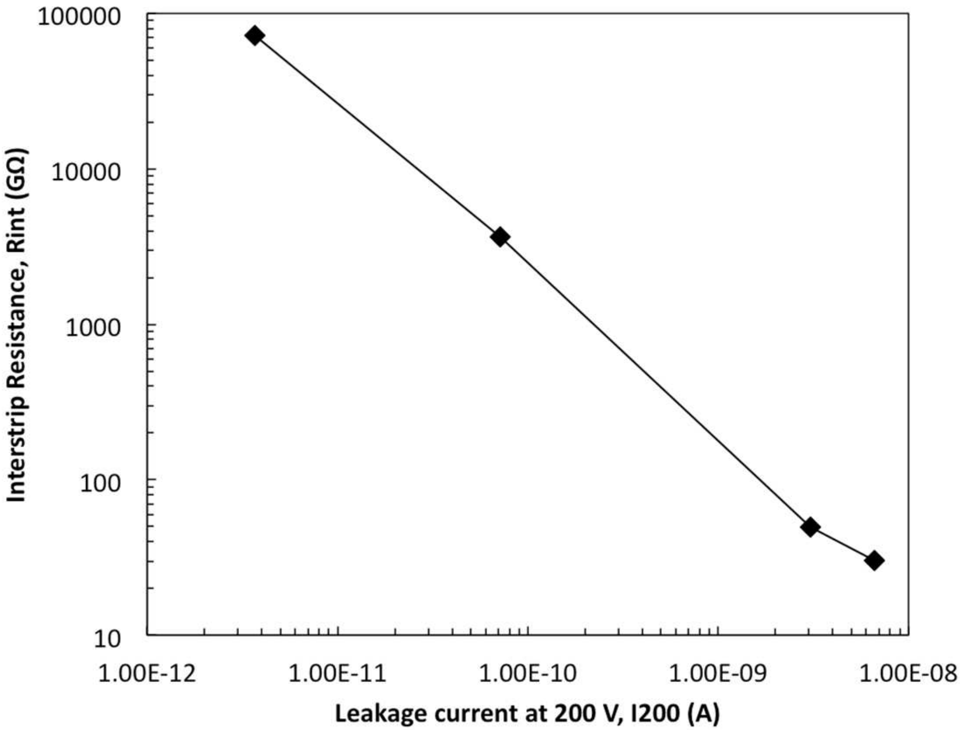
Backplane at 200 V


Leakage current

- Black: non-irrad.
  - N_{eff}=4.7 × 10^{12} cm^{-3}, A_n, A_p = 1.0
- Green: Irrad.
  - Increase of full depletion voltage, N_{eff}=1.5 × 10^{13} cm^{-3}
  - Increase of leakage current, A_n, A_p = 1 × 10^{-8}

Interstrip Resistance, R_{int}

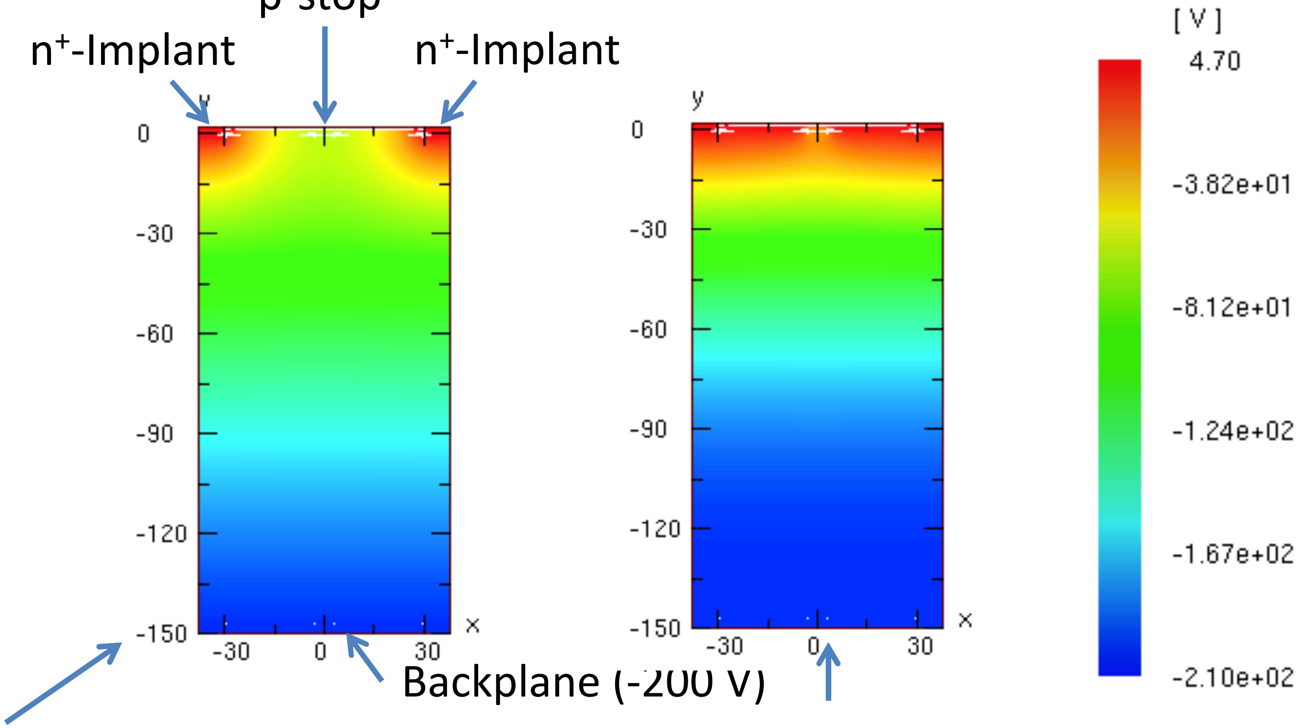




- Decrease of interstrip resistance after irradiation
  - is qualitatively explained by the increase of leakage current.
  - Other factors, the effective doping concentration nor the oxide interface charge, have not changed the interstrip resistance.
  - In retrospect, it is natural that the current is the other manifestation of the resistance.

Electric potential of p-stop
- Introduction of Si-SiO_2 interface charge -

Potential in bulk, 2D display


p-stop

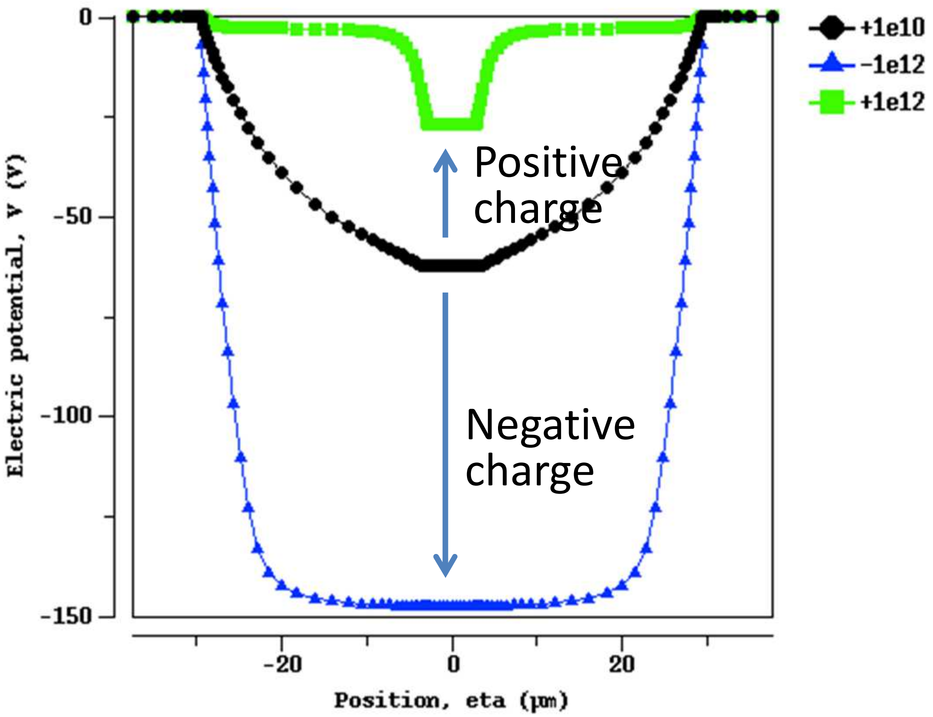
n^+-Implant

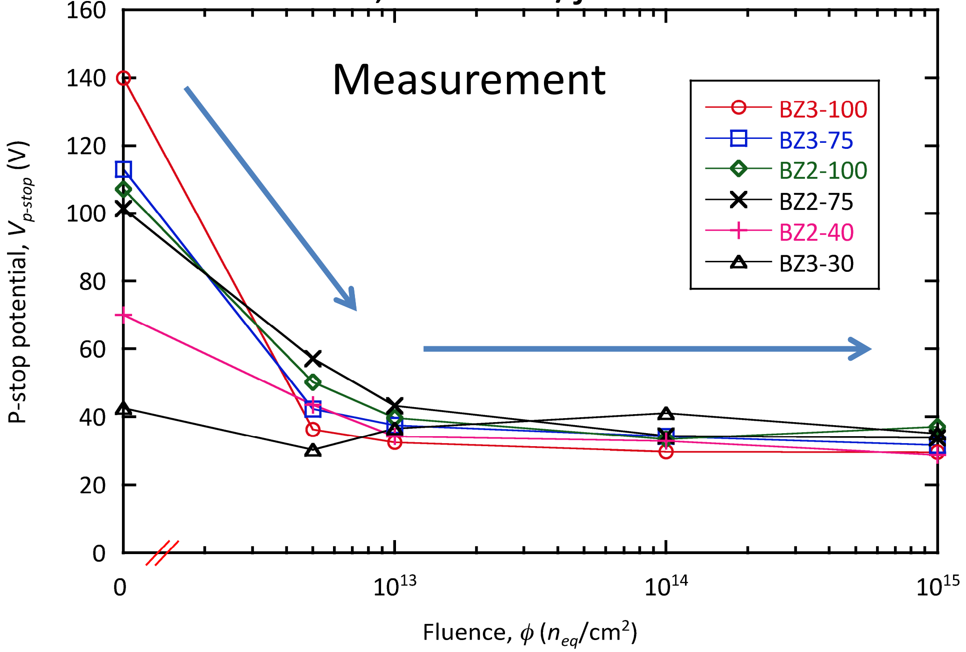
n^+-Implant

Backplane (-200 V)

- Non-irrad:
  - N_{eff}=4.7 × 10^{12} cm^{-3},
  - SRH A_n, A_p=1.0,
  - Fixed Oxide Charge =1 × 10^{10} cm^{-2}
- Irrad:
  - N_{eff}=1.5 × 10^{13} cm^{-3},
  - SRH A_n, A_p=1 × 10^{-8} ,
  - Fixed Oxide Charge =1 × 10^{12} cm^{-2}

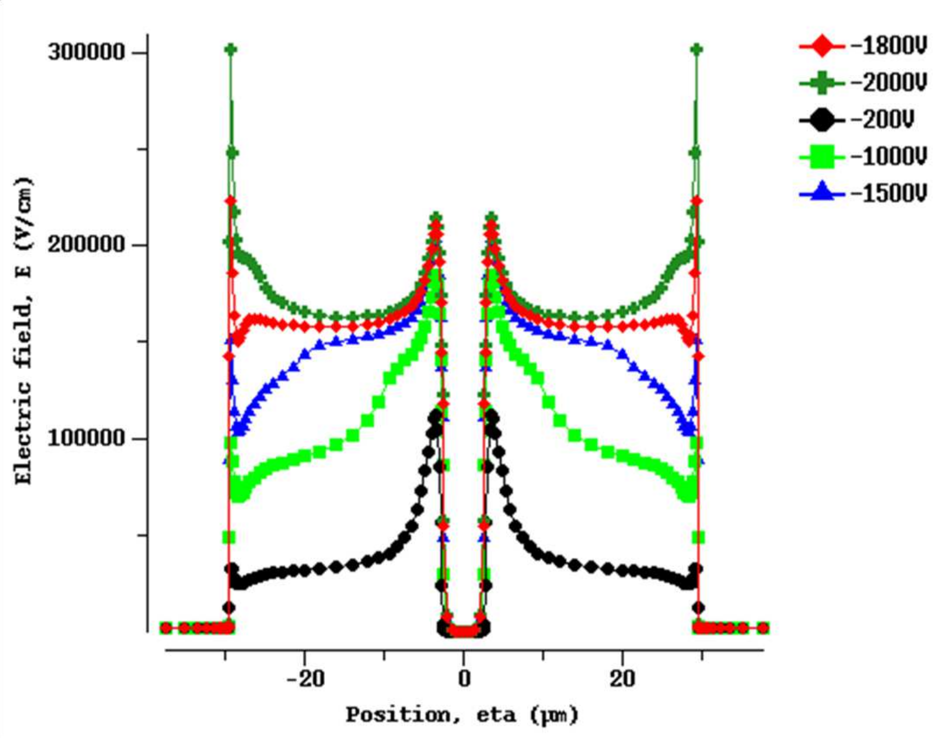
Electric Potential between Strips

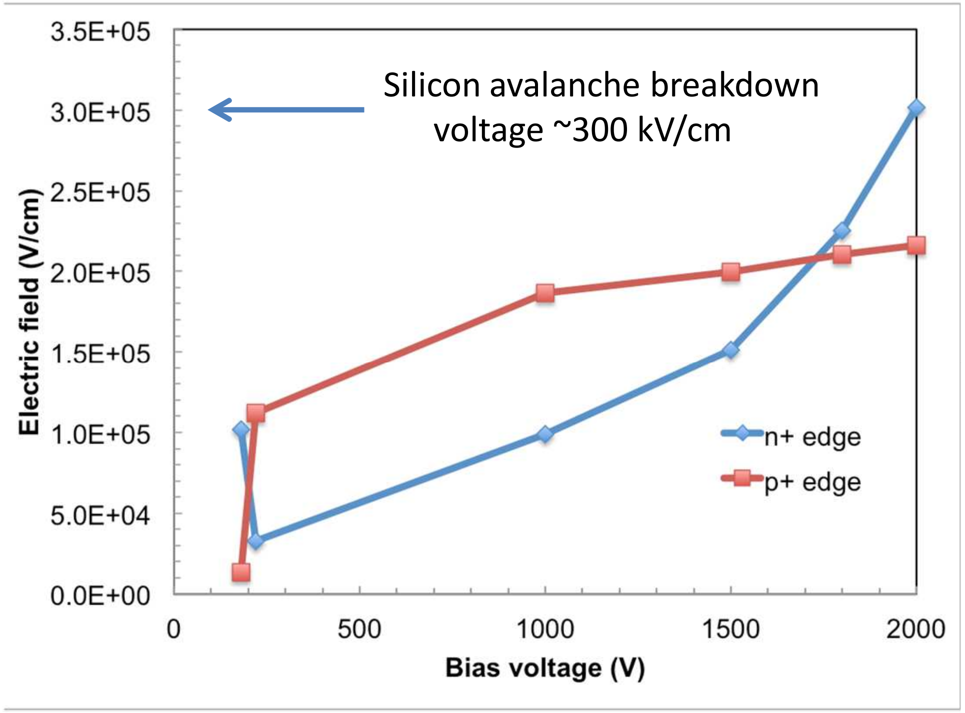



Y. Unno et al., 10.1016/j.nima.2013.04.075

- Electric potential of p-stop
  - decreases as the interface charge increases positively,
  - increases as the interface charge increases negatively.
- Measurement confirms that the interface charge is positive.

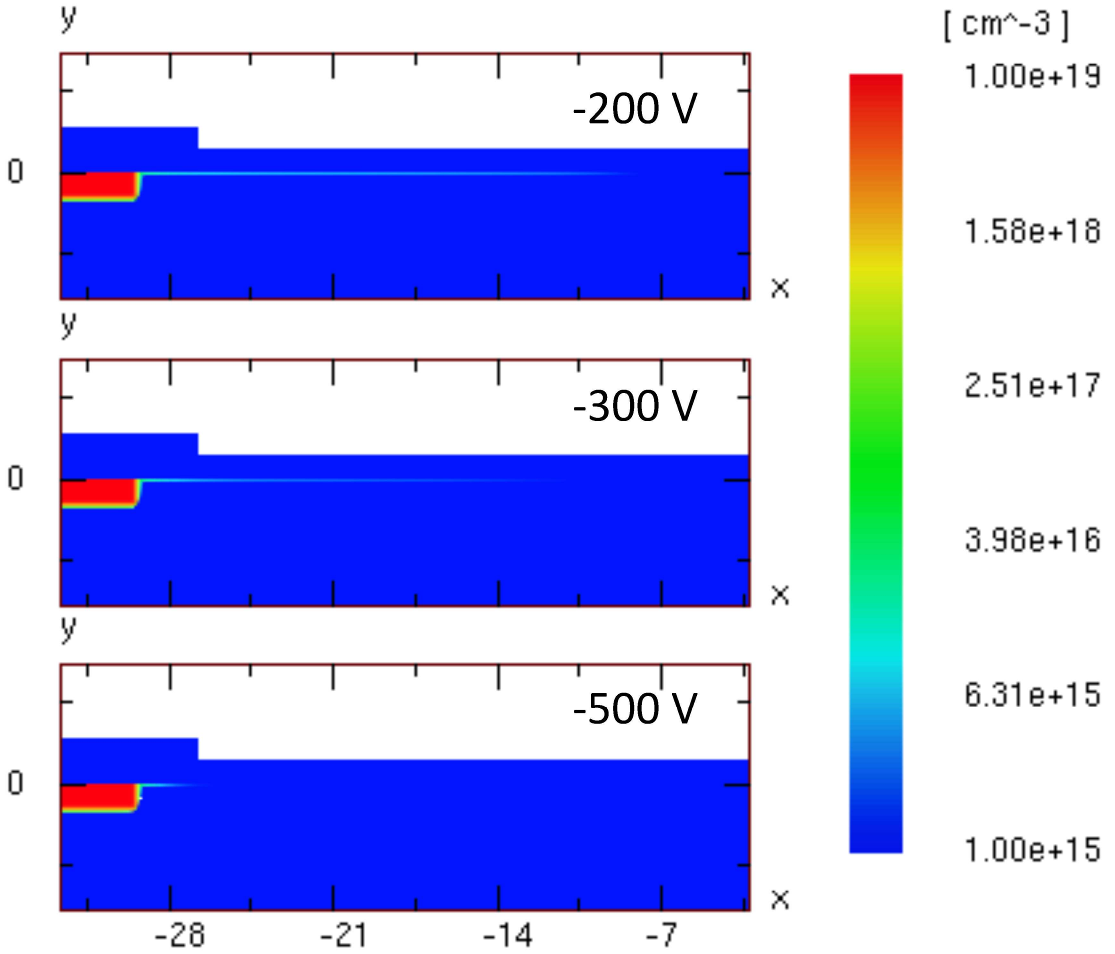
Breakdown at p-stop




Silicon avalanche breakdown voltage ~300 kV/cm

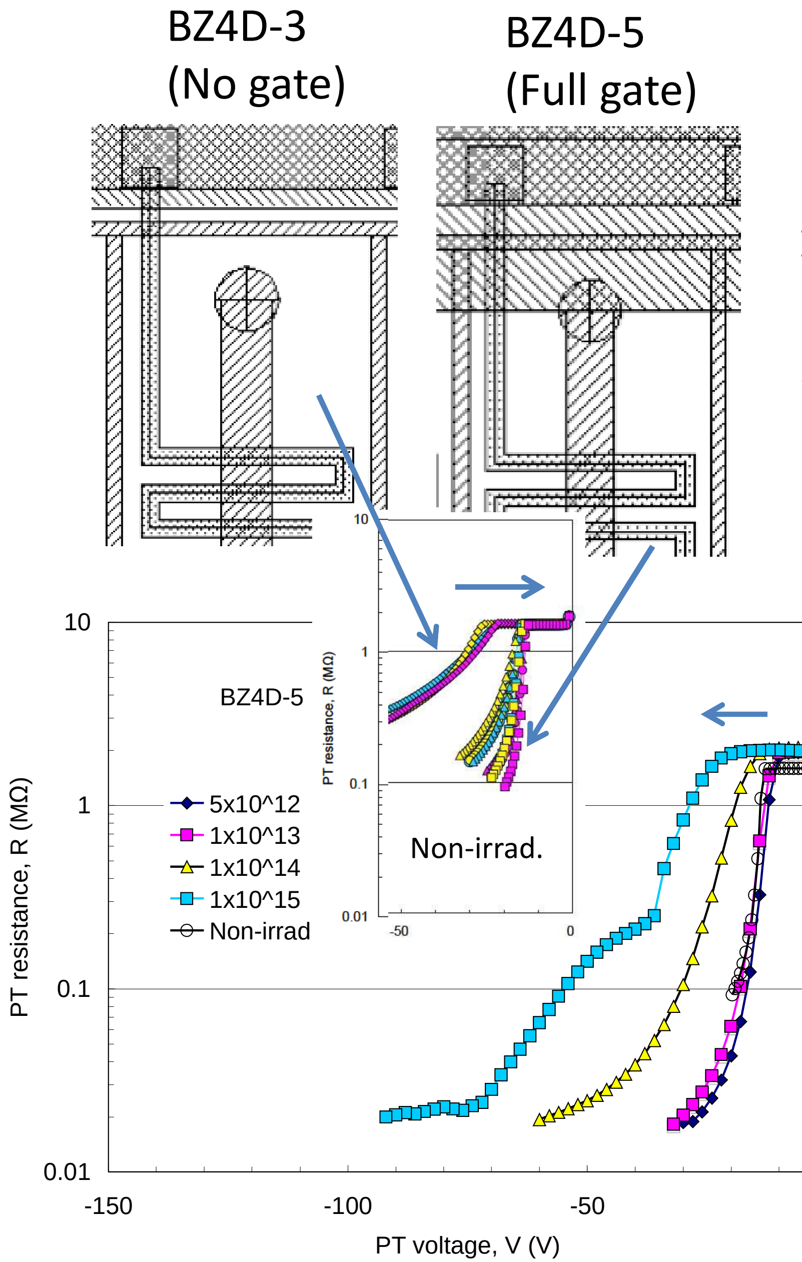
- Under the “Irradiated” condition
- Breakdown occurs at high voltage at the n$^+$ edge, although the p-stop edge was the higher electric field initially.
- The rate to increase of the electric field at the p-stop edge is saturating at higher voltage.
- The p-n junction eventually overtakes the highest electric field by the time of breakdown.
- Why?

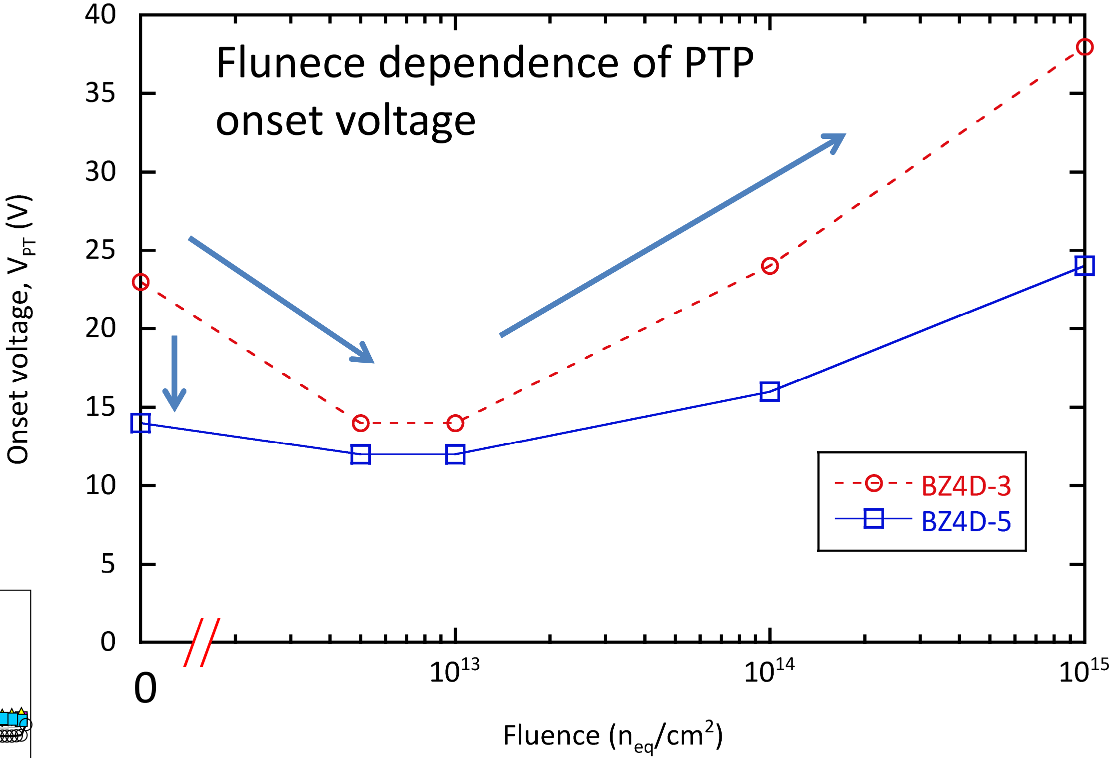
Insight into the physics



- Electron inversion layer is diminishing
  - as the bias voltage is being increased.
  - This also explains that in p-bulk the bias voltage helps to isolate the n$^+$ implants.
- Understanding the underlying physics is only possible with TCAD simulation, eventually …

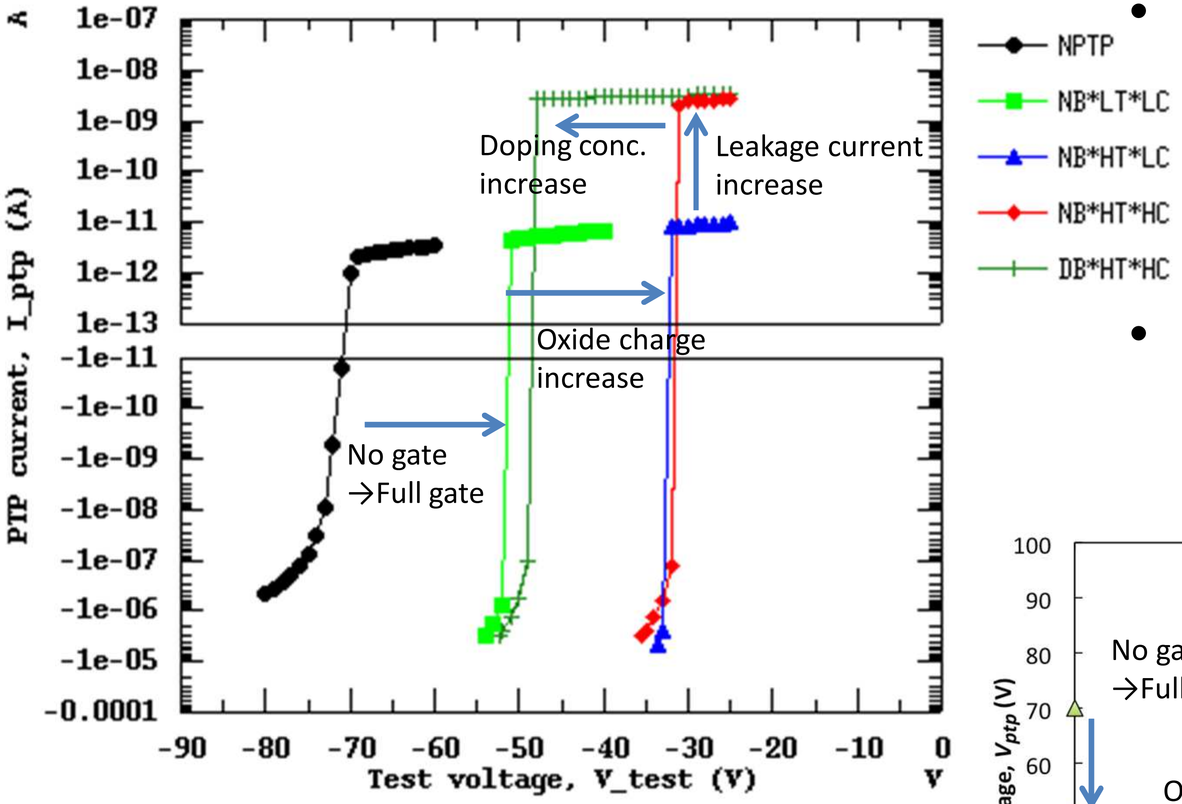
Punch-Through Protection (PTP) Structure





- “Full gate” induced PTP onset in lower voltages than “No gate”.
- Onset voltage went down first and then started to increase.
  - What causes the transitions?

PTP Simulations



Doping conc. increase

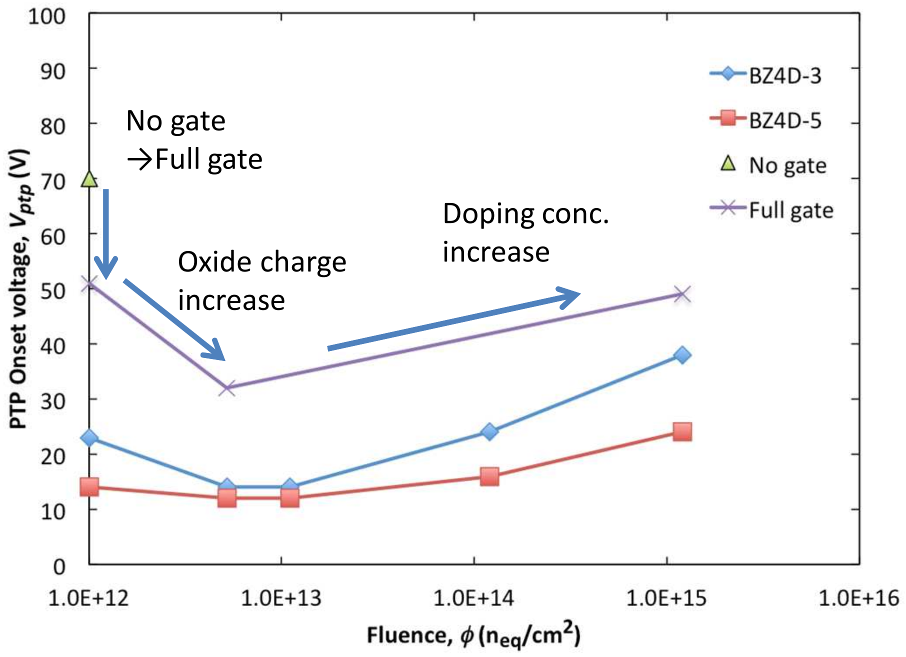
Leakage current increase

Oxide charge increase

No gate →Full gate

- The fluence dependence can be understood as the effect of
  - Build-up of the Interface charge and
  - Increase of acceptor-like levels.
- The systematic “offset”
  - difference between the 2D simulation and the 3D real.

- Onset voltage decreased as
  - No gate (black) → Full gate (colored)
  - Interface charge increased
- Increased as
  - accepter-like state increased

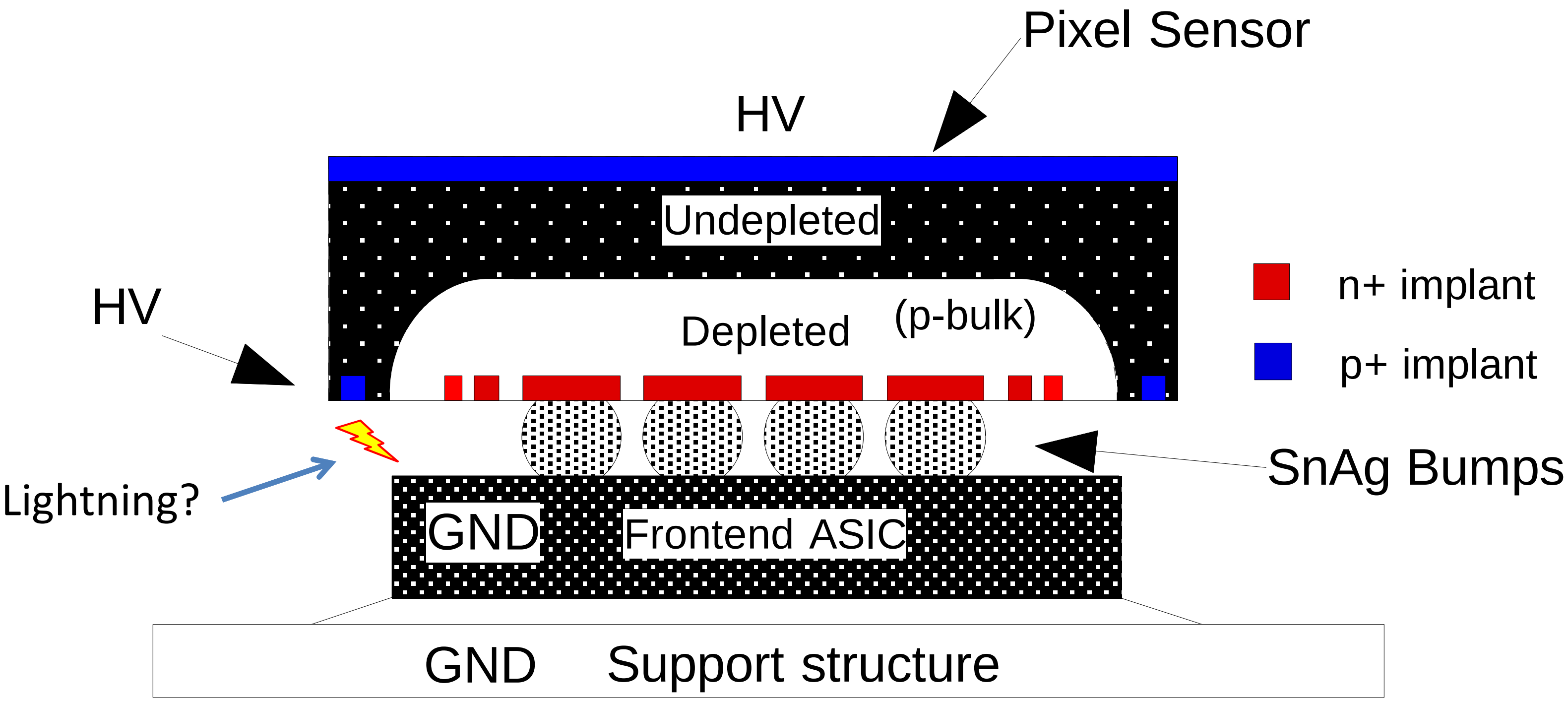


No gate →Full gate

Oxide charge increase

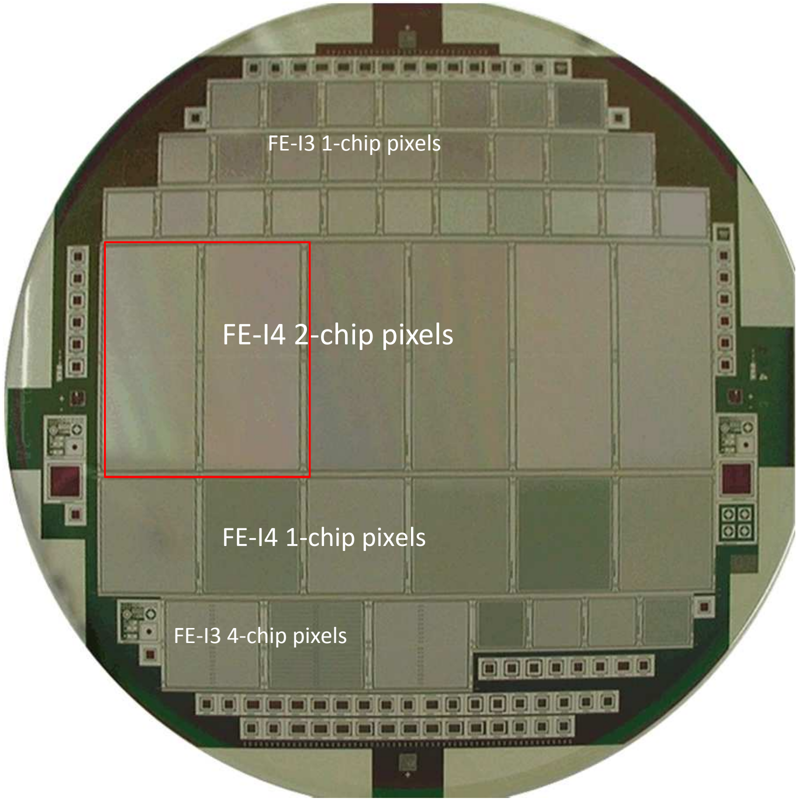
Doping conc. increase

Hybrid Planar Pixel Sensor Module

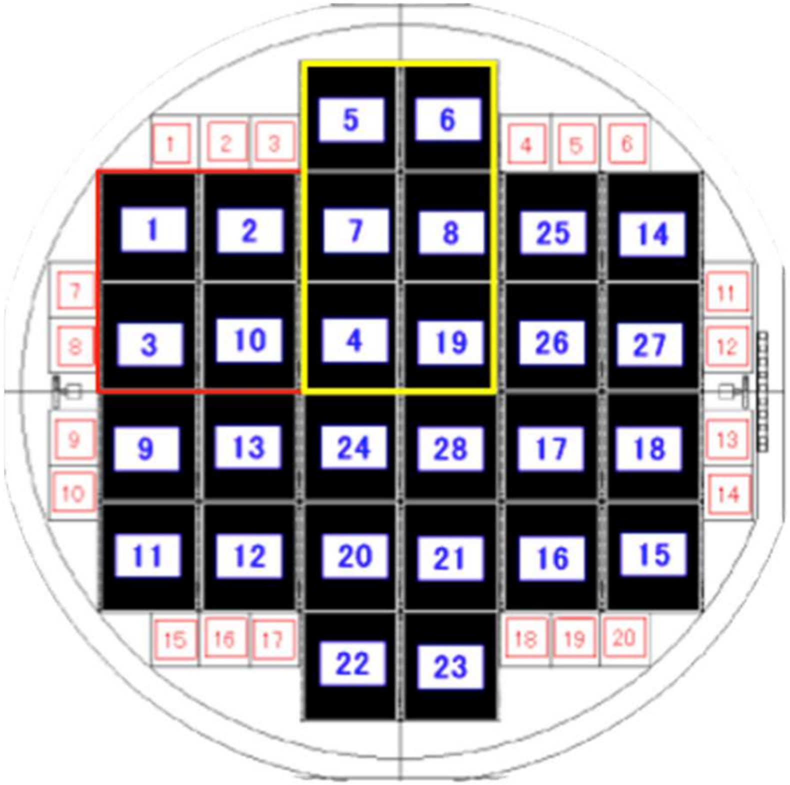


- Frontend ASIC and Pixel sensor can be optimized
  - independently, without compromise…
- We need 3 ingredients in the sensor:
  - Radiation tolerant pixel sensor (pursuing Planar process pixel sensor)
  - Bump-bonding (SnAg solder bump, e.g.)
    - Also, thin sensor (≤150 μm) – thin ASIC (≤150 μm)
  - High voltage protection at edges
    - against HV ~1000 V

KEK/HPK n-in-p Pixel Sensors

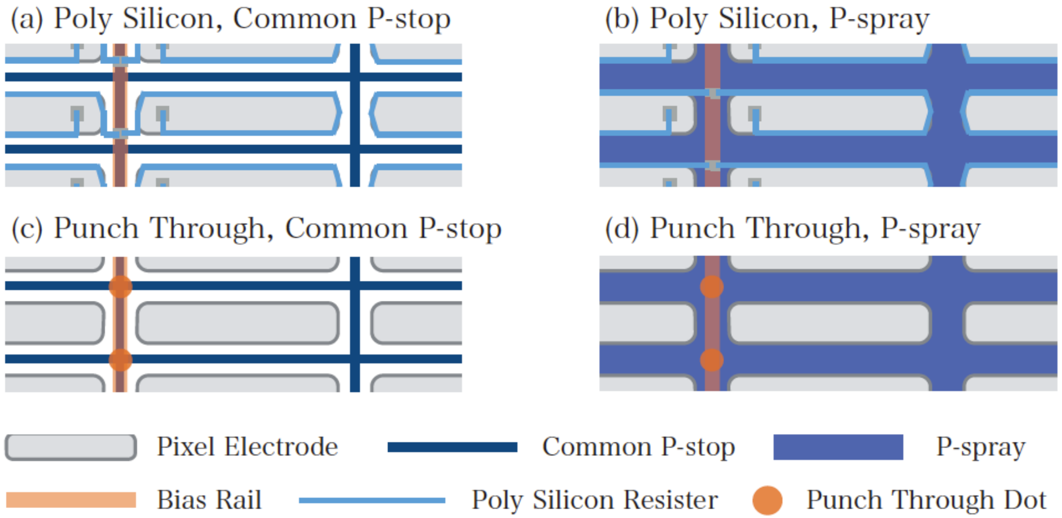


n-in-p 6” #2 wafer layout
(“Old” pixel structures)



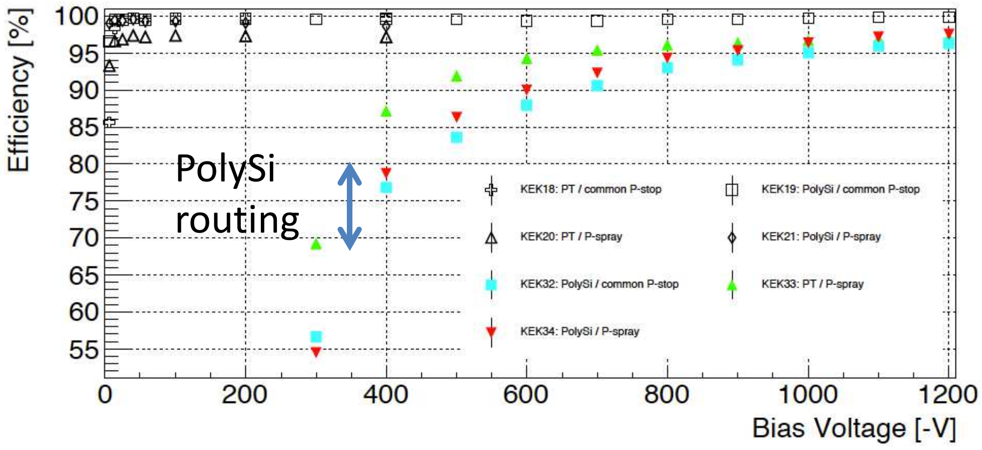
n-in-p 6” #4 New wafer layout
(“New” pixel structures)

“Old” Pixel Structures



K. Motohashi et al. HSTD9
(DOI: 10.1016/j.nima.2014.05.092)

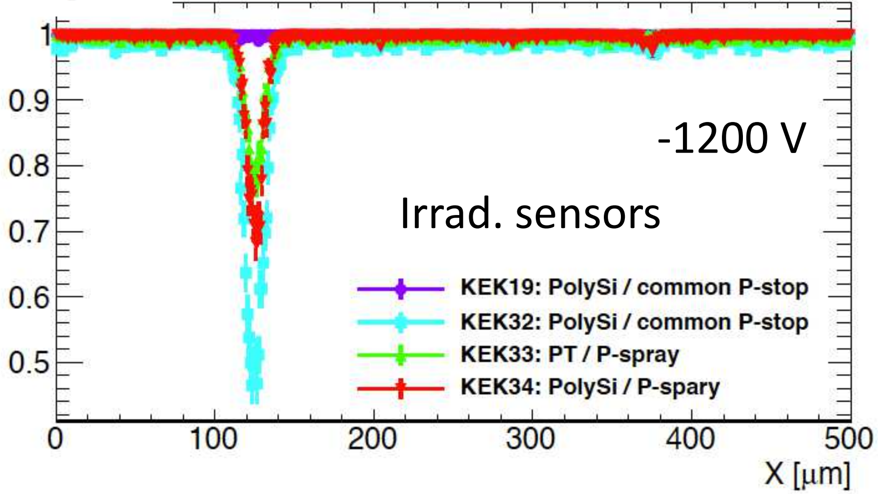
Irradiation: n 1×10^{16} neq/cm^2
at Ljubljana



PolySi routing

Bias rail

No bias rail

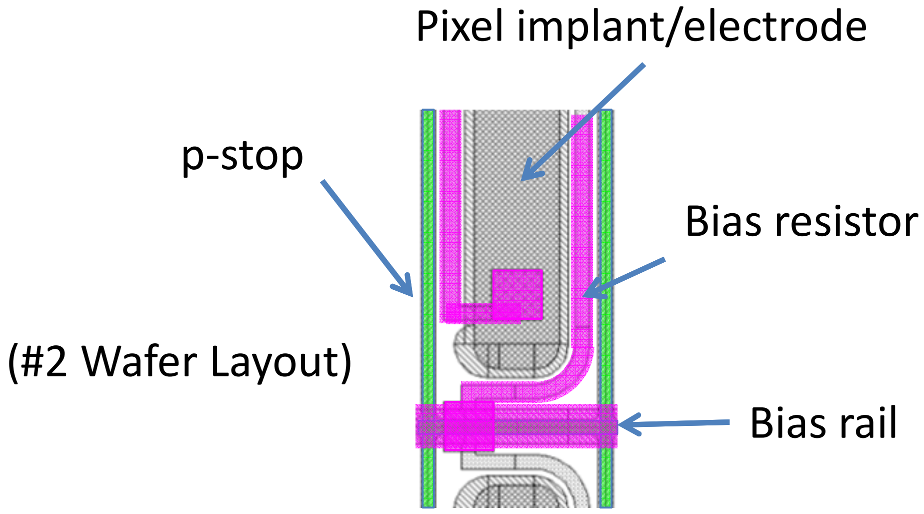


-1200 V

Irrad. sensors

- Severe efficiency loss at the boundary of pixels, under bias rail
- Subtle efficiency loss due to the routing of bias resistor

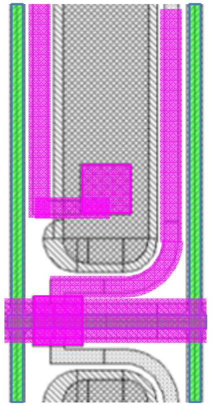
Old Pixel Structures (Wafer #2)

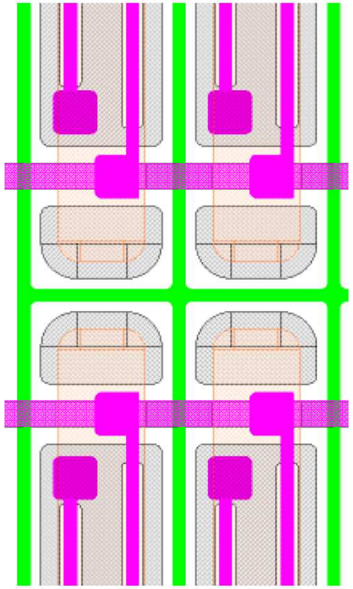


- Bias rail → at the boundary of pixels
- Bias resistor (PolySilicon) → encircled outside the pixel implant
- Bias resistor and Bias rail are connected to the pixel electrode in DC,
  - thus, both are at “ground potential”

Optimization of Pixel Structures

(#2 Wafer Layout)





(#4 Wafer Layout)

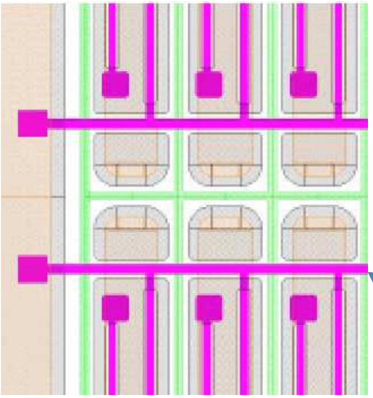
- Bias rail → Removing from the boundary to “inside” the pixel electrode.
  - Removing “ground potential” at the boundary.
- PolySilicon bias resistor → routing inside the pixel.
  - Removing another “ground potential” outside the pixel.

Bias Rail & Resistor Routing in Wafer#4

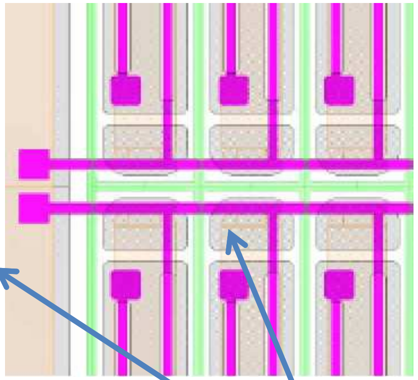
- Bias rails away from the boundary: Large-, Small-, Zig-zag-offset
  - Bias rail material (Al, PolySi)
- Bias rail at the boundary but with “wide” p-stop
- Biasing structure: PolySi , Punch-Thru (PT) resistor, No biasing

PolySi

Type2, 10
(Large-offset)

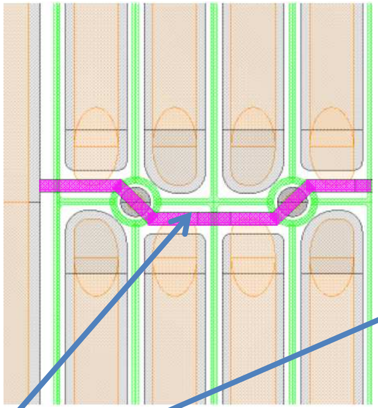


Type4, 12
(Small-offset)

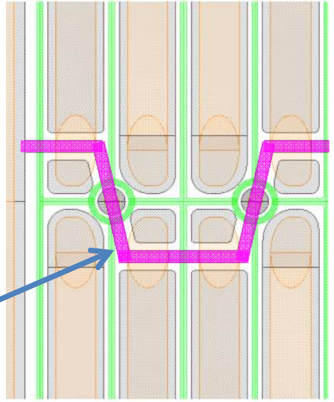


PT

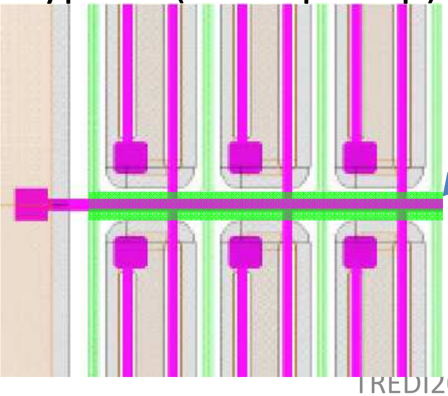
Type17
(Small-offset)



Type18
(Large offset)

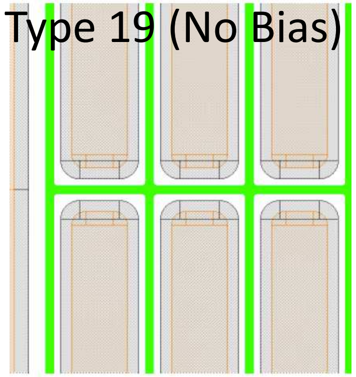


Type13 (Wide p-stop)



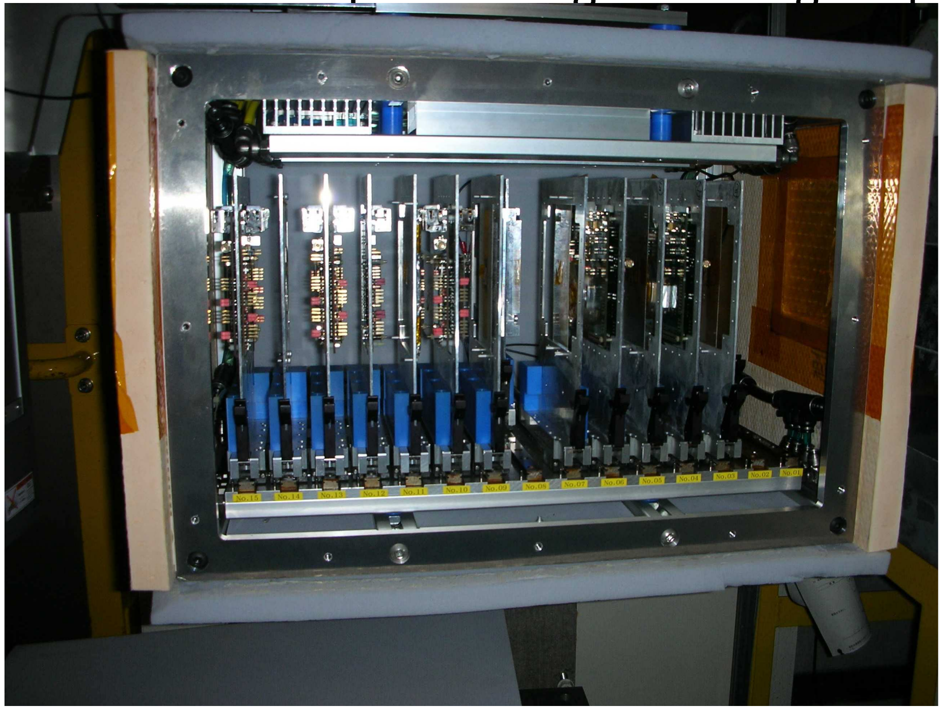
Bias rail

Type 19 (No Bias)



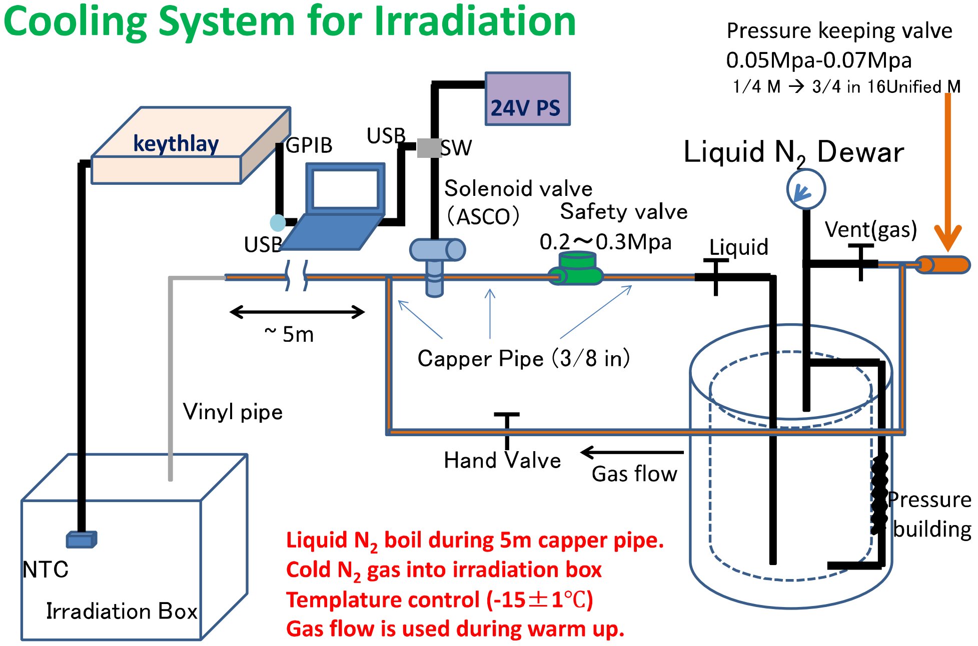
Evaluation of New Pixel Structures

- Irradiation at CYRIC
  - 70 MeV protons, Tohoku Univ., Japan
  - 3 to 5 x 10^{15} neq/cm^2
- Latest setup
  - Irradiation box with 15 “push-pull” slots
  - “Liquid” Nitrogen cooling evaporated in supply line



Samples in the irradiation box at CYRIC

Cooling System for Irradiation



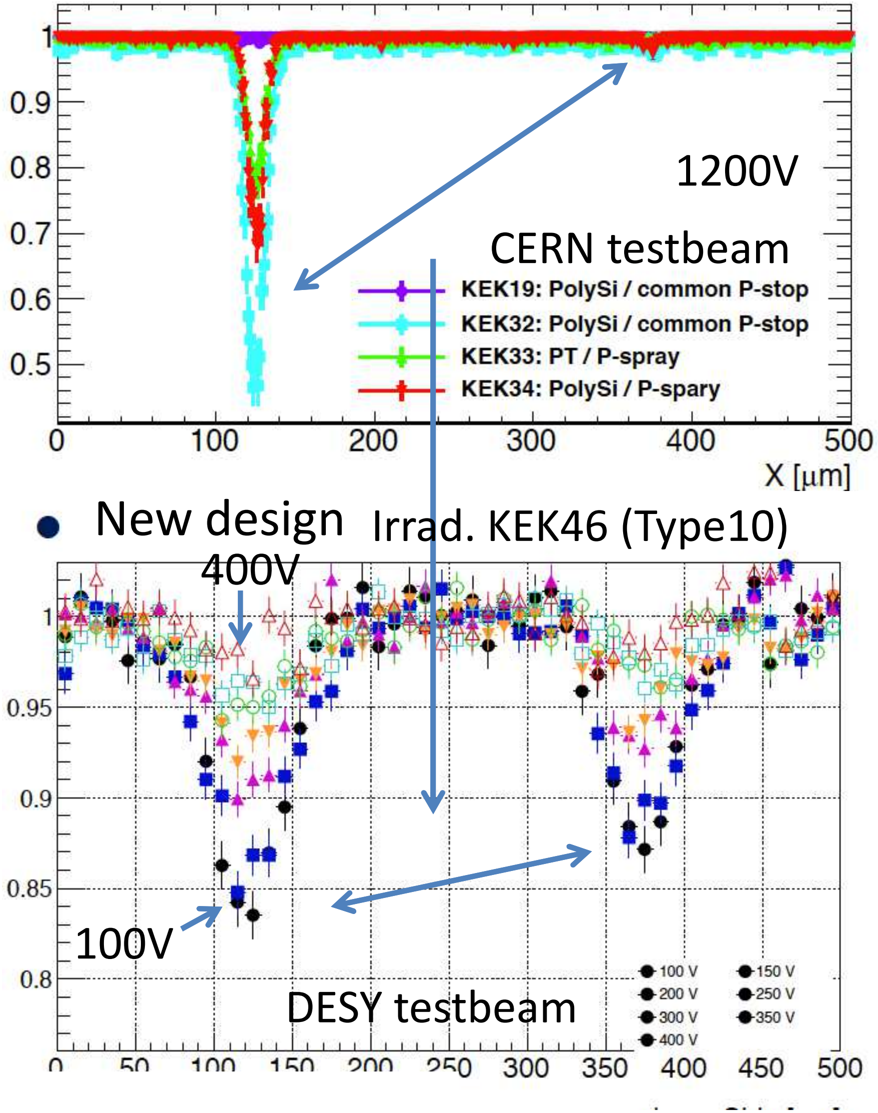
Liquid N_2 boil during 5m capper pipe.
Cold N_2 gas into irradiation box
Templature control (-15±1℃)
Gas flow is used during warm up.

** 1 atm = 1.03 kg/cm^2=1013hPa=0.1013MPa

Results with Testbeams

D. Yamaguchi

Old design



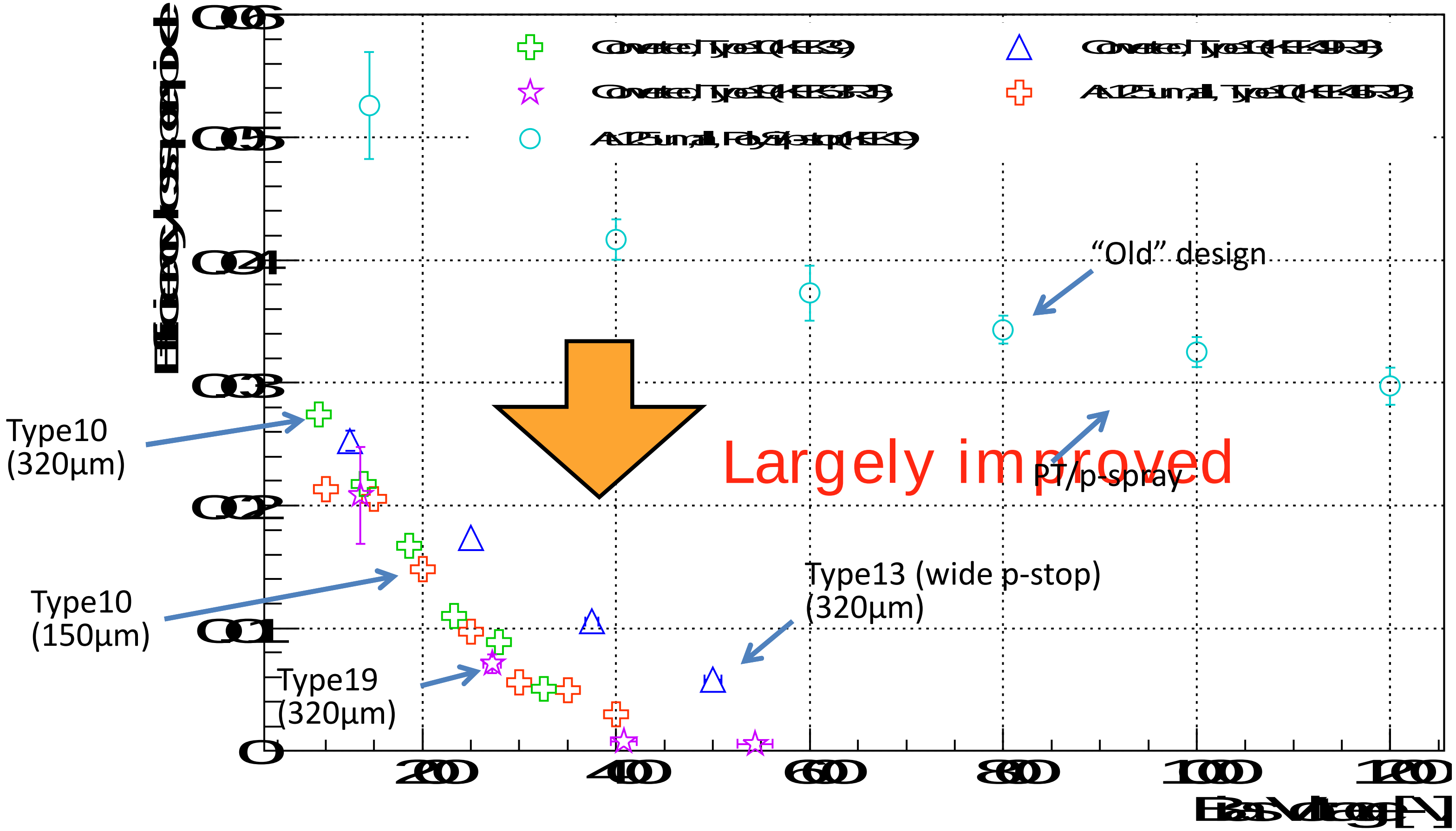
- New design Irrad. KEK46 (Type10)

- Comparison of “Area”
  - Width of the dip is due to pointing resolution,
  - Eliminating the effect of resolution.
- Left-Right imbalance is very much improved.
  - Bias rail effect is nearly eliminated.

Comparison of Structures

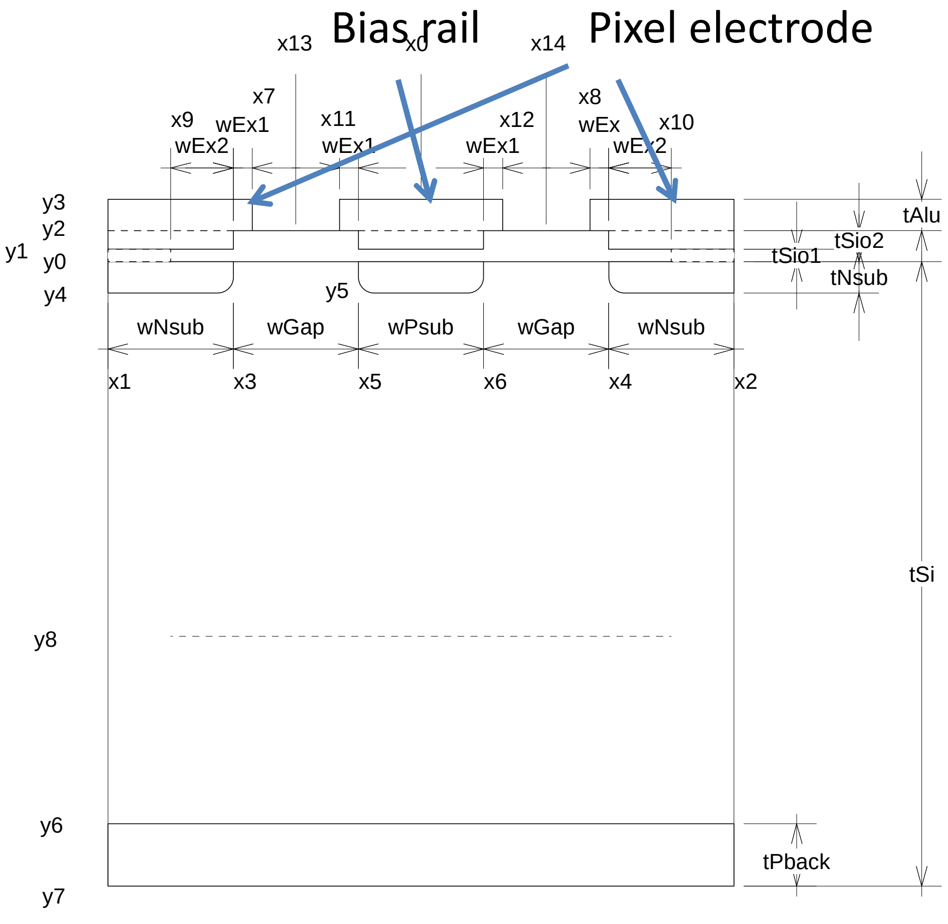
D. Yamaguchi

Scaled to 150 µm, 5×10^{15} irrad.



- "Old" design loses 2-3% eff. under the bias rail; 97-98% eff. overall.
- "New" design (Type10 (large offset)) is nearly as good as "no bias", almost 0% loss >400 V.
- Type13 (wide p-stop) has been improved.

TCAD Geometry



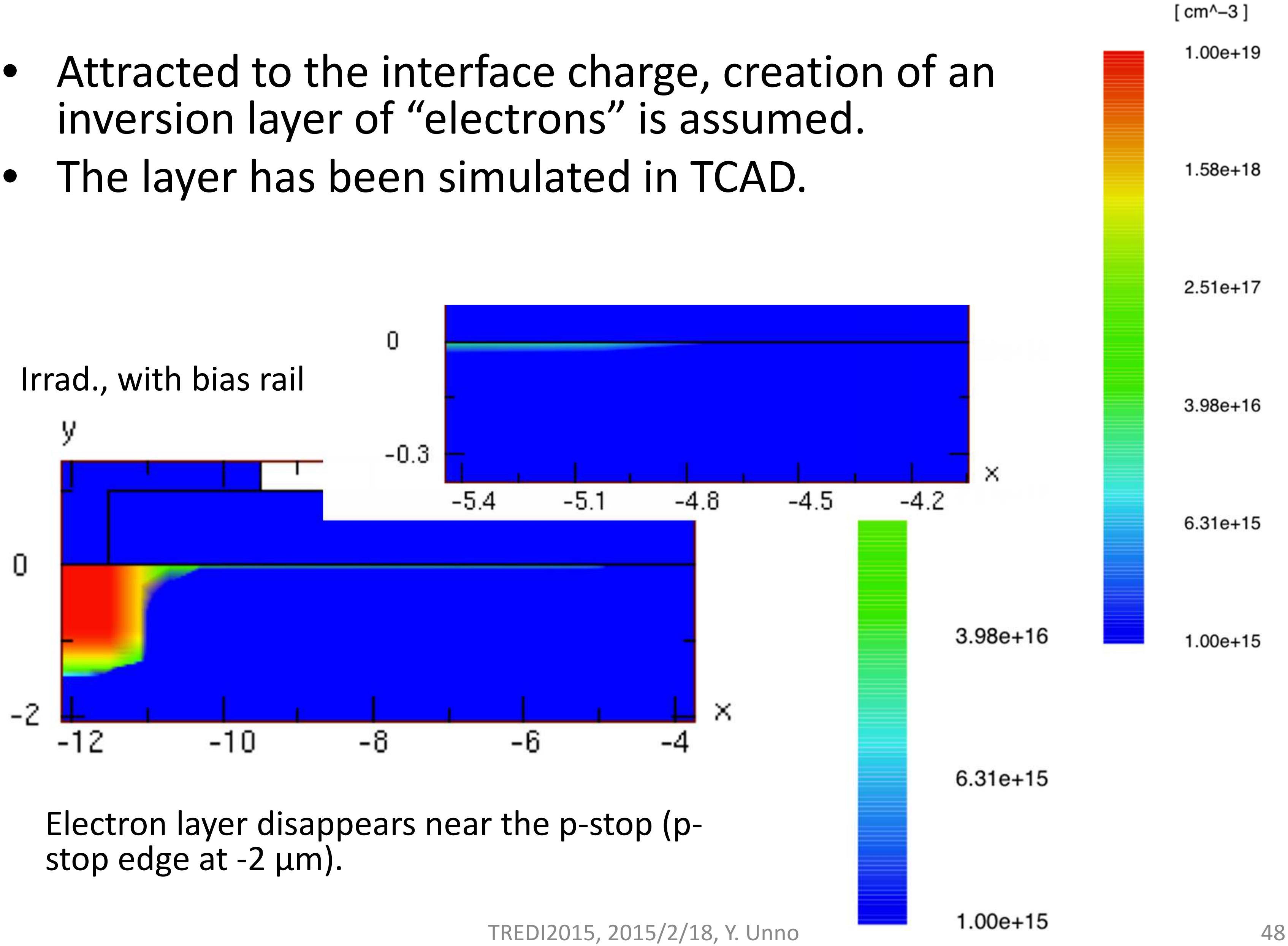
(Not to scale)

	Non-irrad	Irrad
Si thickness (μm)	150	150
Fluence (neq/cm^2)	Null	3×10^{15}
N_{eff} (p-type)(cm^{-3})	2.6×10^{12}	2.5×10^{13}
V_{dep} (V_{app}) (V)	44 (100)	430 (430)
Interface charge Q_f (cm^{-2})	1×10^{10}	1×10^{12}

V_{dep} = depletion voltage
V_{app} = applied bias voltage

Electron Layer

- Attracted to the interface charge, creation of an inversion layer of “electrons” is assumed.
- The layer has been simulated in TCAD.

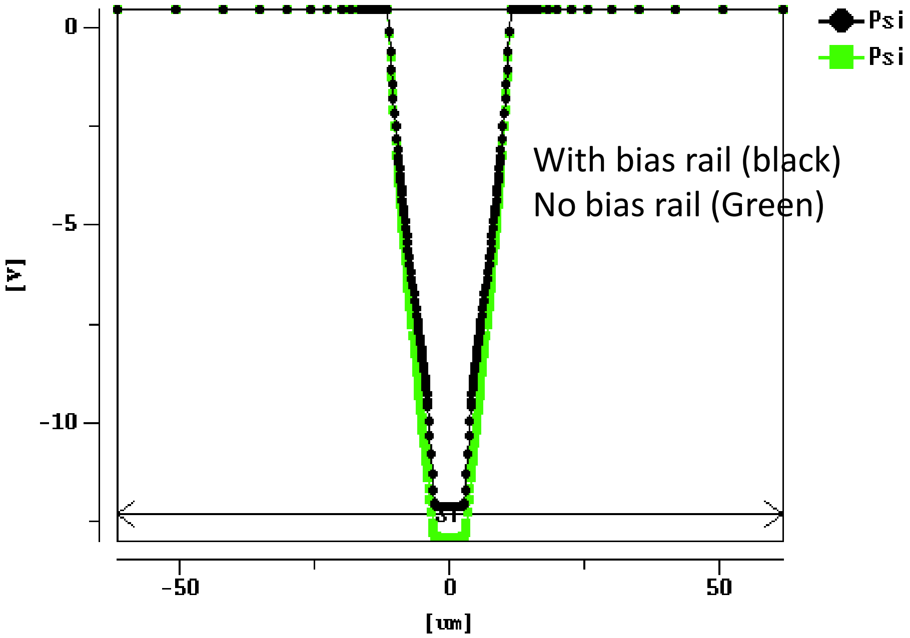


Irrad., with bias rail

Electron layer disappears near the p-stop (p-stop edge at -2 µm).

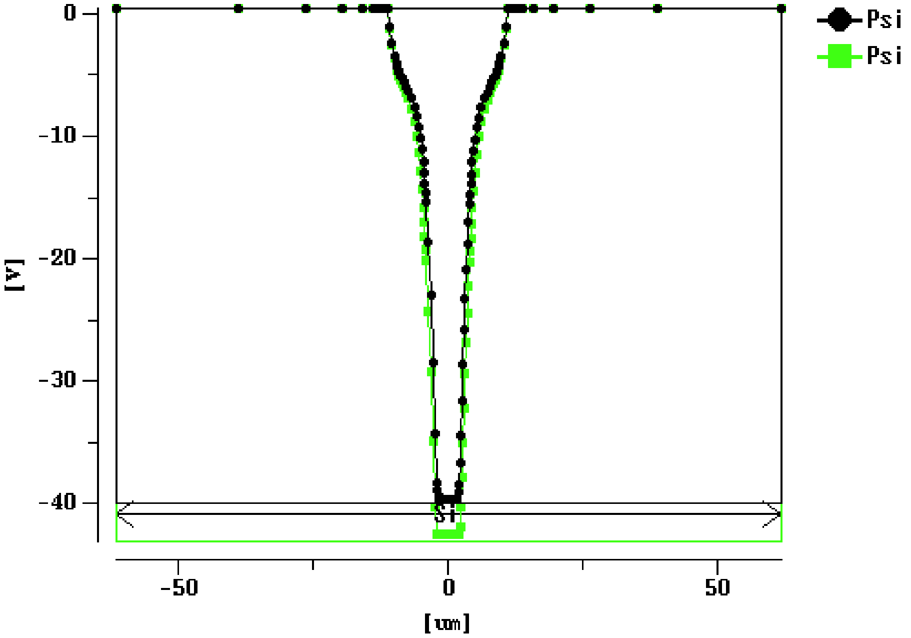
Effect of Potential of Bias Rail

Non-irrad.



With bias rail (black)
No bias rail (Green)

Irrad.



- Electric field (Potential) between pixels
  - near the surface (1 µm below the surface of Si in TCAD)
- Existence or non-existence of bias rail (“ground potential”)
  - has not affected the electric field potential very much.
  - Relative potential “depth” at the boundary is shallower in “Irrad.”: ~15% (=-15/-100, Non irrad.), ~9% (=-40/-430, Irrad.), but
  - Absolute potential is larger in “Irrad.”: -15 V (Non-irrad.), -40 V (Irrad.)

Induced Charge – Ramo's theorem

- A mobile charge in the presence of any number of grounded electrodes, the induced charge Q_A at an electrode A is

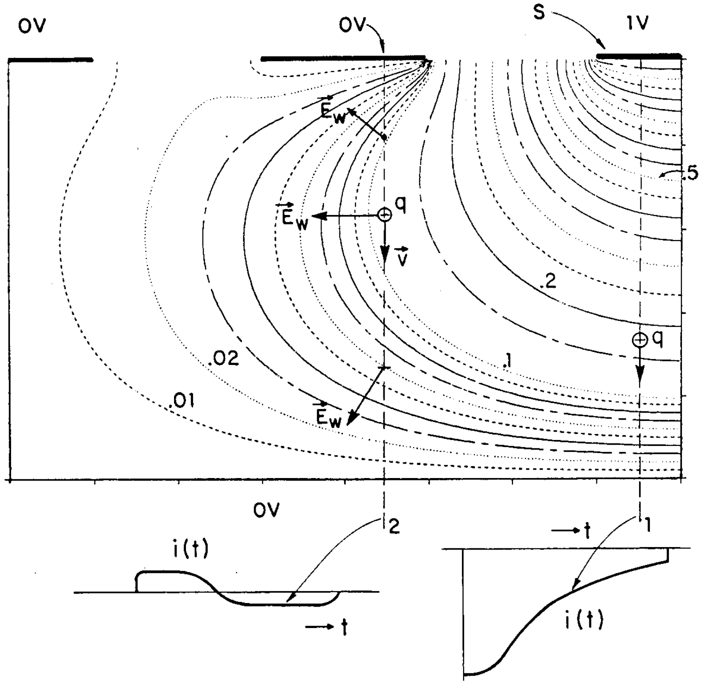
$$Q_A = q \cdot V_{qA}$$

  - where q is the charge in a position, V_{qA} the "weighting potential" of the electrode A at the position of q.
- If a charge q moves along any path from position 1 to position 2 (after infinite time),

$$\Delta Q_A = q \cdot \left(V_{qA}(2) - V_{qA}(1) \right)$$

- In a finite time and with a readout circuitry, instantaneous induced current, i_A, shall be integrated (with a proper shaping time) along the moving direction.

$$i_A = q \frac{dV_{qA}}{dt} = q \left(\frac{\partial V_{qA}}{\partial x} \frac{dx}{dt} \right) = q \cdot \overrightarrow{v_x} \cdot \overrightarrow{\frac{\partial V_{qA}}{\partial x}}$$



(From V. Radeka)

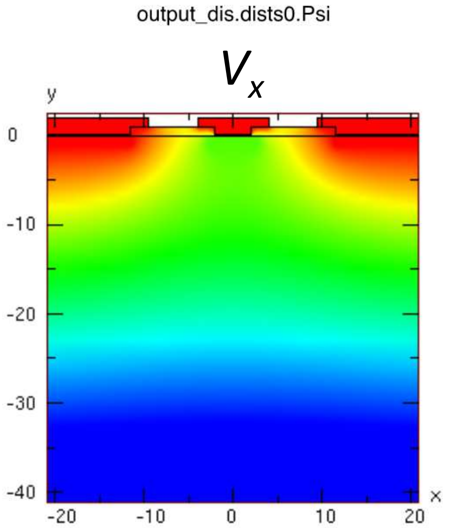
Induced Charge – Ramo's theorem

$$i_A = q \cdot \overrightarrow{v_x} \cdot \overrightarrow{\frac{\partial V_{qA}}{\partial x}} \qquad \overrightarrow{v_x} = \mu \overrightarrow{E_x} = \mu \overrightarrow{\frac{\partial V_x}{\partial x}}$$

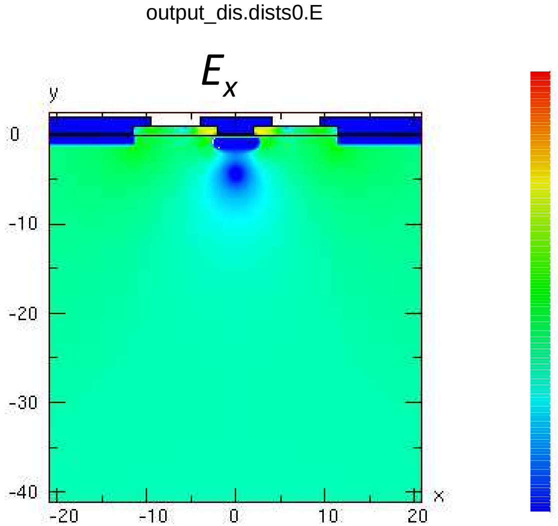
- We have to think two different fields: the "electric field" E_x (and in turn the "electric field potential" V_x) and the "weighting potential" V_{qA} .
- Although the final answer shall be obtained after integrating the current, we can have insight qualitatively from the relevant potentials,

$$V_x, E_x, V_{qA}$$

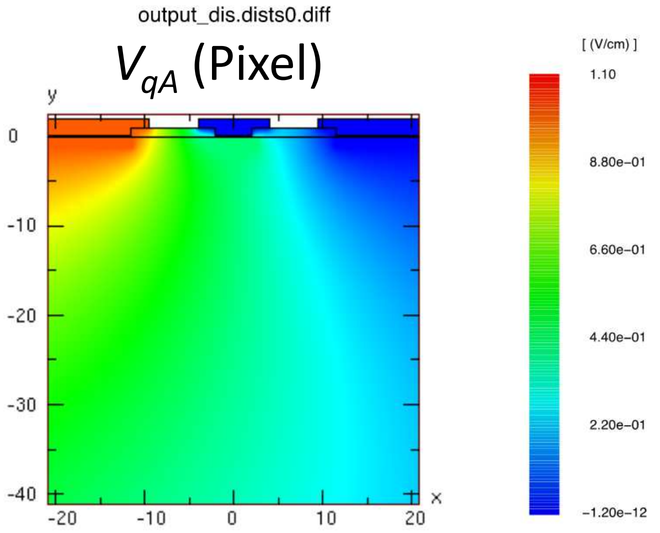
Non-irrad, With Bias Rail



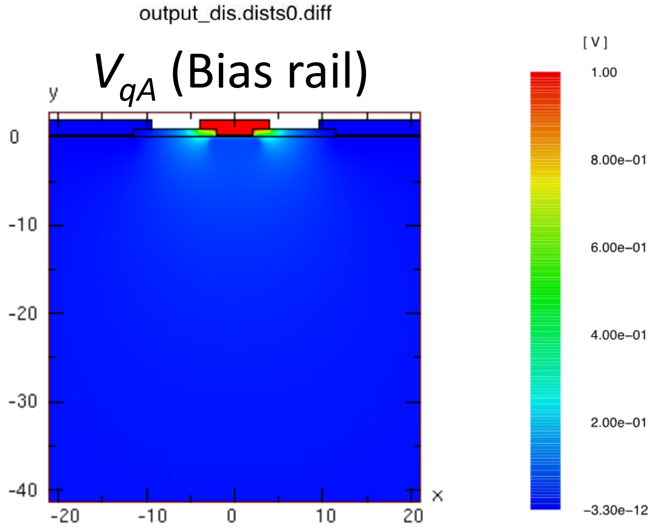
V_x



E_x



V_{qA} (Pixel)



V_{qA} (Bias rail)

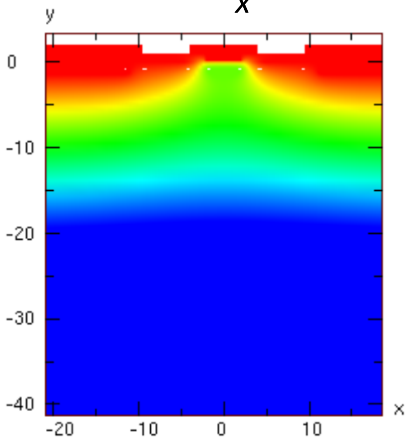
$$\vec{v}_x = \mu \vec{E}_x = \mu \frac{\overrightarrow{\partial V_x}}{\partial x} \qquad i_A = q \cdot \vec{v}_x \cdot \frac{\overrightarrow{\partial V_{qA}}}{\partial x}$$

$$\Delta Q_A = q \cdot \left(V_{qA}(2) - V_{qA}(1) \right)$$

Irrad, With Bias Rail

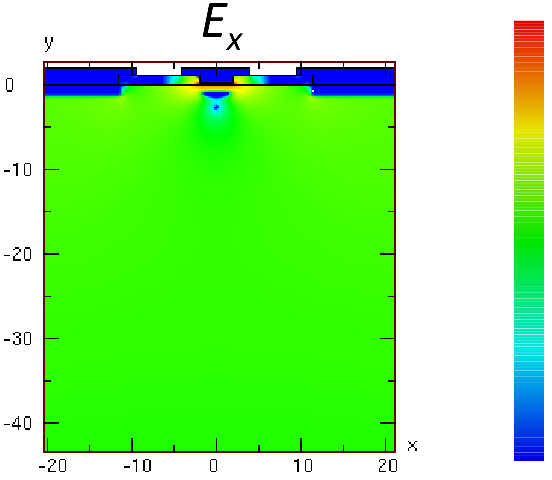
output_dis.dists0.Psi

V_x



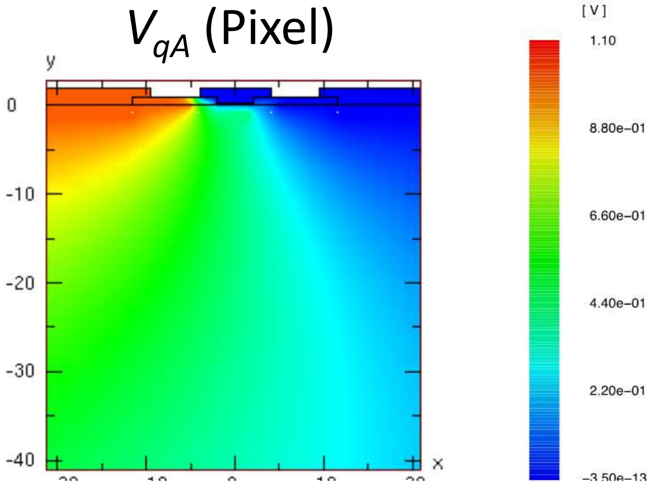
output_dis.dists0.E

E_x



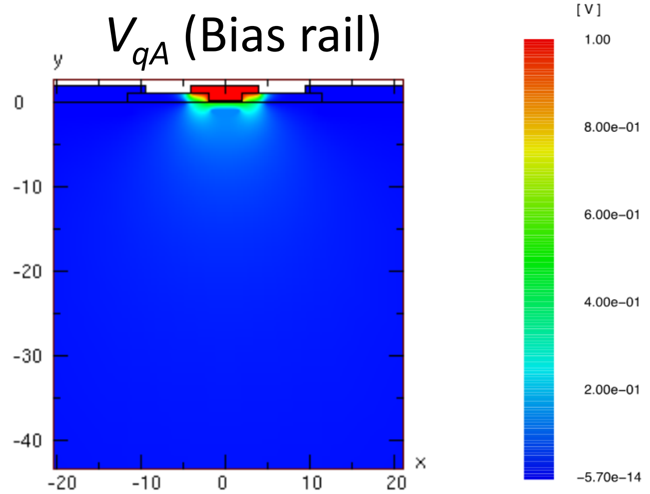
output_IrradWBS_dis.dists0.diff

V_{qA} (Pixel)



output_dis.dists0.diff

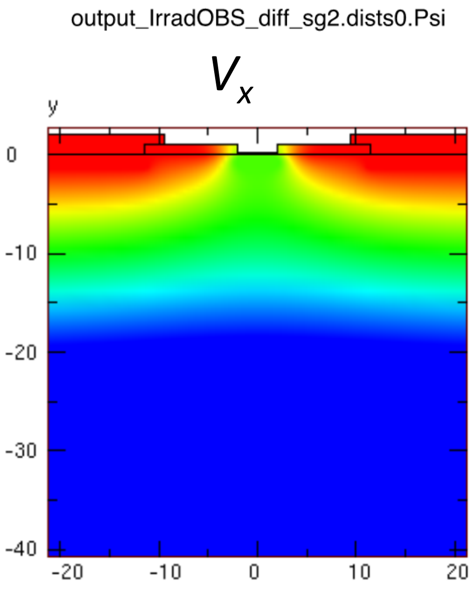
V_{qA} (Bias rail)



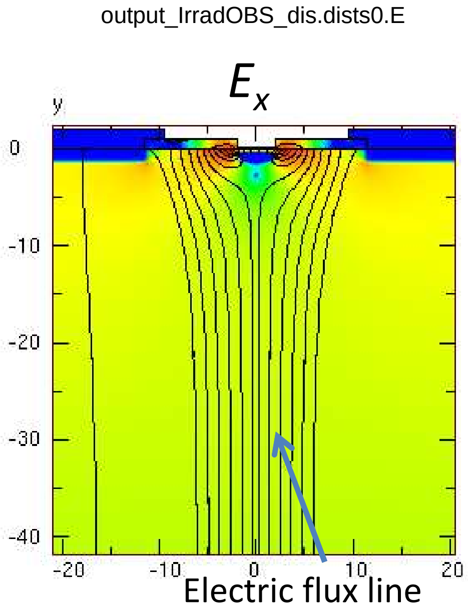
$$\vec{v}_x = \mu \vec{E}_x = \mu \frac{\overrightarrow{\partial V_x}}{\partial x} \qquad i_A = q \cdot \vec{v}_x \cdot \frac{\overrightarrow{\partial V_{qA}}}{\partial x}$$

$$\Delta Q_A = q \cdot \left(V_{qA}(2) - V_{qA}(1) \right)$$

Irrad., No Bias Rail

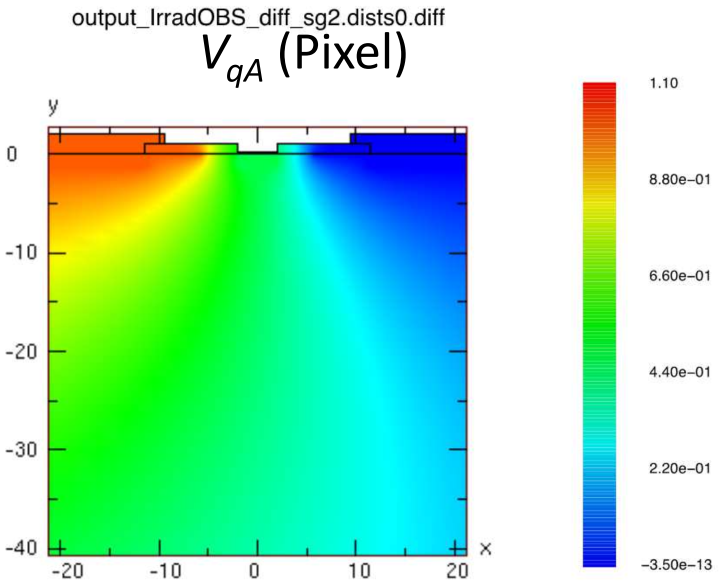

output_IrradOBS_diff_sg2.dists0.Psi

V_x


output_IrradOBS_dis.dists0.E

E_x

Electric flux line


output_IrradOBS_diff_sg2.dists0.diff

V_{qA} (Pixel)

$$\overrightarrow{v_x} = \mu\overrightarrow{E_x} = \mu\frac{\overrightarrow{\partial V_x}}{\partial x} \qquad i_A = q\cdot\overrightarrow{v_x}\cdot\frac{\overrightarrow{\partial V_{qA}}}{\partial x}$$

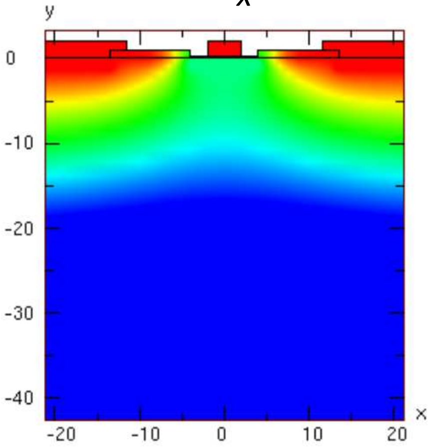
$$\Delta Q_A = q\cdot\left(V_{qA}(2) - V_{qA}(1)\right)$$

- Charges move along the electric flux lines.

Irrad., Wide P-stop

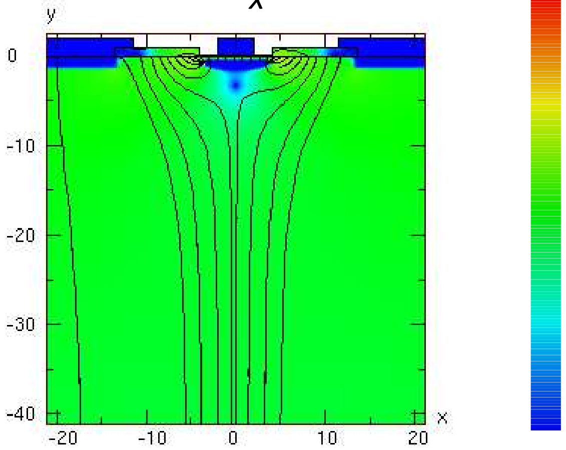
output_dis.dists0.Psi

V_x



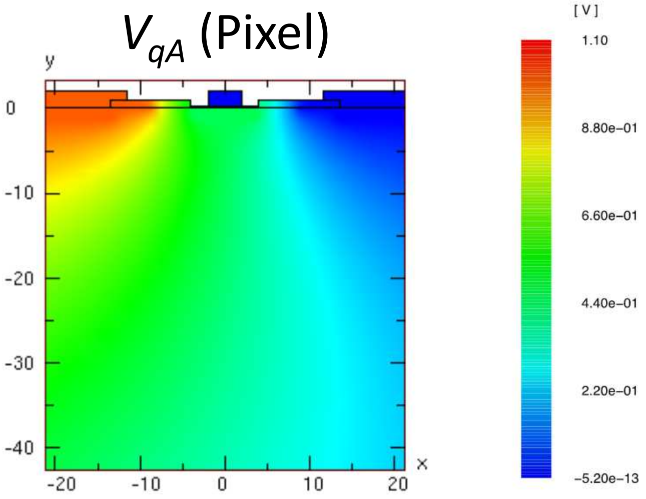
output_IrradWidePstop_dis.dists0.E

E_x



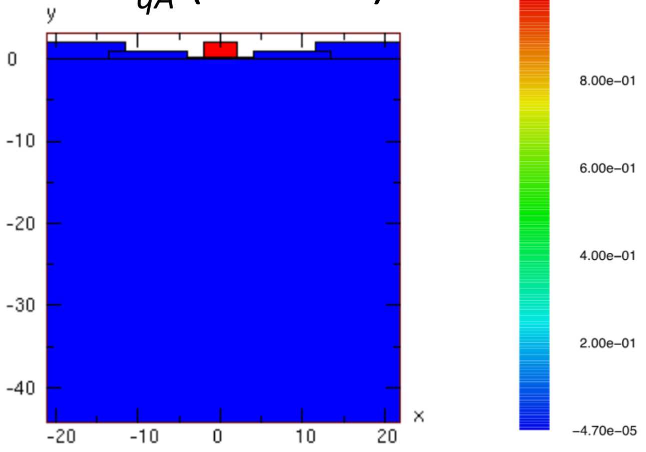
output_dis.dists0.diff

V_{qA} (Pixel)



output_dis.dists0.diff

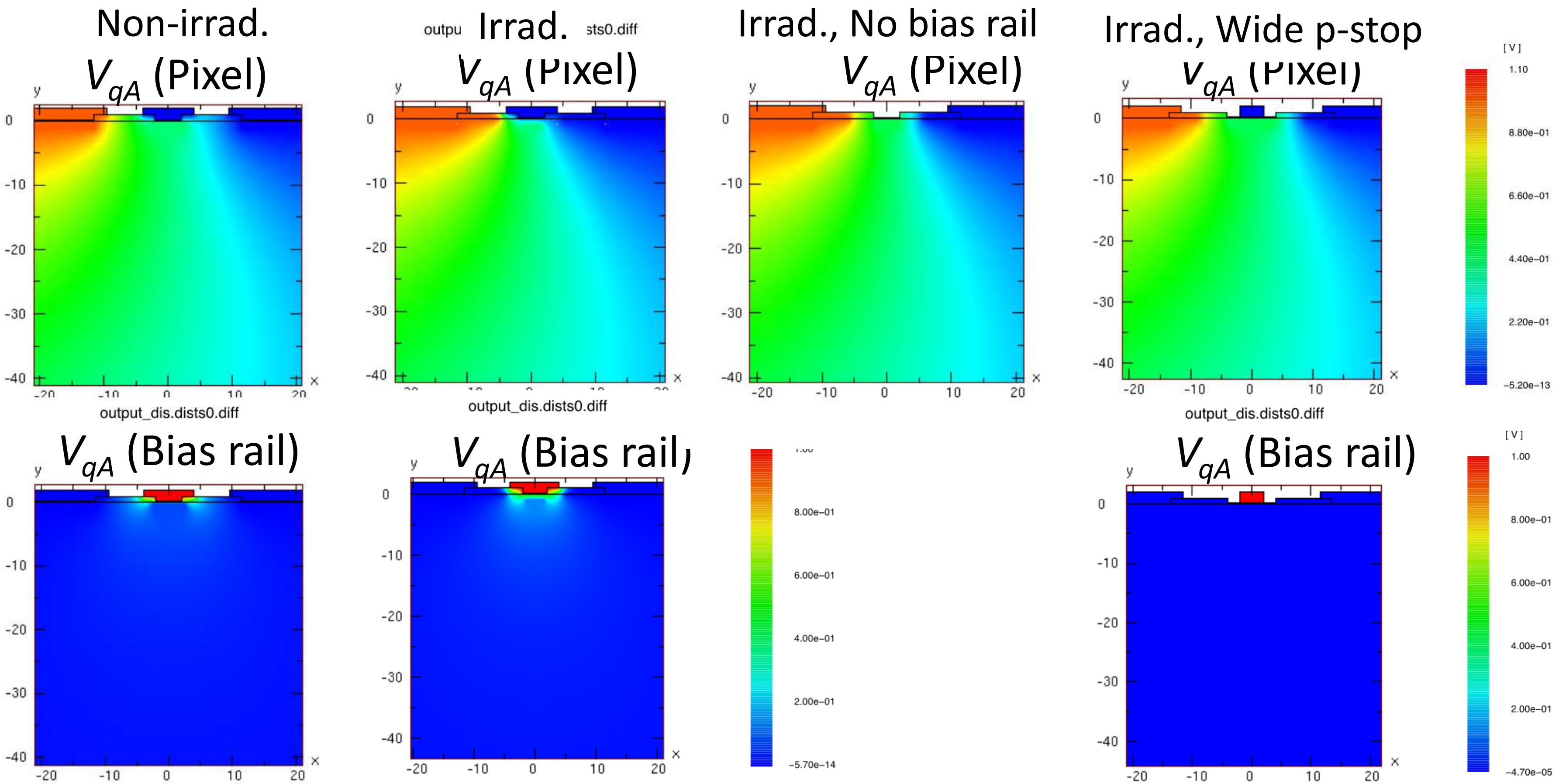
V_{qA} (Bias rail)



$$\overrightarrow{v_x} = \mu \overrightarrow{E_x} = \mu \frac{\overrightarrow{\partial V_x}}{\partial x} \qquad i_A = q \cdot \overrightarrow{v_x} \cdot \frac{\overrightarrow{\partial V_{qA}}}{\partial x}$$

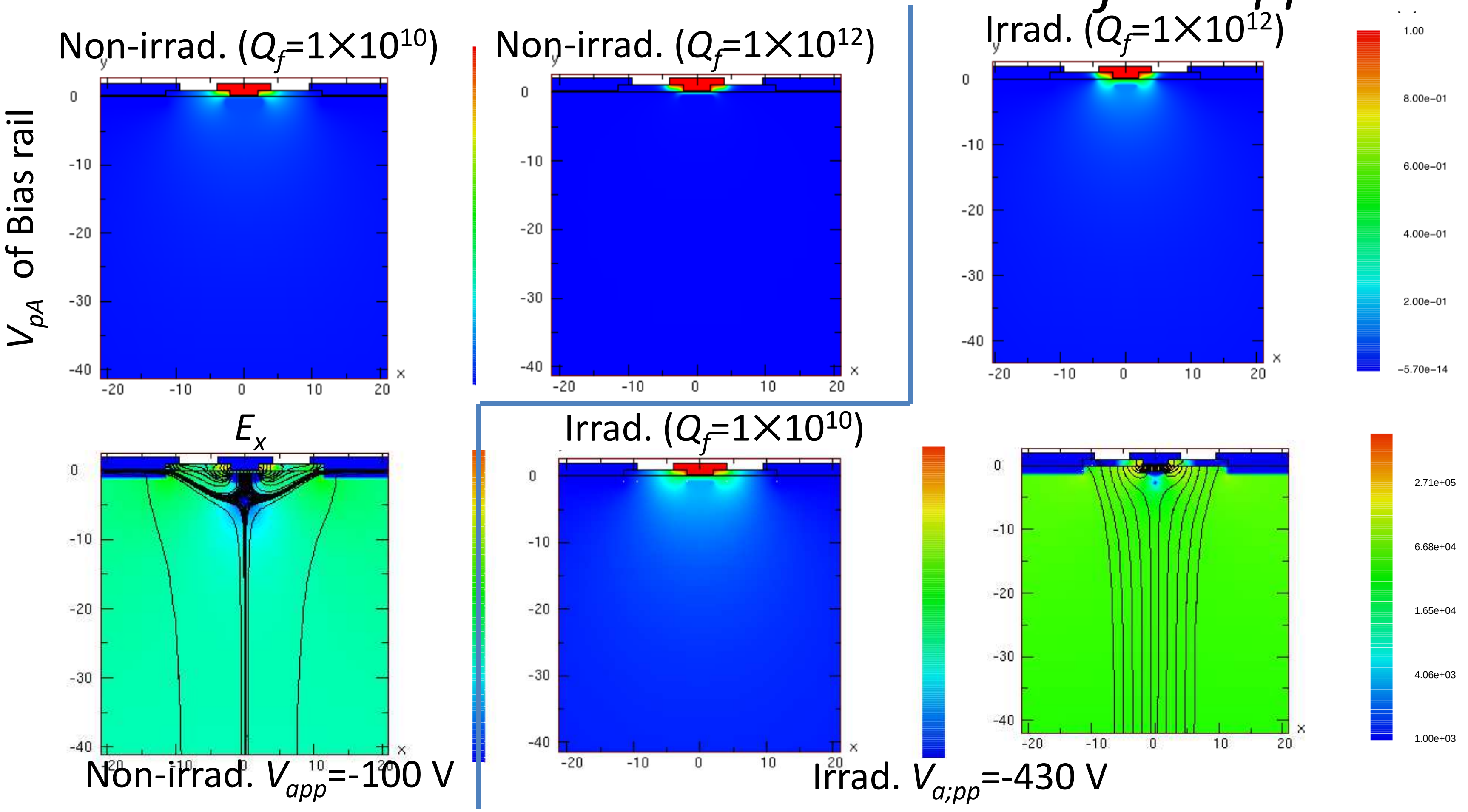
$$\Delta Q_A = q \cdot \left(V_{qA}(2) - V_{qA}(1) \right)$$

What is going on with bias rail?



- "Weighting potential"
  - of the "bias rail" has larger area of non-uniformity under the bias rail in "irrad." than "non-irrad." condition .
- Why?

Who is the Suspect? Q_f, V_{app}?



V_{pA} of Bias rail

Non-irrad. (Q_f=1×10^{10})

Non-irrad. (Q_f=1×10^{12})

Irrad. (Q_f=1×10^{12})

E_x

Irrad. (Q_f=1×10^{10})

Non-irrad. V_{app}=-100 V

Irrad. $V_{a;pp}$=-430 V

- Strong electric field in the “irrad.” device has enhanced the non-uniform area of the weighting potential of the bias rail.
- Interface charge increase is acting to reduce the non-uniform area.
- Weak spot in the “non-irrad.” device deflects electric flux lines and the weighting pot., like a “shield”.

Discussion

- Novel design of the pixel structure has improved the efficiency loss due to the bias rail and bias resistor routing.
  - More structures need to be evaluated with testbeam to complete the variation of the design.
- Underlying physics has been understood with TCAD simulation (at least qualitatively).
  - The less-charge collection under the bias rail of the irrad. device seems to be caused by the fact that the bias rail is acting as electrode (collecting induced charge).
- If the bias rail acts as electrode, why are “irrad.” and “non-irrad.” different?
  - Strong electric field in the “irrad.” device has enhanced the charge to the bias rail.
  - In “non-irrad.” device, the bias rail as an electrode seems to be “shielded” with low electric field region under the bias rail.
  - Interface charge increase is helping to “reduce” the charge to the bias rail, (contrary to naive expectation).

Summary

- We have undertaken development of radiation-tolerant silicon tracking sensor over 30 yrs in Japan, together with the study of radiation damages.
- In the planar process sensor, radiation-tolerance is to make the sensor being operable to high voltage to cope with the increase of the full depletion voltage, and even in the non-irrad. device for the QA and preparing for un-expected.
- The first application was the p^+-in-n microstrip sensor for the ATLAS inner tracker, to the fluence of $2x10^{14}$ neq/cm^2, which is operable to 500 V.
- We have developed further radiation-tolerant silicon tracking sensors (strips ($2x10^{15}$) and pixels ($2x10^{16}$)) for the LHC upgrade (HL-LHC), based on n^+-in-p technology, operable to 1000 V.
- TCAD simulation (but using only a part of it) has been a great tool for understand/visualizing the underlying physics, together with the visualization by the infrared camera.

Contributors

- ATLAS-Japan Silicon Group
  - KEK, Tokyo Inst. Tech., Osaka Uni., Kyoto Uni. Edu., Uni. Tsukuba, Waseda Uni.
- Hamamatsu Photonics K.K.
- p-type strip sensor collaboration
  - Birmingham, BNL, Cambridge, DESY, Freiburg, Geneva, Glasgow, KEK, Kyoto-Edu, Lancaster, Liverpool, Ljubljana, UNM-Albuquerque, NIKHEF, Osaka, Prague, AS CR, QMW, UC Santa Cruz, Sheffield, Tokyo Inst. Tech., Tsukuba, IFIC
- PPS collaboration
  - AS CR, Prague, LAL Orsay, LPNHE / Paris VI, Bonn, Berlin, DESY, Dortmund, Goettingen, MPP and HLL Munich, Udine-INFN, KEK, Tokyo Inst. Tech., IFAE-CNM, Geneva, Liverpool, UC Berkeley, UNM-Albuquerque, UC Santa Cruz