# Trends and Perspectives in Electronics for HEP experiments

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Acknowledgements to all my group, CERN, HEP colleagues.
None mentioned, non forgotten

# Quick outline

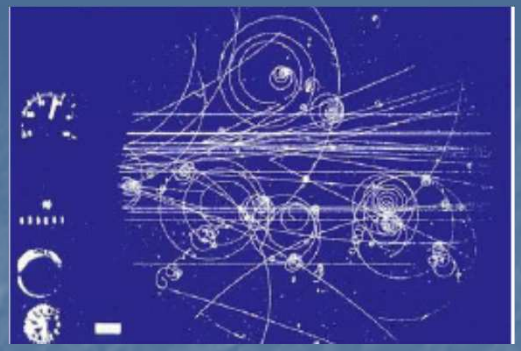
- History (past – now - future)
- Readout architectures
- Electronics required for different detectors
  - Pixels, strips, calorimeter , ,
- Electronics technologies
  - Integrated circuits, Interconnect, links, power conversion
- Our major problem: Radiation tolerance

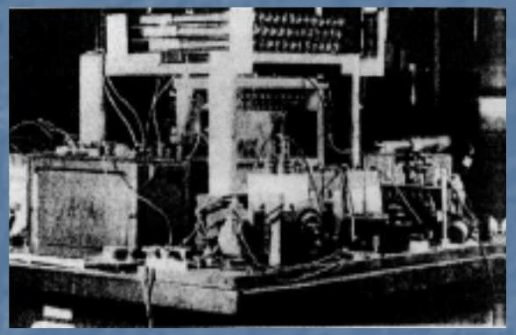
# Past

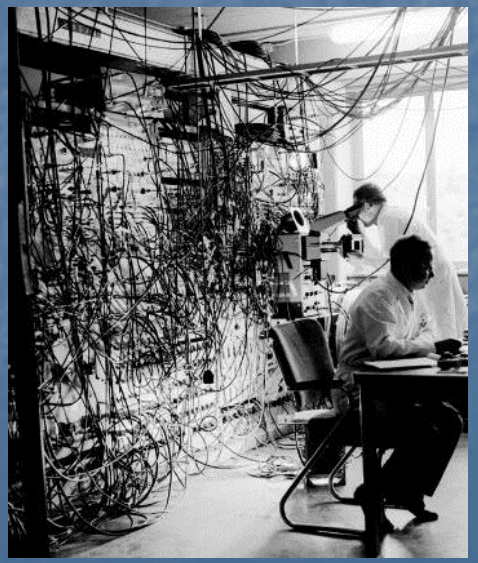
- Electronics has been one of the major ingredients to develop modern HEP experiments:
  - Improved performance: Position, Amplitude, Time , etc.
  - Lower noise
  - Higher channel counts
  - Higher integration: IC integration, low power
  - Higher readout rates
  - Sophisticated high rate trigger systems
  - High reliability
  - Radiation tolerance
  - DAQ is also electronics, but not any more "home made"

At affordable cost

- Extensive electronics engineering expertise required in HEP community

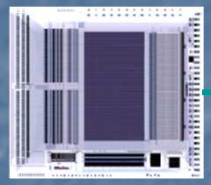


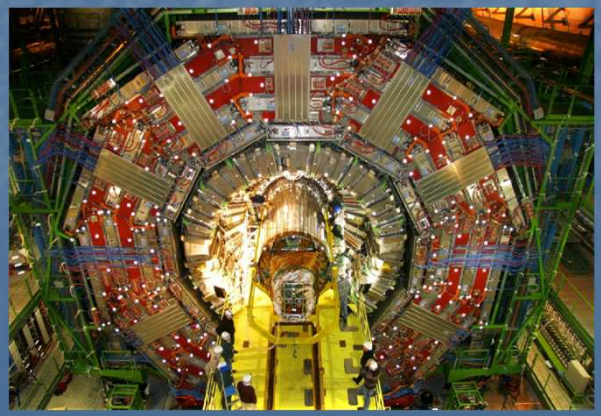




# Now (the LHC experiments)

- Radiation "tolerant" Front-End electronics (cavern, muon, calorimeter):
  - 0.7um – 0.35um CMOS/BiCMOS ASIC's
  - Qualified COTS
- Radiation hard FE electronics (trackers)
  - **0.25um CMOS (Qualified standard commercial)**
  - 0.8um DMILL BiCMOS (specialized technology, phased out).
- Optical links
  - Custom TTC (Timing, Trigger and Control distribution)
  - Custom analog (CMS tracker)
  - Custom digital (GOL serializer, ATLAS tracker)
  - Commercial digital
- Power
  - Rad tol/hard linear regulators
  - Rad tol power supplies (cavern, calorimeters)
- FPGA's for fast and sophisticated trigger systems
- FPGA's/DSP/CPU's for DAQ interfaces
- Critical integration of electronics, detectors, mechanics, cooling
  - Required material for cables, cooling an unpleasant "surprise".
- A significant fraction of the cost and R&D needed to develop these experiments is in the electronics





# Future HEP electronics

- Better resolution -> More channels-> Higher integration -> IC and interconnect technology.
- Low mass trackers -> Minimize cables, cooling, services -> Low power -> Low power IC technology and efficient power distribution
- Acquire more data at higher rate -> High density, high speed data transport -> IC technology and optical links.
- Hostile radiation environment -> Radiation hard technologies
- High reliability - > Efficient QA procedures
- Low error rates -> Well designed systems and IC's with SEU's immunity
- High speed flexible data processing -> FPGA based trigger systems, CPU based DAQ farms (assumed off detector)
- Large and complicated systems -> Well designed systems and critical sub-system integration -> Extensive system/sub-systems simulation/verification, Integration tests, Coordination.

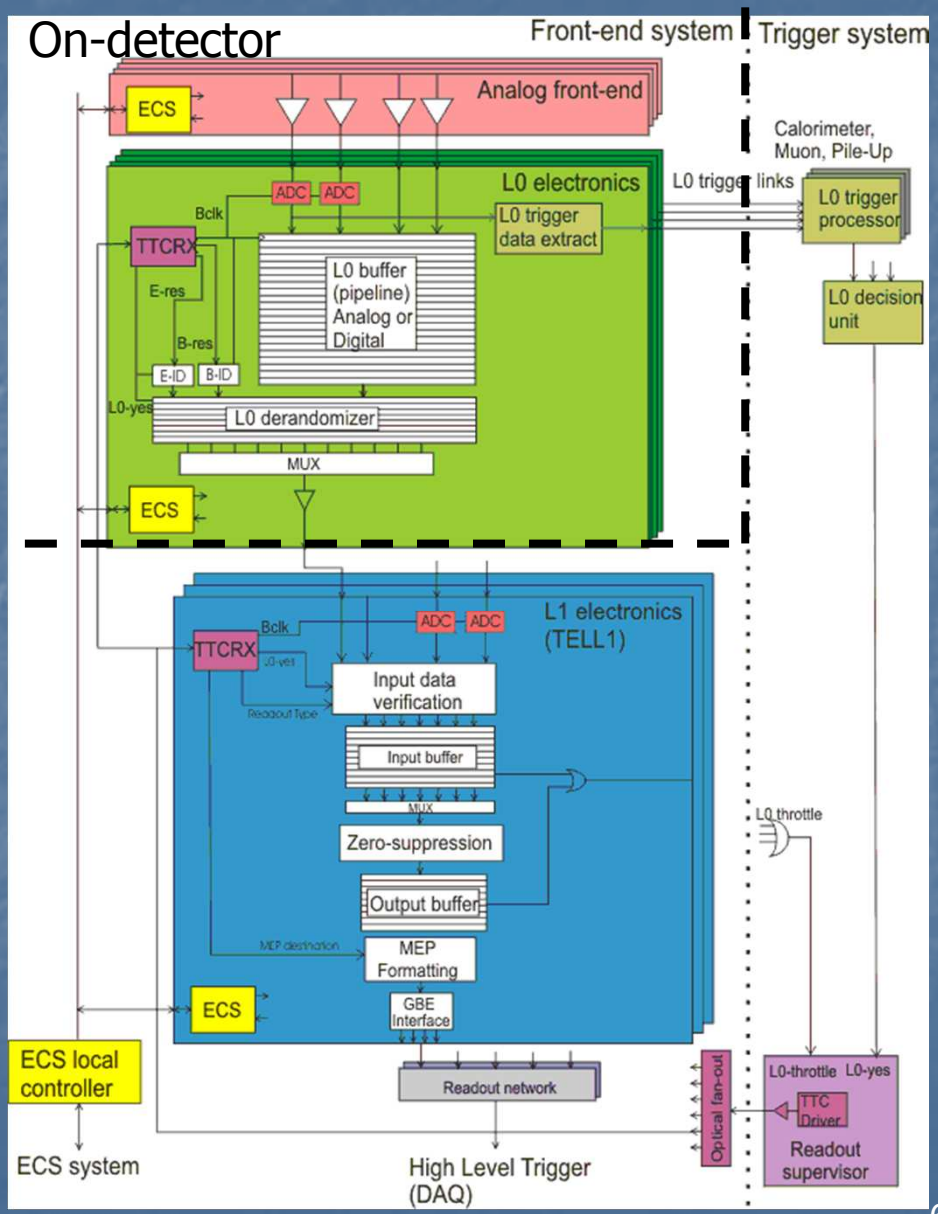
At affordable cost in a world-wide distributed community.

Electronics technologies for this must come from commercial market, but significant efforts required to adapt this to our environment: Radiation, low mass, mixed signal, integration, etc.

# Global architecture I

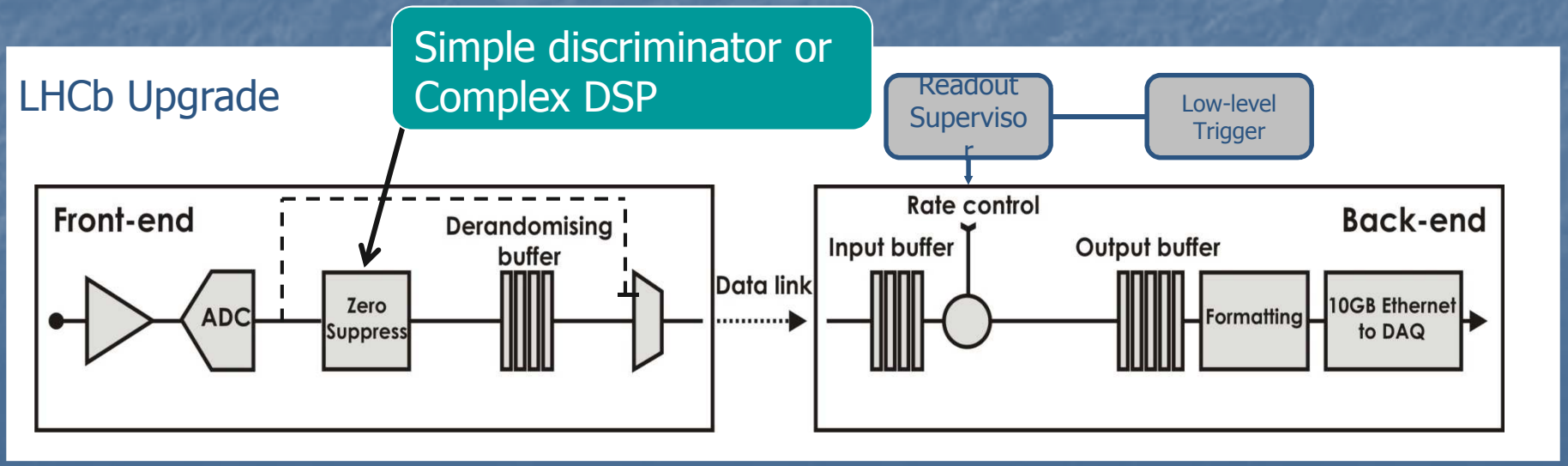
- Global front-end/readout architecture has major effects on electronics
  - Architecture in fact determined by electronics capabilities/limitations
- Triggered: Global event selection with local data buffering (and processing) to minimize readout data
  - Data buffering in hostile environment
  - Specific local processing (trigger towers, , , loss of flexibility ?)
  - (Local data sparcification/zero-suppression)
  - Complicated front-end systems
  - "Moderate" number of links

High rate experiments (LHCb, ATLAS, CMS, )



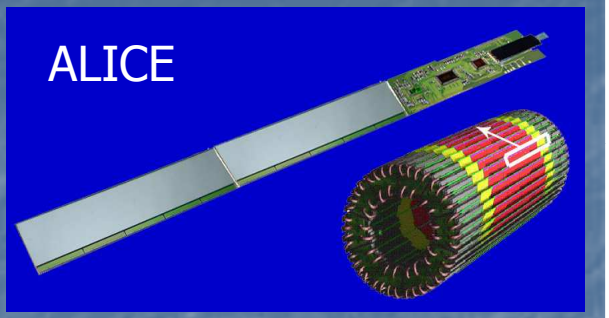
# Architecture II

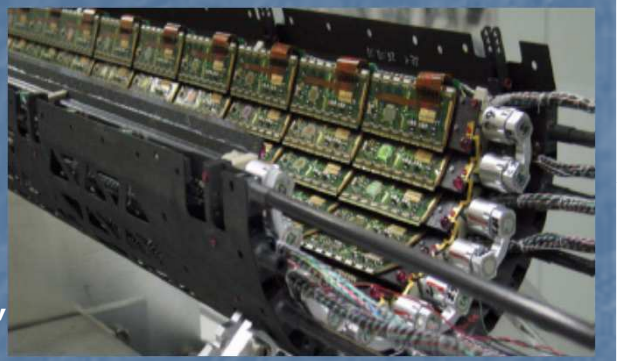
- Trigger less: Minimal local processing, high speed data transport
  - Send out all "raw" data ASAP
    A. Synchronously for easy pipelined event processing
    B. **Sparcified/zero-suppressed with time tag to minimize data (links)**
  - Simple high speed front-ends.
  - Large number( >10k) of data (optical) links
  - Flexible data processing in counting house using latest commercial FPGA's/DSP/CPU/PC (No radiation)
  - Moderate rate/size experiments (LHCb upgrade, CLIC/ILC, , )

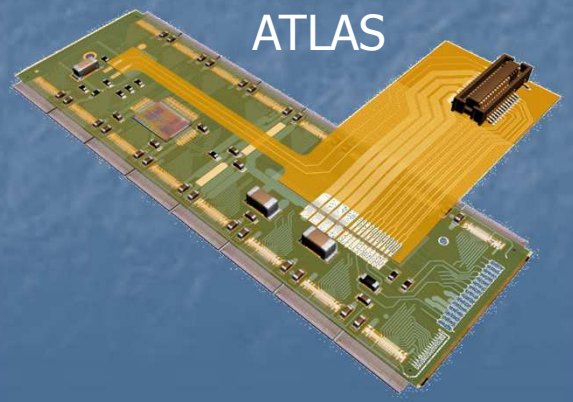


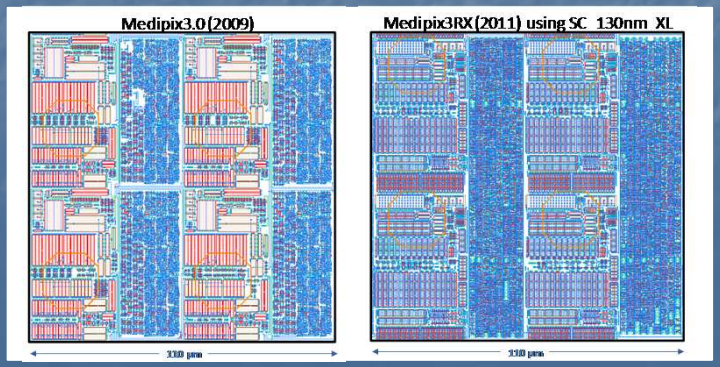
# Pixel detectors

- Pixel detectors are our IC technology drivers as high integration level vital
  - Better resolution -> Smaller pixels, Higher integration
    - Binary versus analog (TOT) readout.
  - Smaller pixels -> Smaller capacitance -> Better S/N -> smaller analog power
    - Limited by pixel to pixel capacitance
  - More pixels, Higher rates (radiation), More features, Data buffering in pixel , ->
    More logic/storage per pixel -> Higher integration,
    **Low power** digital required
    - Material in today's pixel detectors are determined by cabling, power distribution, cooling, , , sensors, ASICs
    - Complicated digital pixels:
      Full custom -> Synthesized high density standard cells,
      Pixel grouping (pixel regions, super pixels)



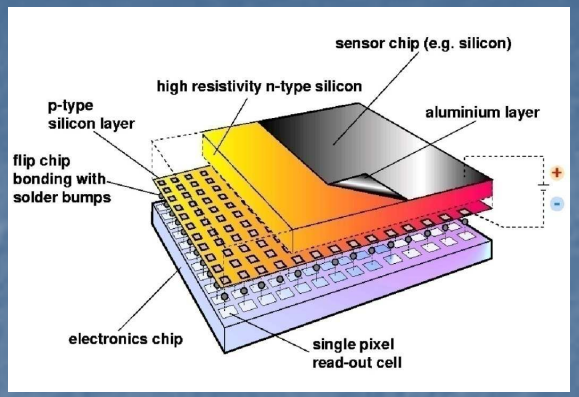



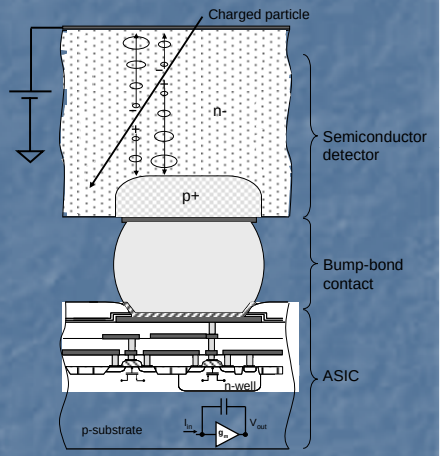


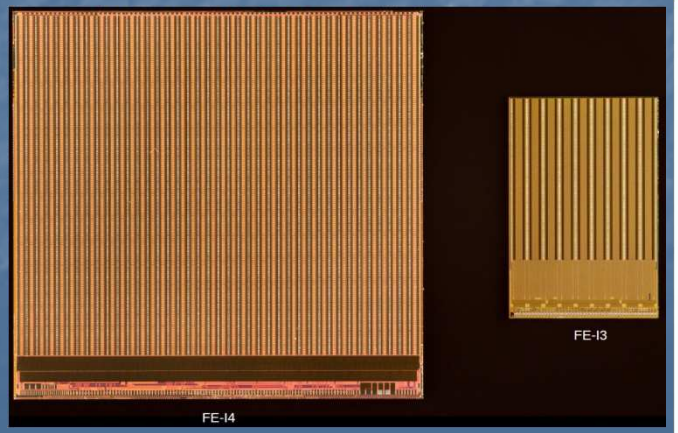




# Hybrid Pixels

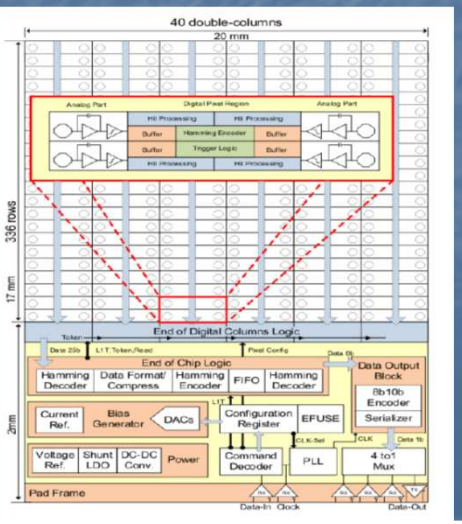
- Decoupled ASIC and detector technology
  - Standard high density ASIC technology
  - Dedicated sensor technologies (Planar, 3D, Diamond, , )
- High cost of bump bonding ASIC and detector
  - Multiple technologies under evaluation in HEP
  - Bonding technics from 3D IC technologies will hopefully bring improvements on this (more on 3D later)
- Material: Thinning ASIC to 50 – 100um
  - Delicate combination with bump bonding
- High radiation level and high rate applications:
  - LHCb upgrade with pixel vertex detector
  - ATLAS/CMS phase 2 upgrades: RD53.
- "Limited" by bump bonding, material, cost

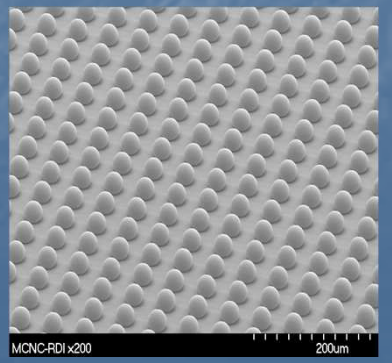



ATLAS FEI4 50 x 250um

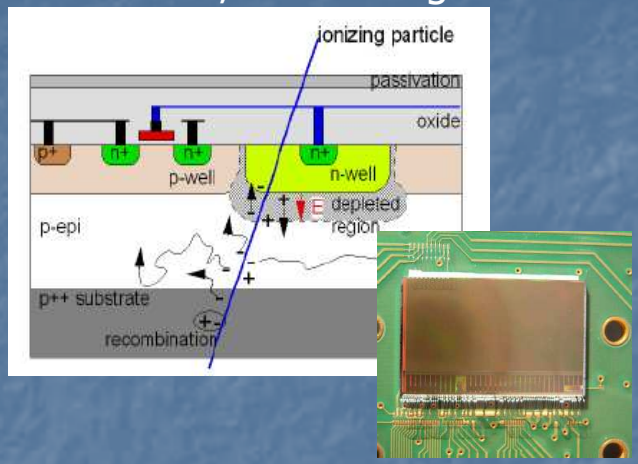


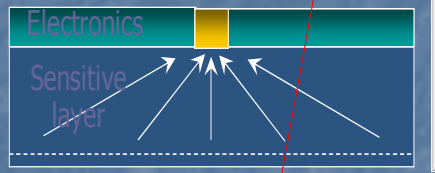
# Monolithic Pixels

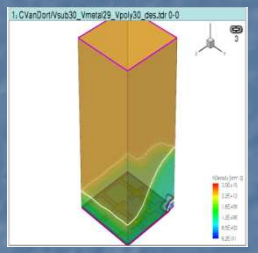
- Aim: Lower cost, Higher resolution, Lower mass
- Diffusion based : Charge collection (~100ns)
  - Epi (epitaxial layer), DEPFET (internal gate)
  - Relatively low rate and low radiation
- Drift based: SOI (KEK), LePix bulk triple well (CERN),
  - "HV" bias critical
  - Can possibly work in LHC environment
- Simple pixel cells (few transistors)
  - Rolling shutter
    - Limited rates, Significant boundary circuits needed.
  - Digital cells in pixel, Cross talk problems
- HEP needs 100% fill factor
- Stitching to make "large" pixel modules
- Challenges: Radiation tolerance, Speed, Rates: on-chip/in-pixel buffering/processing, technology dependence.

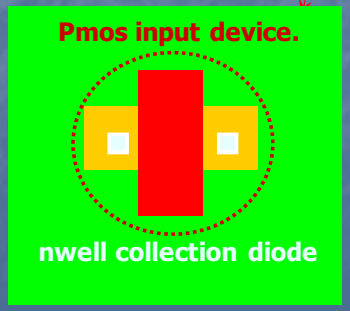
Mimosa, Strasbourg

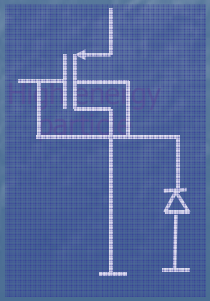


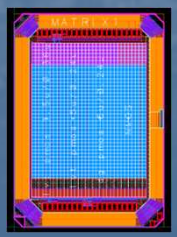

LePix (CERN)

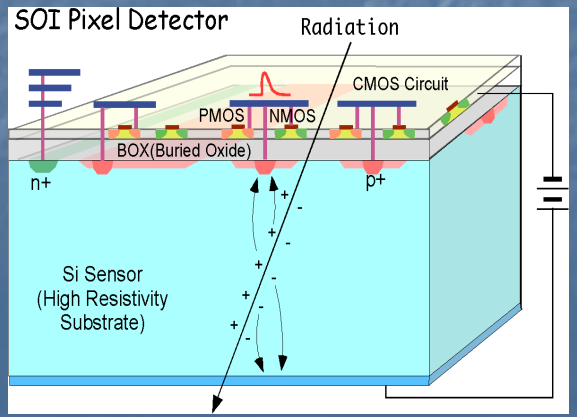


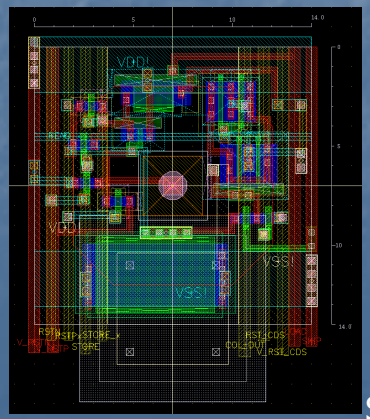







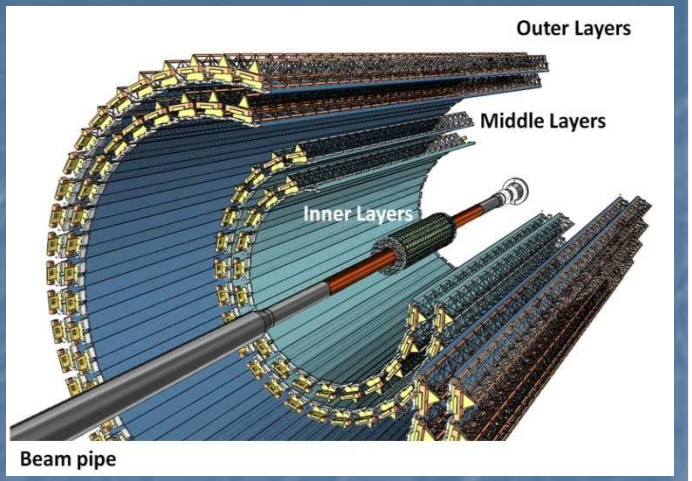


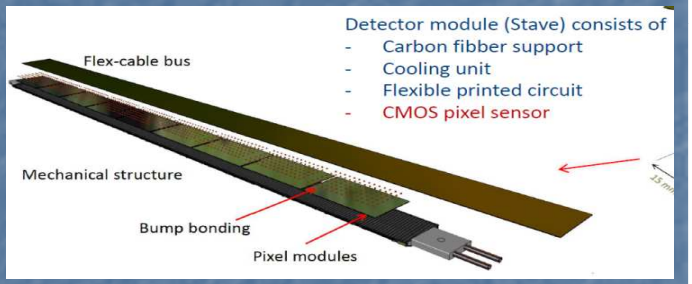



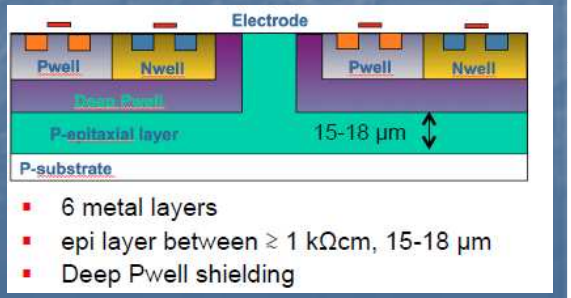
SOI, KEK

# Alice inner tracker upgrade

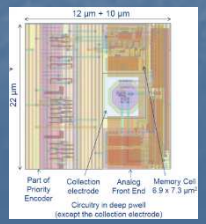
- **Novel MAPS** based tracker system for ~2018
  - Replaces 3 tracking detectors: Pixel, Strips, Silicon drift
  - High track multiplicity of 115/cm$^2$ per event at 50KHz interaction rate : 5MHz/cm$^2$ (inner layer)
- Detector – Front-end - Interconnect
  - 22 x 22 um$^2$ MAPS: Binary
  - 10 m$^2$, 25k 15x30mm$^2$ Pixel chips, **25G pixels**
  - **Modest radiation**: < 1Mrad , < $10^{13}$ 1Mev $n_{eq}$/cm$^2$
    - **Enables use of MAPS**
  - **180nm CMOS imager sensor technology**
  - **Status: Design and testing on-going**
- Module/stave Interconnect:
  - **Bump bonding of thinned chips** (50um)
- Readout:
  - Event trigger (50KHz): **<1Gbits/s per pixel chip**
  - Electrical links to intermediate patch panel
- Power:
  - **Aims at very low power consumption**: ~50mW/cm$^2$



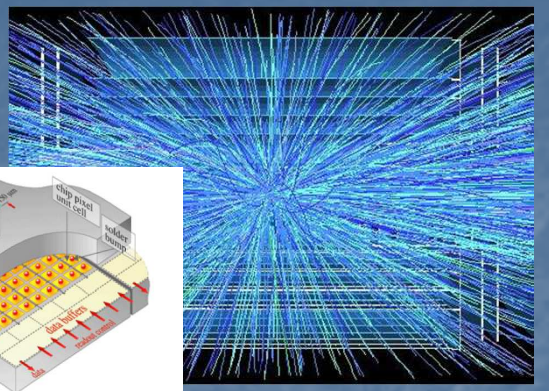



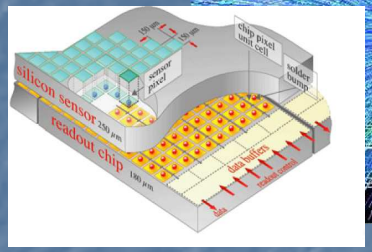


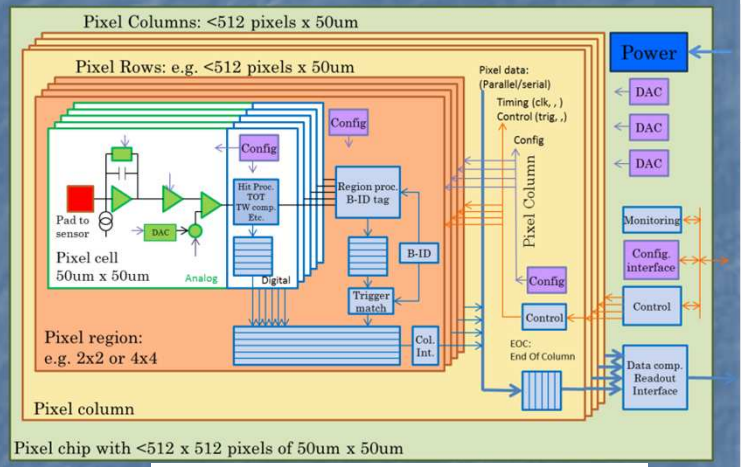


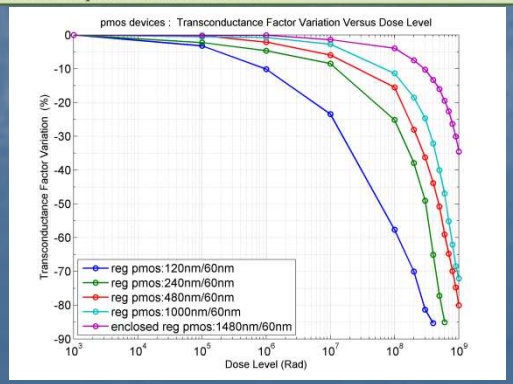
# CMS/ATLAS Phase 2 pixel challenges

- Extreme particle rates: ~500MHz/cm$^2$ (inner layer)
  - Hit rates: ~2(3) GHz/cm$^2$ (factor ~16 higher than current detectors)
  - Assuming max 140 (200) pileup and 25ns crossings
- Smaller pixels: ~¼ (~50x50um$^2$ or 25x100um$^2$)
  - Increased resolution
  - Improved two track separation (jets)
  - Outer layers with larger pixels, using same pixel chip
    - Lower power – low material, lower cost
- Increased readout rates: 100kHz -> 500KHz - 1MHz
  - Data rate: 10x trigger X >10x hit rate **= >100x !**
- Increased buffering: 10x latency x 10x hit rates = **100x**
- Unprecedented hostile radiation: ~1Grad, ~$10^{16}$ Neu/cm$^2$
  - Hybrid pixel detector with separate readout chip and sensor.
    - Monolithic seems unfeasible for this very high rate hostile radiation environment
  - Phase2 pixel will get in 1 year what we now get in 10 years
- Low mass -> Low power, Critical and very challenging
  - Can we maintain same low power as now ? , Increase by <2x ?
- Pixel sensor(s) not yet determined
  - Planar, 3D, (Diamond, HV CMOS), Final choice may come late
  - Charge information/Binary ?
- Complex, high rate and radiation hard pixel chip required and critical -> RD53 collaboration
  - 1 year old, 20 institutes, ~100 collaborators,
  - Working groups: Radiation, Top, Analog, Simulation, IP blocks, Top level, IO
  - Radiation tolerance of 65nm baseline technology Critical



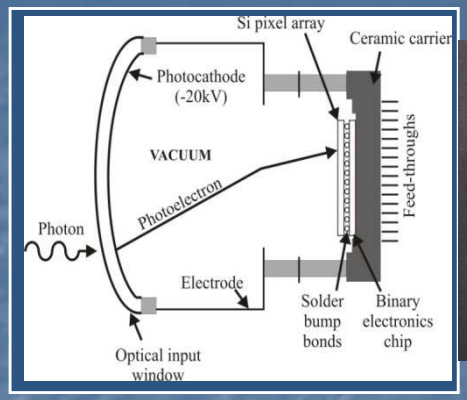


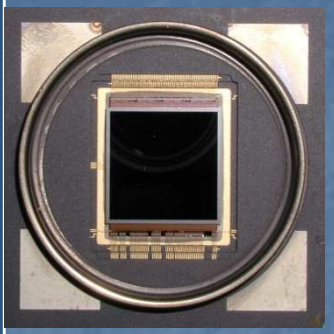



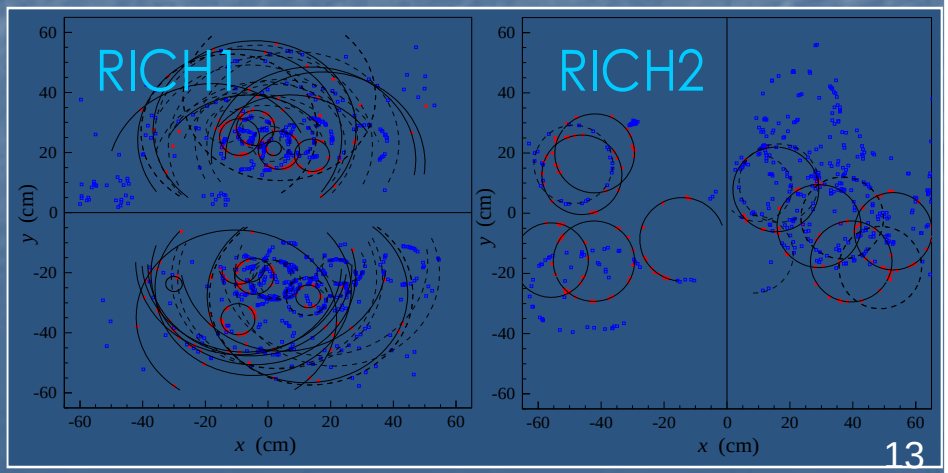



# Pixel photon detector

- Integration of a pixel detector in a photon tube: Hybrid Photon Detector
  - Electrostatic acceleration and focusing of photon-electrons on pixel detector.
- Single photon detection in LHCb RICH
  - Very low noise
  - Same pixel chip as used in "classical" pixel detector in Alice
- Integration in vacuum tube difficult
  - Bake out, vacuum tightness, out gassing, etc.
  - "Discontinued"
  - Revival based on new pixel chips ?.
- Many potential applications using HEP pixel chips in HPD's, MCP, ,

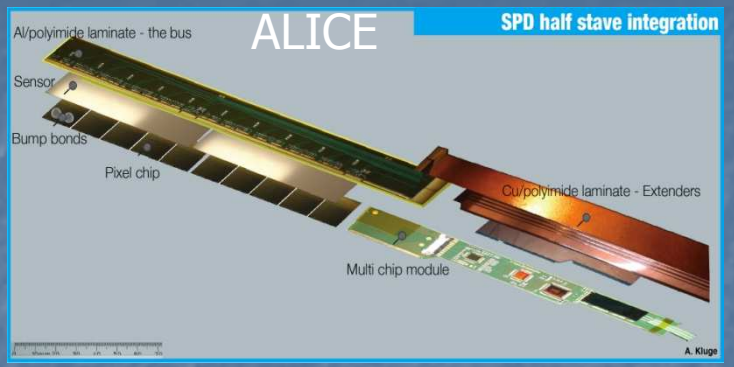


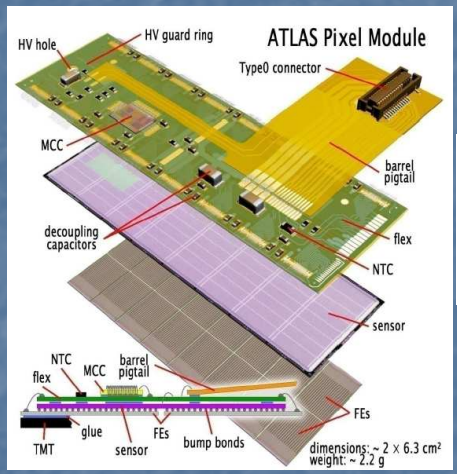



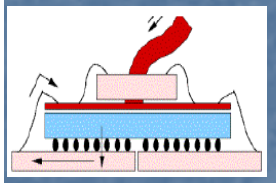


# Building pixel systems

- Building low mass hermetic pixel detectors from relatively small pixel modules/assembles far from obvious
  - 100% coverage, Small assemblies, Modules, Power, cooling, readout, ,
- Ladders, modules, edgeless detectors, ,
- Future:
  - Stitching (to make very large pixel ASIC's)
  - TSV (Through Silicon Via's) to have abuteable pixel assemblies ?
    - TSVs are "surprisingly" difficult
  - Micro channel cooling ?



ATLAS

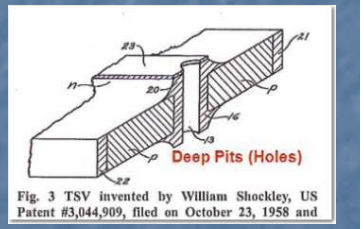
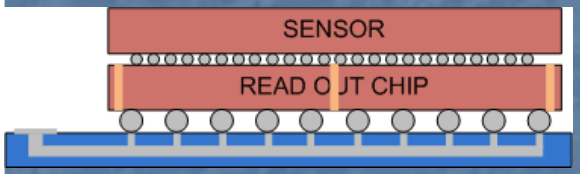
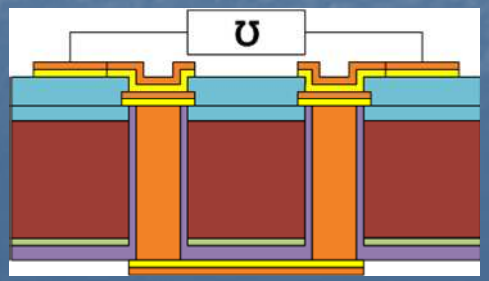
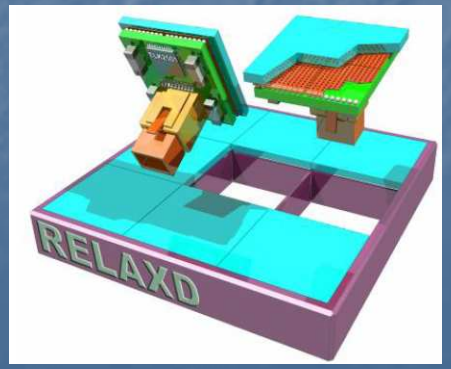
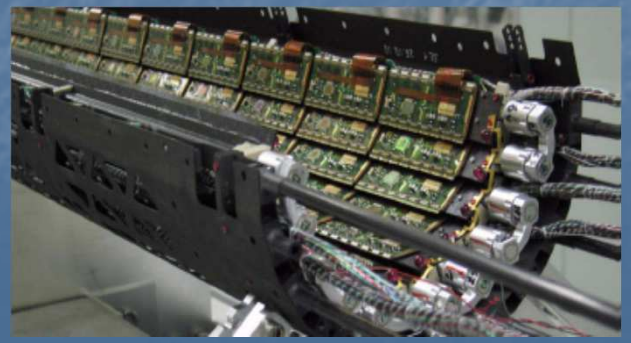


Fig. 3 TSV invented by William Shockley, US Patent #3,044,909, filed on October 23, 1958 and



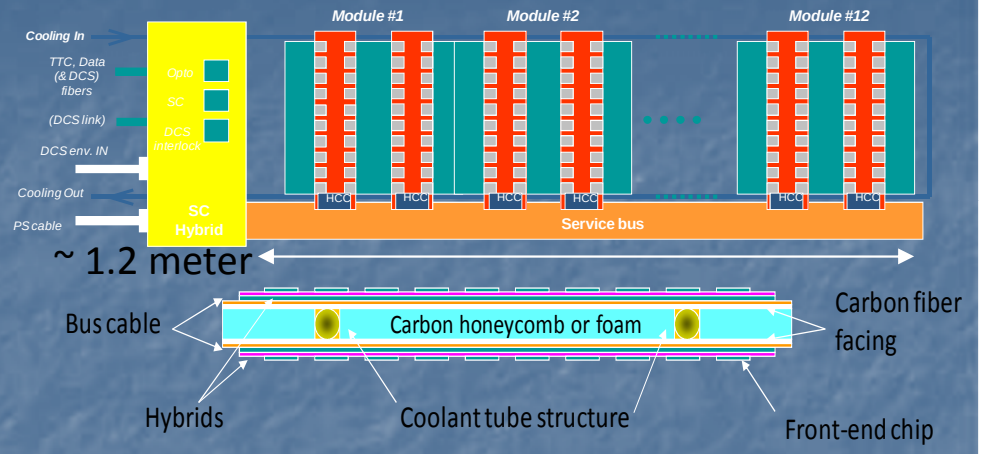



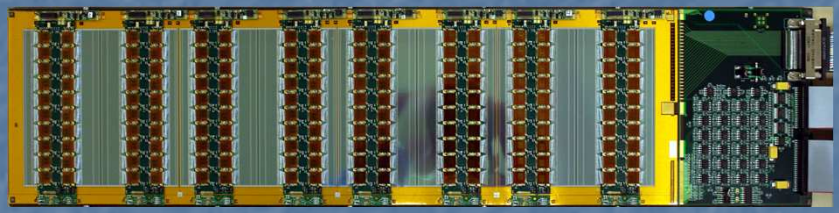


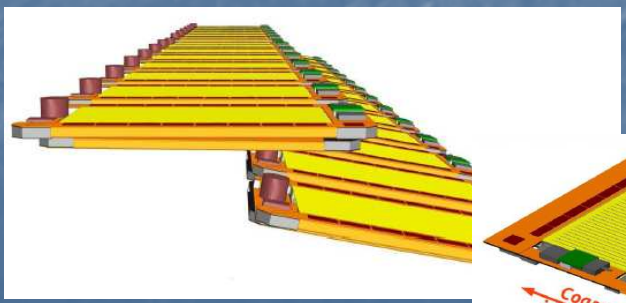
# Strip detectors

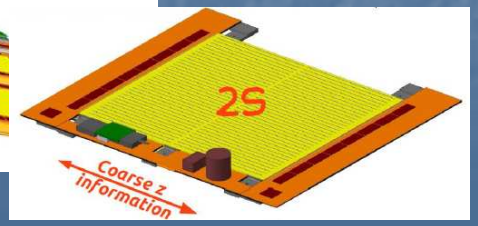
- High resolution tracking over large surfaces
  - Pixels too expensive. MAPS can change this
- Ladders, long strips, short strips, strixels
- CMS and ATLAS upgrades: Binary.
  - Analog power decreases when going to 130/90 nm. 65 nm may not give significant gain.
  - Digital power gets dominating so use of modern technologies gives lower power.
- ADC per channel in future ?
  - Very low power 8/6bit SAR ADC or TOT.
- Connection between FE chip and detector: **Wire bonding** or tap or bump ?
- Integration in stave/rod or modules ?
- Powering:
  - CMS DC/DC
  - ATLAS Serial power or DC/DC



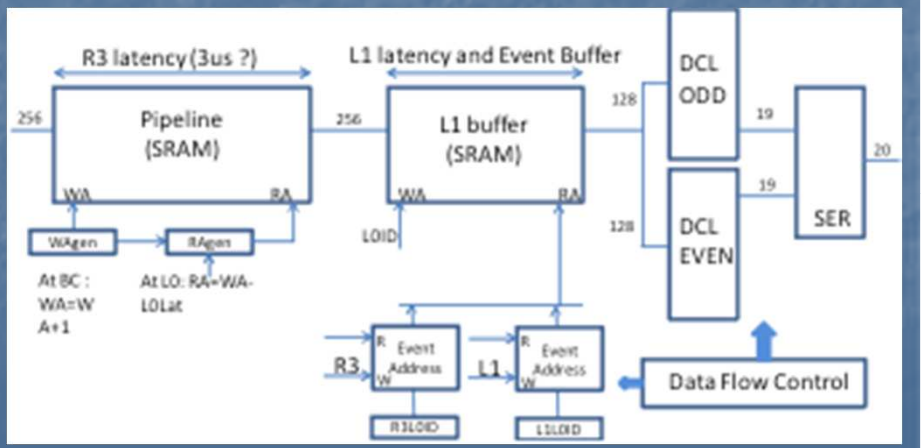



ATLAS stave with common services





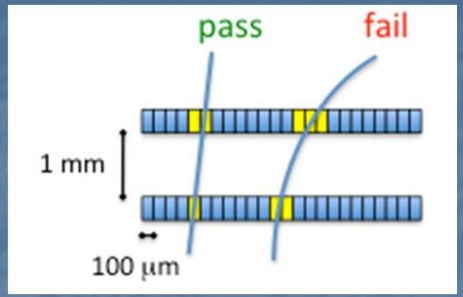

CMS modules with independent services

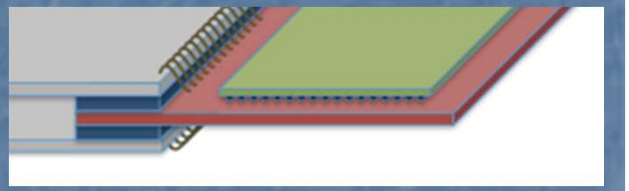


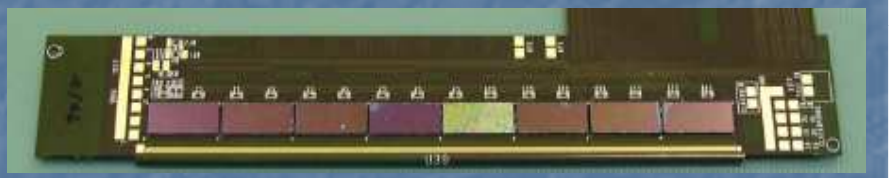
# Combining pixel/strip trigger

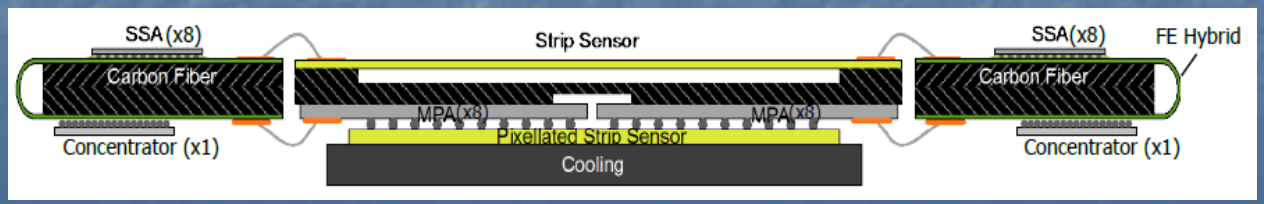
- CMS track trigger
  - At HL-LHC first level trigger saturates
  - Include tracker Pt information in first level trigger
    - Send track information for tracks with high Pt.
    - ~1 order of magnitude data reduction from Pt cut
  - Sufficient Pt resolution, short latency, bandwidth , ,
  - Double layer modules with correlation
    - Strips – strips in outer part
    - Strips – Macro pixels in inner part (to get Z)
    - Critical: Low mass as not to destroy tracker resolution: Low power, high interconnectivity ,

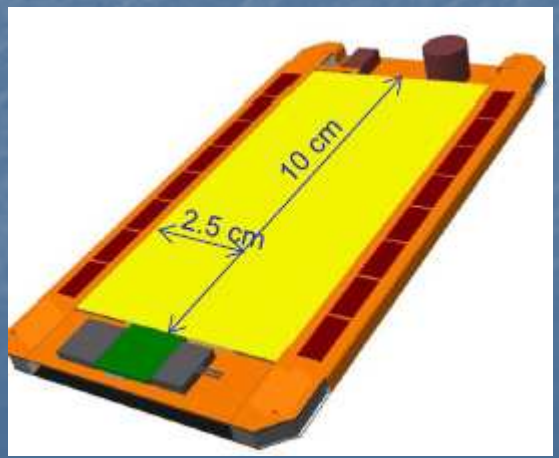
    Critical interconnect technology and module assembly
  - Challenging off-detector correlation/trigger logic
- ATLAS: Two level trigger with Region Of Interest (ROI)



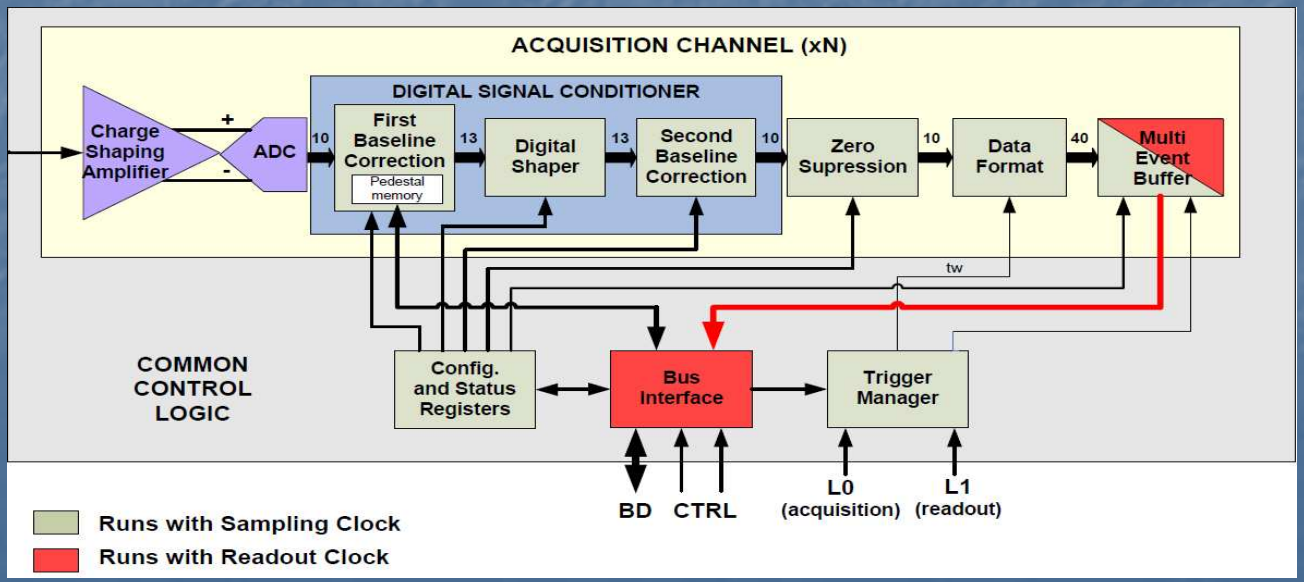




# Full DSP approach

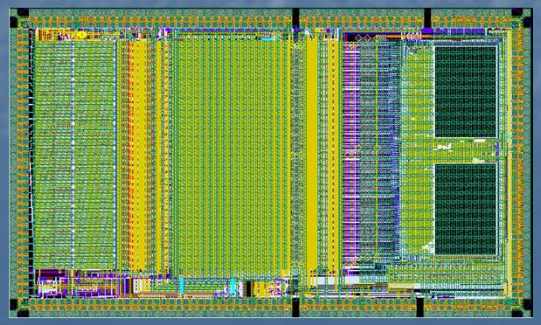
- The world is going digital: ADC plus powerful DSP processing can be integrated in front-end chip.
  - Digital shaping, baseline restorer, pulse detection, zero-suppression, time tagging, clustering, pulse parameter extraction, compression, buffering, link/DAQ interface
- Very low power ADC's extensively developed by industry over the last decade.
  - Can be bought from specialized IP companies (do not develop ourselves if not required)
  - Extreme: ADC per pixel -> ~200k ADCs per chip: TOT or SAR
- DSP processing at low power: modern technology plus power optimized architecture and design.
- Required integration possible with modern technologies
- Example: S-ALTRO prototype: 16 channels, ~1W, 130nm CMOS
  - No significant crosstalk from digital to analog
  - Power dominated by home designed ADC (~60%)
- Realistic future aim: 64 channels, 12/10bits, ~1W.
  - Applications: TPC, GEM, Micromegas, Calorimeters, ,
  - Pulsed power can reduce power considerable in certain applications (e.g. ILC/CLIC)

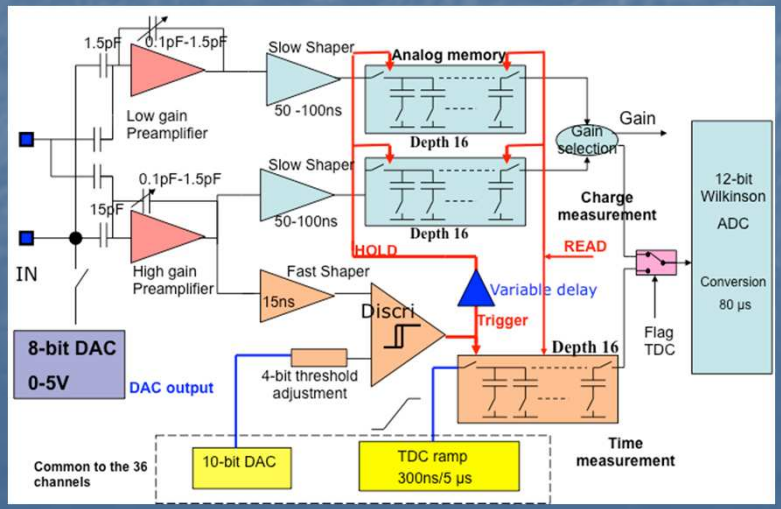


# Calorimeter

- Large dynamic range: Low power, 40MHz 14/16 bit ADC's now available as standard multichannel chips and as IC IP's.
  - Good alternative to custom made multi range analog memories
  - Our usual problem: Radiation tolerance. COTS versus modified IP's
- Particle flow: Many channels ($10^8$), lower resolution per channel, Low power critical (power pulsing in ILC/CLIC)
  - CALICE (ILC) currently using multi gain multilevel analog memories (low power, low cost)
  - Multichannel ADC/DSP seems promising for this in the future.
- Parallel high speed optical links now makes it viable to perform direct ADC in front-end and send all raw data to off-detector processing for "classical" calorimeters.
  - Allows very flexible FPGA based calorimeter trigger systems
  - Original CMS Ecal architecture, but abandoned because of cost/implementation of the ~100k links.
- High time resolution forward calorimeter (next slide)

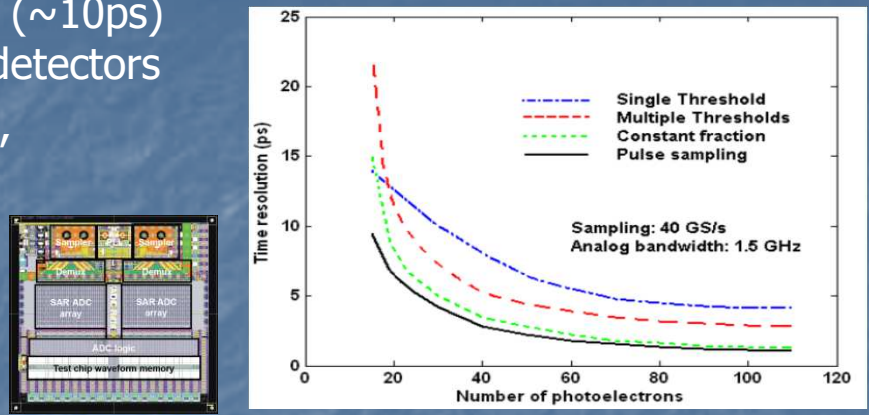
SPIROC,
Omega – In2P3
CALICE



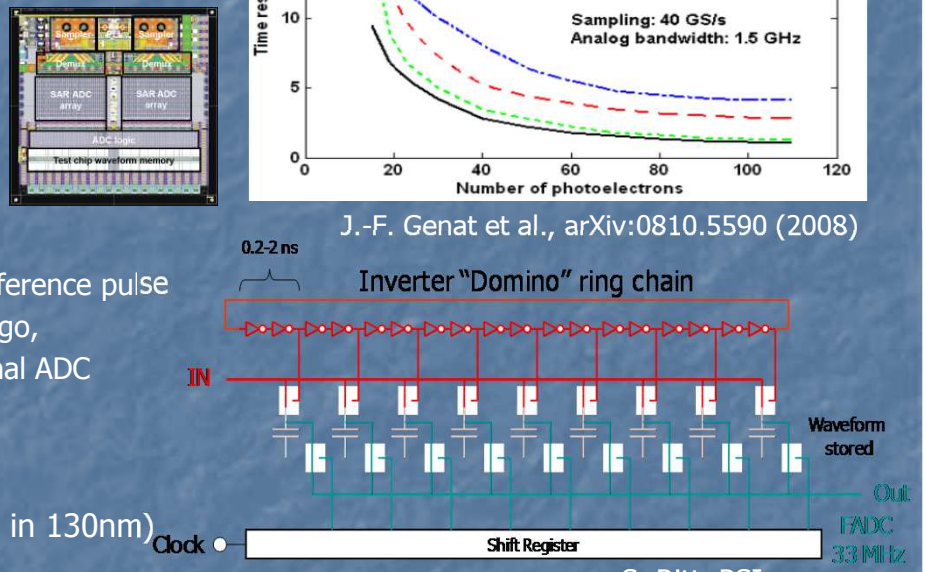


# Timing detectors

- High channel count, very high time resolution (~10ps) detectors feasible with novel electronics and detectors
- TOF, RICH, Calorimeter detectors: MCP, SiPM, MG-RPC, MAPMT,
  - LHCb Torch, FP420, HPS, CMS forward calorimeter
- Fast ADC's: 55GHz, 8 bit, 2W
  - How to deal with the massive data flow and power?
- Fast analog memories: 1 – 10GHz Sampling, ~1GHz bandwidth
  - High time resolution with software pulse fitting to known reference pulse
  - Multiple chips made in community: PSI, LAL, Hawaii - Chicago,
  - Limited number of channels, limited memory, power, external ADC
- TDC with Constant fraction or TOT time walk compensation (E.G. ALICE TOF) .
  - ~ps TDCs feasible in modern IC technologies (e.g. 2ps in 130nm)
  - ~10ps TDCs can now be implemented in FPGAs
- Very high speed circuits now possible with limited power, but requires fast detectors

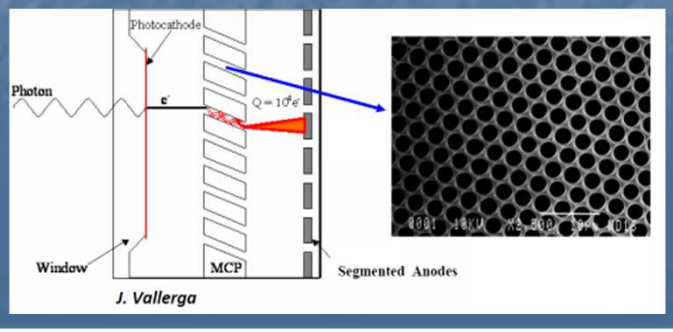


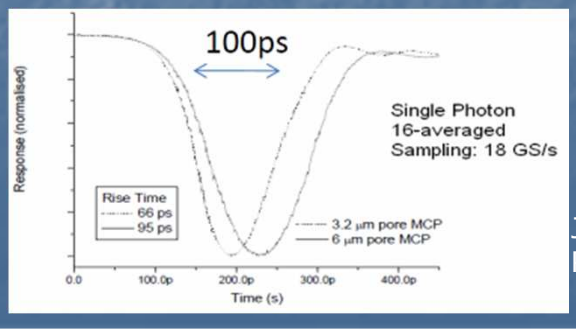

J.-F. Genat et al., arXiv:0810.5590 (2008)




S. Ritt, PSI

"Time stretcher" GHz → MHz

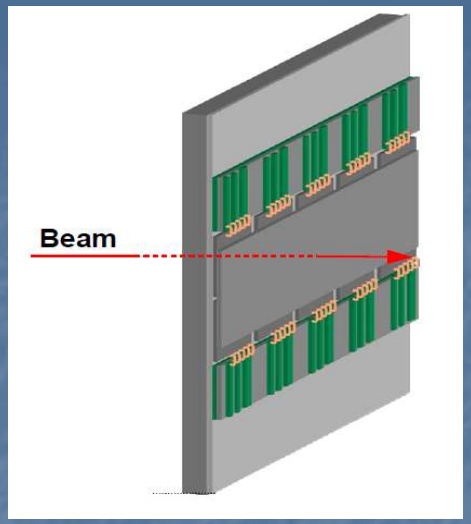


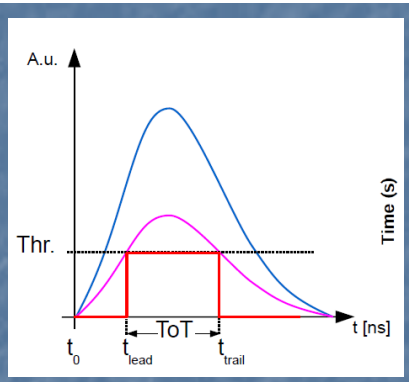



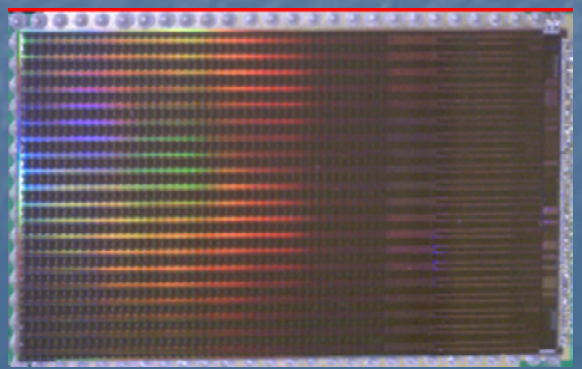

J. Milnes, J. Howoth, Photek

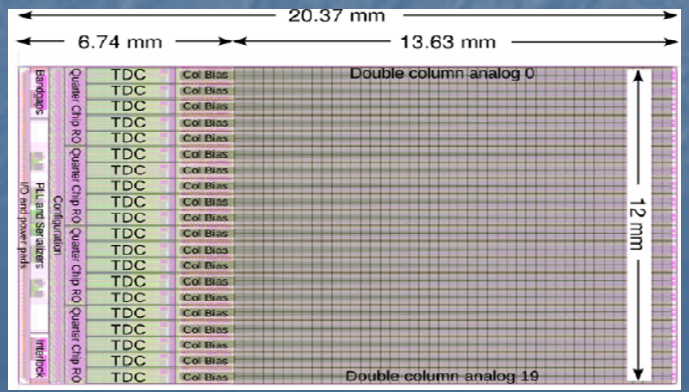
# NA62 GTK

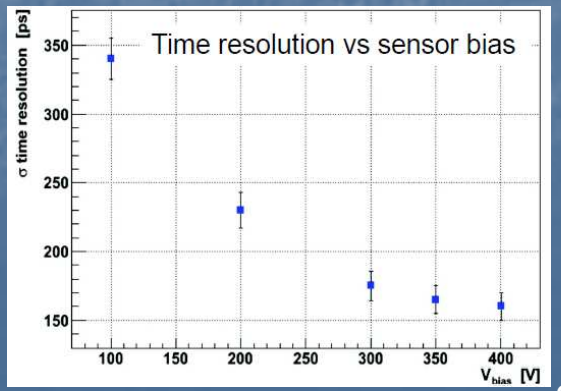
- 300um x 300um pixel detector with ~200ps resolution (ASIC: 75ps)
- 3 stations (10 ASIC's, 1 pixel sensor) with very high particle rate: ~1GHz
- Time walk compensation with TOT (CFD also evaluated)
- High radiation levels (secondary beam goes straight trough)
- Demonstrated in beam test with 130nm prototype
- Final 40 x 45 pixel array ASIC available (test with sensor ASAP)
- Pixel detectors with this kind of time resolution can open up new applications of pixel detectors in HEP, medical, material science, bio chemistry, , ,
- What determines ultimate time resolution with silicon pixel ?
  - **Signal variation across pixel, signal/noise, Signal generation in silicon itself** (e.g. 3D detectors)
  - Pixel ASICs and requirements for "low power"



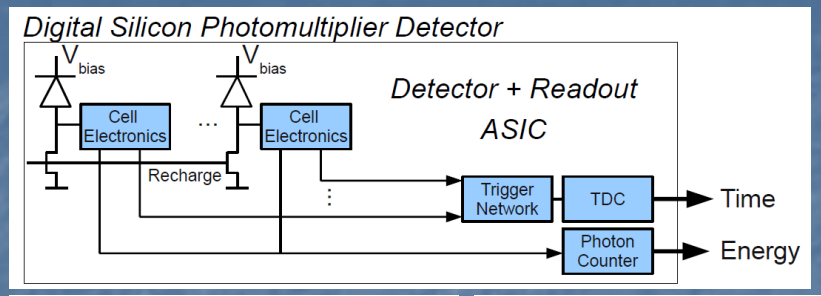



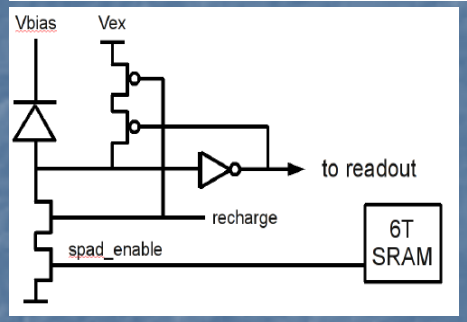


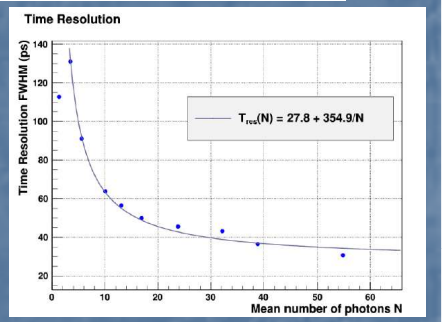



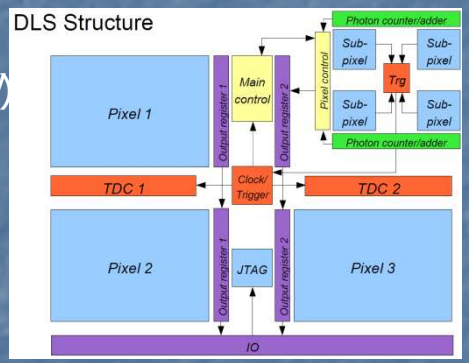
# Digital Photon counting

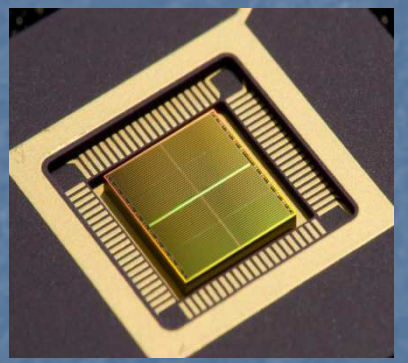
- Single photon counting with SPAD/GAPD array with integrated electronics
  - Use of "standard" IC technology
    - SPAD bias only needs a few volts
  - Optimization of SPAD difficult
    - Dark count rates, cross talk, efficiency , ,
- Photon counting, High time resolution
  - 32 x 60um micro-cells/pixels
  - Up to 80% fill factor
  - Integrated TDC, readout, configuration , ,
- Enormous effort in development
  - Foundry (NXP 180nm) and user (Philips *medical*) originally part of same large company
  - Aimed at applications with high system costs (medical scanners)
  - Investment that will be hard to find in HEP
  - PH detector seminar: https://indico.cern.ch/conferenceDisplay.py?confId=149010
  - "Open" to let HEP use their technology
- Other groups/projects develops similar SPAD detectors/chips

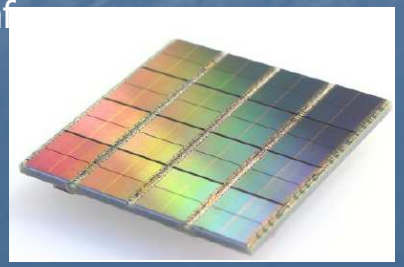


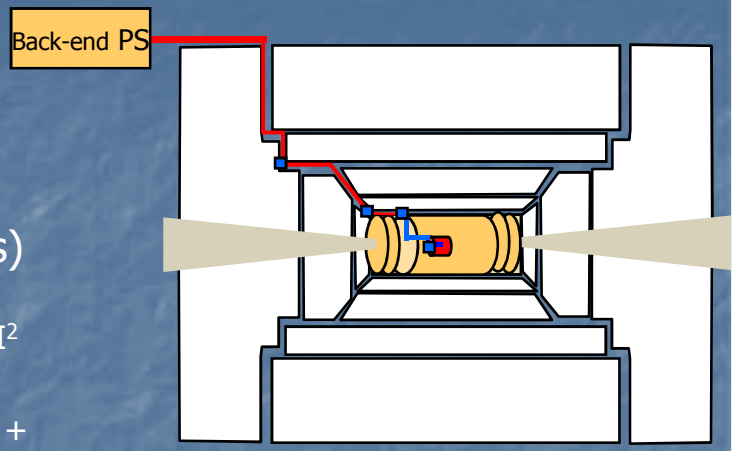



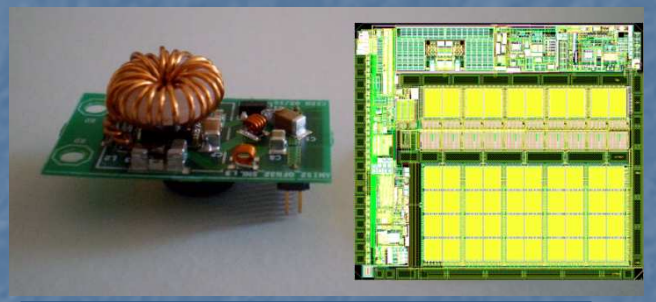


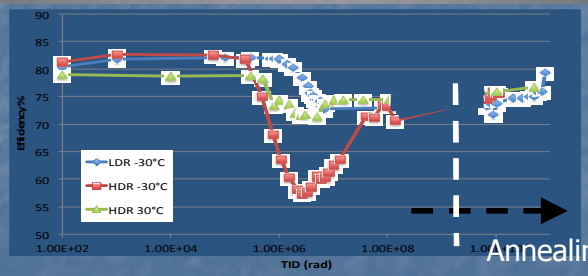
T. Frach, Philips

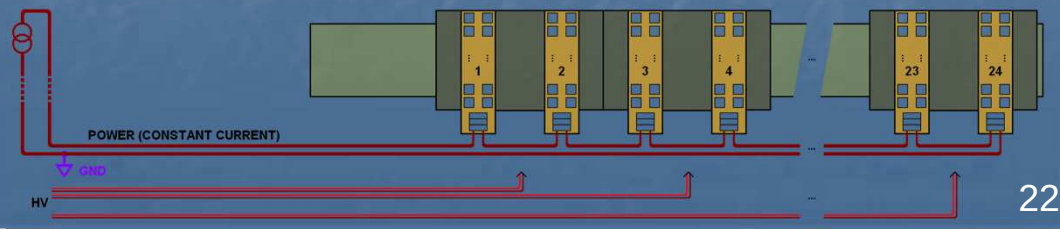
# On-detector power distribution

- Distributing low voltage power in large experiments, without local power conversion, impractical/impossible
  - Voltage drops -> power loss –> large cables -> material
- Modern technologies use lower supply voltages: 5V, 3.3, 2.5, 1.2, 1.0V (down side of new low power technologies)
  - Upgrades: Assume same total power (as more channels) the power supply currents will increase and power loss in cables increases with $I^2$
  - Local power conversion becomes a must.
  - Power conversion must occur in very difficult environment: Radiation + magnetic field + minimal power dissipation + minimal mass.
- DC/DC: Inductive (module), Capacitive (on-chip)
  - High input voltage (low cable currents), high efficiency
  - IC technologies that can stand high voltage are not radiation tolerant
    - Compromise: Medium voltage (10v) but still problematic
  - Inductive and capacitive DC/DC conversion
    - Radiation tolerance of technology a critical issue (two promising technologies used)
    - Shielding and appropriate EMC handling critical but have been successfully verified on silicon strip detector modules
- Serial powering: Distribute current and generate locally voltage. Tested by ATLAS SCT.
  - Grounding and fault isolation delicate
- Power pulsing: significant gain possible for certain experiments (ILC/CLIC), but not trivial



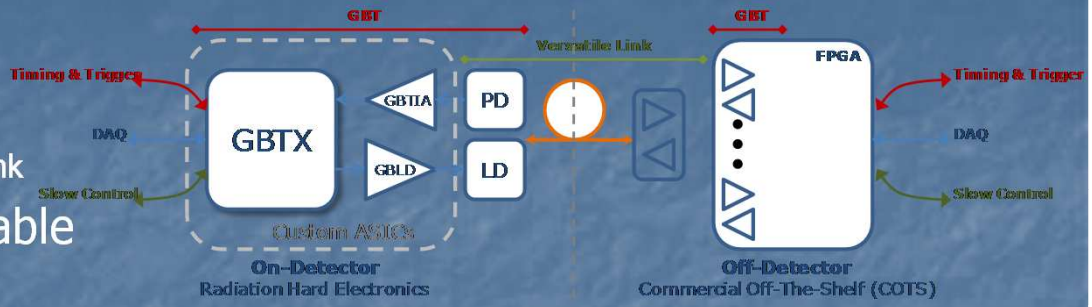



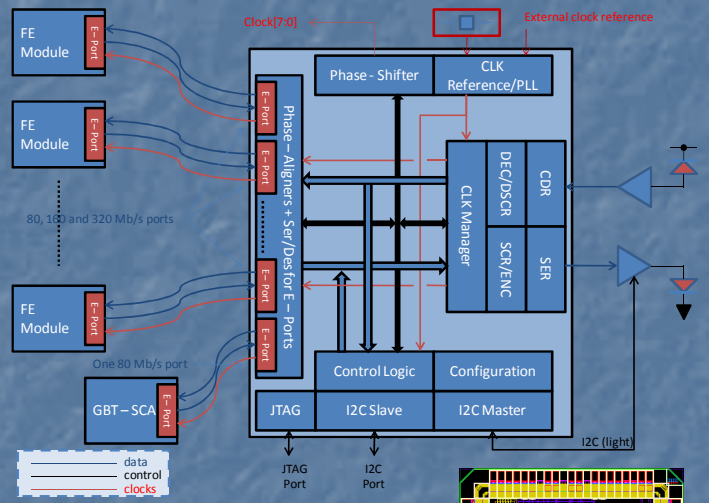


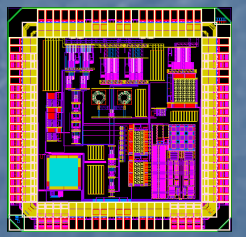



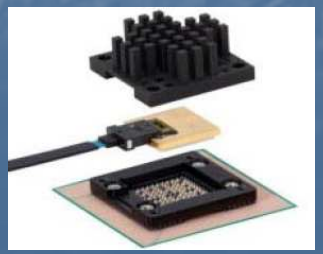
# Optical links

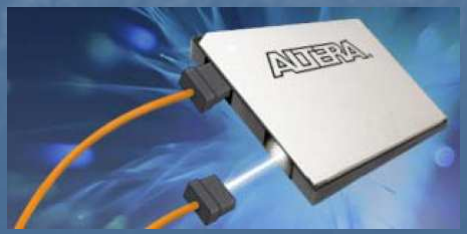
- Information types :
  Readout, Trigger, Timing, Slow control,
  - Past/current: Separate links
  - Future: Merge all in one bidirectional optical link
- Must be high speed and highly reliable
  - Redundancy in critical cases
- Radiation problems:
  - Laser deterioration
  - PIN receiver deterioration
  - Induced multi bit error signals in PIN by particles. Use of extensive forward error correction.
  - SEU's in electronics circuits
- Versatile / GBT link project
  - Identify and qualify appropriate Lasers and PINs
  - On-detector rad hard chip set:
    Laser driver, Pre-amplifier, interface chip (GBTX), control chip.
  - Off-detector: Commercial Opto and FPGA's
- Parallel links for high data rates
  - Custom array transmitters/serializers (ATLAS)
  - Fiber ribbons
  - Commercial array receivers (optical engines)
  - FPGA deserializers

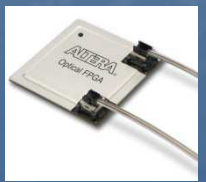






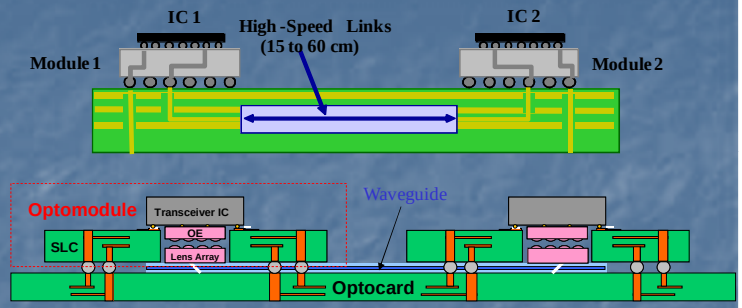



# CMOS photonics

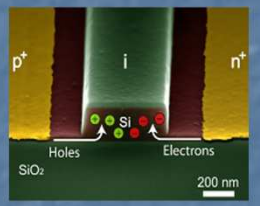
- IO is becoming critical bottleneck for high end multi-core CPU's servers
  (CPU <–> Memory)
- Now: High speed electrical serial connections
- Future: Hybrid optical chips/links
- Dream: Integrating opto electronics in (on 3D) Integrated circuits
  - On-chip optical modulators, waveguides and receivers (laser source problematic in Si)
  - Available when ?.

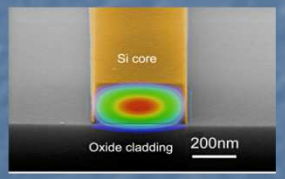
Electrical links are still more cost efficient (power) for short connections

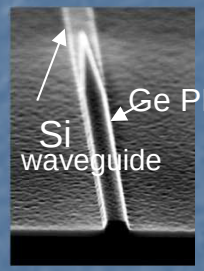
- Dream for HEP: Each Front-end chip has an optical output. Many challenges
  - Radiation
  - Access to technology
  - Cost of technology
  - Design complexity of such mixed technology

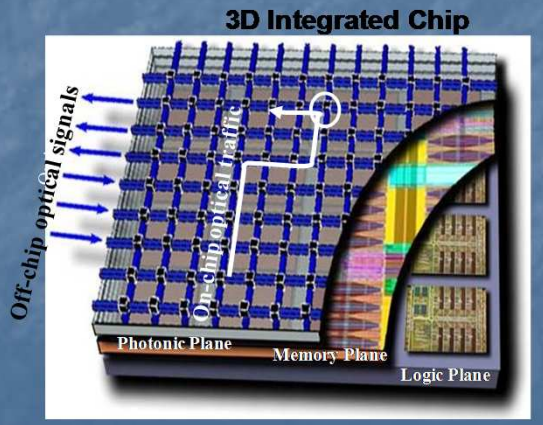



Has been demonstrated
(Sophisticated 3D packaging)



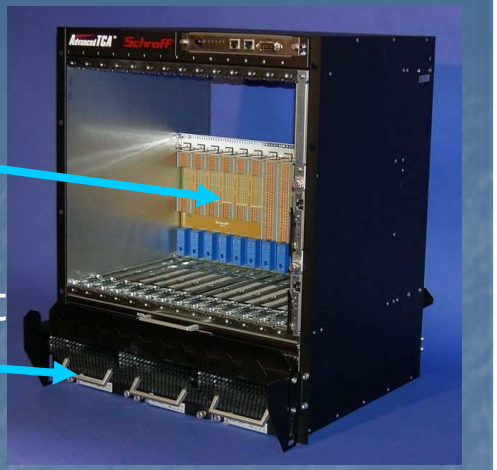



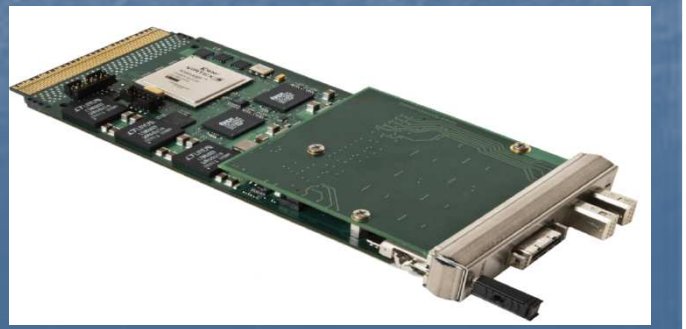

Dream ?

M. Ritter, IBM, TWEPP2010

# Off detector

- FPGA's: Fast, flexible, Improves quickly, Firmware "portable" , The perfect devices for HEP when no/limited radiation.
- CPU's/DSP: Mainly for DAQ interfaces
- Mixing FPGA's, DSP, CPU's on one module
  - Can give very high performance and very flexible modules but implies a huge investment in firmware ( FPGA, DSP, CPU, operating system, , ,)
  - FPGAs can now have DSP, CPU on chip.
- Crate based
  - Not (slow) shared parallel bus (e.g. VME)
  - Switch fabric: Multiple high speed serial links on backplane to centralized switch/controller
    (High speed LAN on backplane)
  - Power, cooling, front-panel, standardization but flexible, hot swap, reliable, affordable
  - ATCA, uTCA, VXS (VME with extra serial link connector) are major candidates for HEP
  - **ATCA and uTCA** gets increasing interest by HEP community (uTCA for physics standardization)
  - Trigger systems, DAQ interfaces
- Plugged into computer: PCIe (LHCb upgrade)
  - No expensive crates (e.g. link to front-ends)
  - Challenges:
    - Keeping up with changing PC's
    - Cooling of hot FPGAs and opto



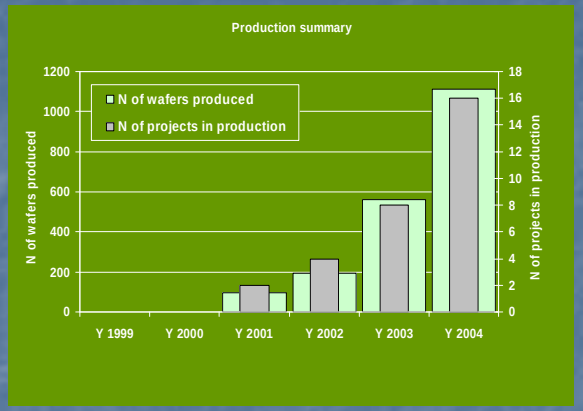
# IC technology for HEP

- Critical to make front-end systems
- What we want:
  - High integration level
    - This exists (e.g. 22nm) but hard for us to access because of problems below
    - The most sophisticated technologies may not even be technically appropriate for us.
  - Appropriate for mixed analog/digital designs
  - Radiation tolerance: >100Mrad
    - Non trivial and requires significant effort to find and qualify technology
    - Special design approaches (and special libraries).
    - Strict export restrictions.
    - Technologies below ~65nm uses "exotic" gate isolation sandwiches where radiation tolerance needs to be qualified/proven
  - Affordable access
    - Sophisticated technologies have very high masks costs but is relatively cheap to produce in very large quantities (exactly the opposite of what we need)
    - We may even not be allowed access, as too small a client.
    - Regular MPW runs vital to share mask costs for prototypes and small scale production
  - Easy to use for relatively small HEP IC design groups
    - Modern technologies and tools get more and more complicated
  - Extensive libraries and IP
    - IP blocks often exists, but may be unusable to us because of radiation (& "too" expensive)
    - Our community has a tendency to make all our selves (limited funding in R&D phase, manpower available, must keep students occupied , ,)
  - Available for long time ( +10years)
    - This may not be the case for certain technology nodes (select strong nodes, bet on the right company)

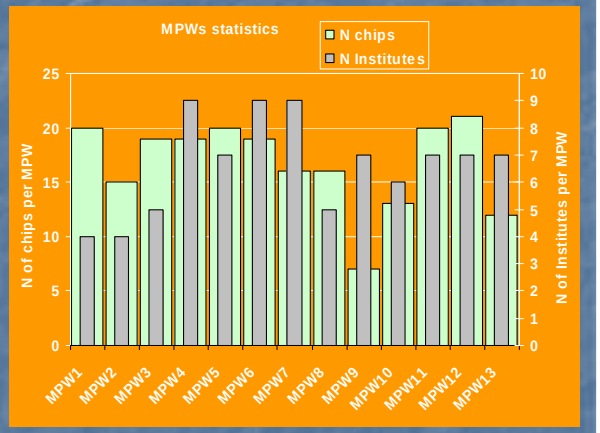
# IC technology

- HEP options
  - Use easily accessible, cheap and mature technologies:
    - Life time, rad tol, Limited integration
  - The community gets together (e.g. via CERN) to use one "modern" technology from a strong technology node, radiation qualify this and get/develop required libraries and tools.
    - LHC: 250nm CMOS
    - LHC phase 1 upgrades: 130nm CMOS
    - LHC Phase 2 upgrades: 65nm CMOS

    Skipping every second node because of long HEP project schedules and limited resources to import/qualify technology.
  - Join with similar communities (e.g. EU Europractice)
  - Specialized technologies:
    - "HV" for DC/DC,
    - Monolithic pixel,
    - HV CMOS sensor
    - CMOS photonics,
- Learning how to use these technologies
  - HEP/CERN community
    - Training sessions in use of technology and related tools
    - Micro Electronics User group
  - Euro-practice training program on tools and technologies



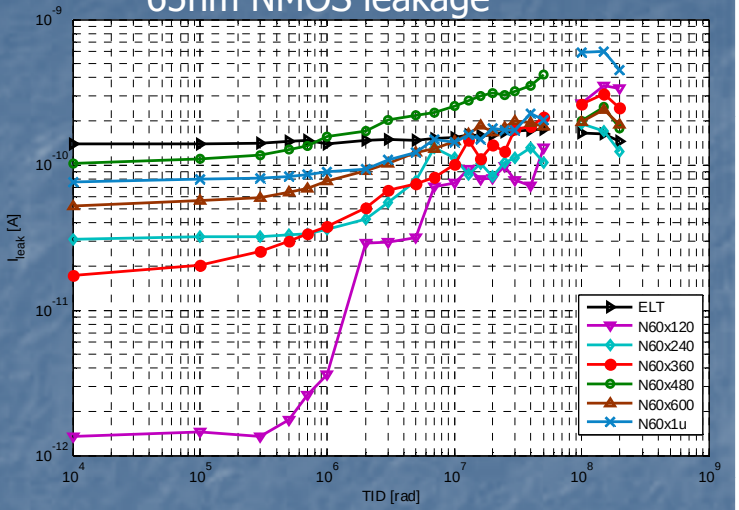

250nm CMOS



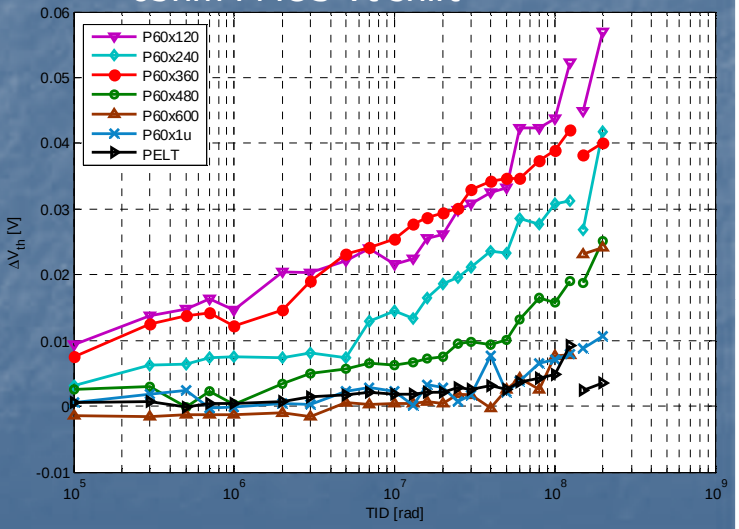
# Next IC technology for HEP

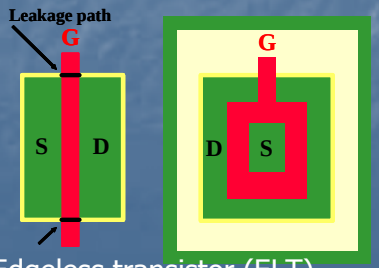
- 65nm seems to be a promising/realistic technology for future long term HEP developments (e.g. LHC phase 2)
  - Well established ~10 year old technology
  - Confirmed to be a strong node
    - Extensively used for many long term components (Industrial, Automotive, Space, etc.)
  - Affordable
    - Small MPW submissions: 50 – 100k CHF
    - Dedicated engineering run: ~2 x 130nm = ~1M CHF
  - Still uses classical "$SiO_2$" as gate insulator
  - Excellent radiation characteristics (up to ~200Mrad)
- Will be available very soon
  - Appropriate Libraries, IPs & tools for HEP institutes
  - NDA issues: >12 months
    (lawyers makes more money than engineers)
- Do we need and can we afford/manage more modern IC technologies ?

65nm NMOS leakage

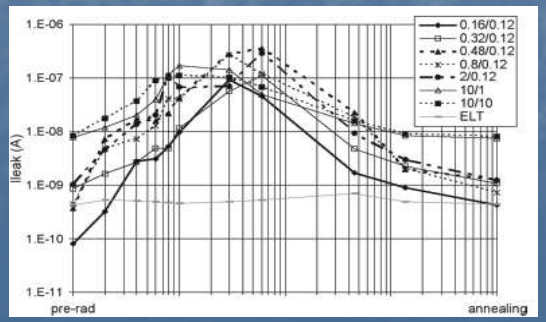



65nm PMOS Vt shift



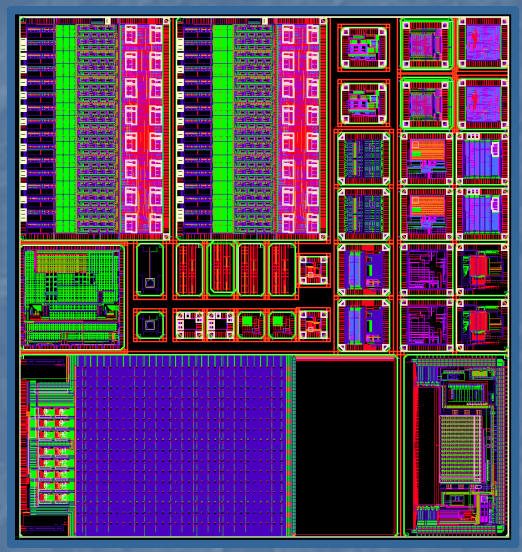

Edgeless transistor (ELT)
Used in 250nm CMOS

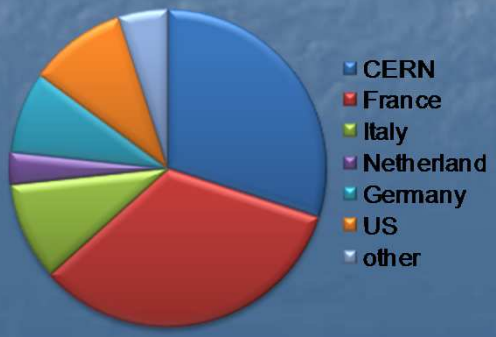


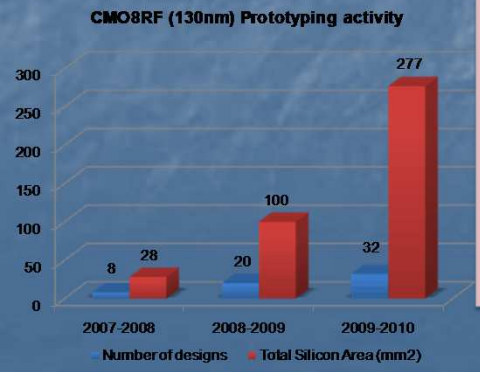

130nm NMOS leakage

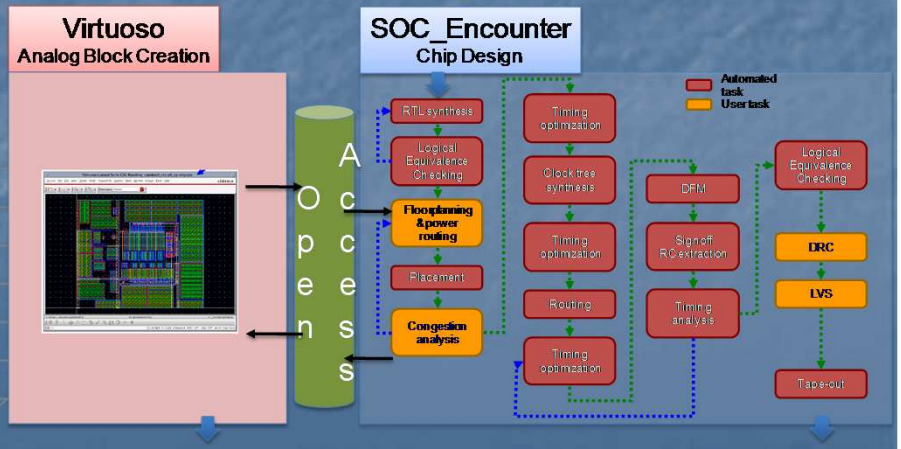
# IC tech from CERN

- 250nm, 130nm, (90nm) and 65nm coming
  - 250nm: workhorse for all rad hard circuits in current LHC experiments
  - 130nm: LHC phase 1 upgrades
  - 65nm: LHC phase 2 upgrades .
- CERN supplies/organizes:
  - Technology selection and rad qualification
  - Frame contract and MPW access
  - Design kit, Libraries
  - HEP users: ~50 world wide institutes
  - 5 day training, 7 courses,  70 Engineers



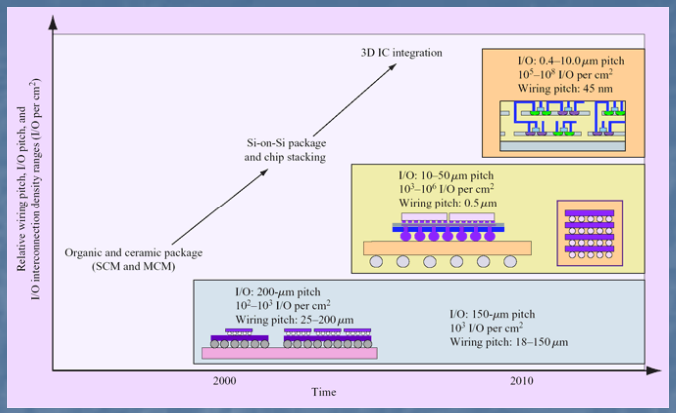


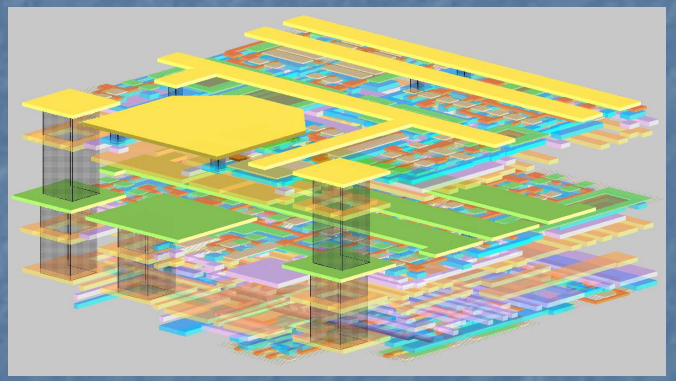



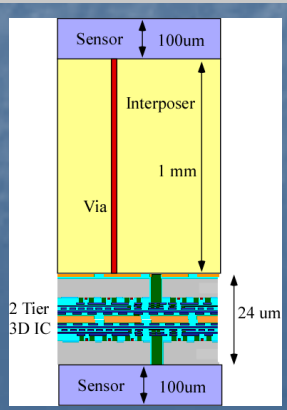
# 3D IC technologies

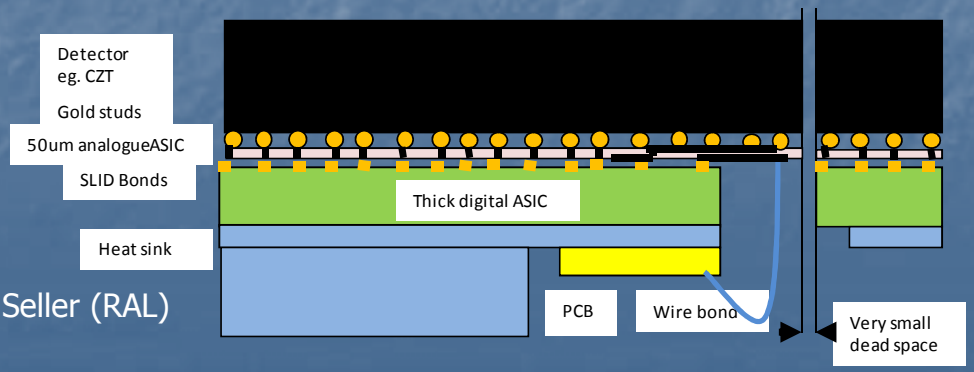
- Dreaming about the perfect 3D IC technology
  - Affordable, Accessible, Reliable, High yield, ,
  - Mixing technologies (Analog, digital, sensor)
- Several HEP institutes teamed together to get access to Chartered/Tezzaron process
  - Chips have been in the pipeline for several years
  - Low yield
  - TSV Technology have now been modified
  - We may still need to wait for this to mature
- Will 3D IC become available (to us) ?
  - Before IC technology hits a technology wall (10nm ?)
    - Why use 3D in 130nm when one can "easily" migrate to 65nm ?
    - Yield is a major problem
  - One obvious candidate: Stacking of memory chips
    - This is more 3D packaging as only coarse TSVs needed at boundary
    - Memory chips have redundancies



Fermilab

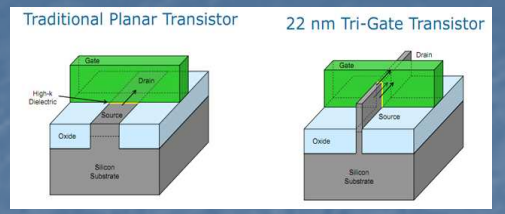


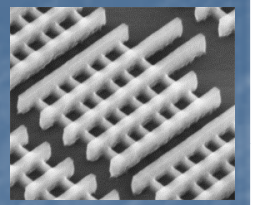



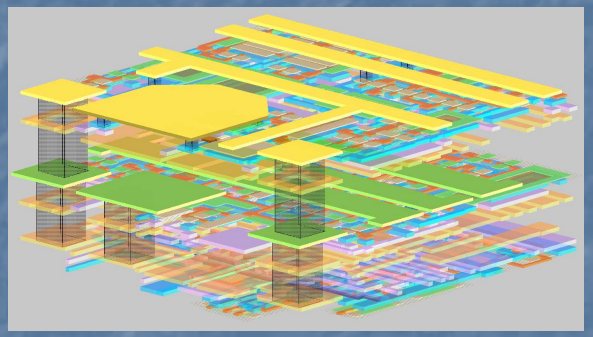

Paul Seller (RAL)

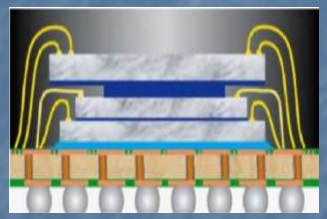
# 3D technologies

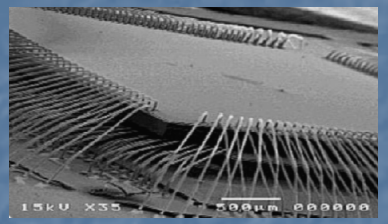
- 3D is fashion, but be careful with confusion between different 3D's
  - 3D transistors (Intel <22nm technology)
    - To be capable of continuing Moore's law without excessive transistor leakage.
      - Controls current flow from ¾ sides of transistor
      - 37% speed improvement from previous technology (32nm) or half power at same speed
      - Expected to scale down to <10nm
    - We can not (yet) get access or afford this
    - Alternative: Fully depleted SOI (Silicon On Insulator)
  - 3D IC's
    - Multiple active layers connected with (small) TSV
  - 3D packaging/integration
    - Stacking chips on top of each other using:
      - Wire bonding
      - Bump bonding
      - TSV + bump bonding
  - 3D detectors

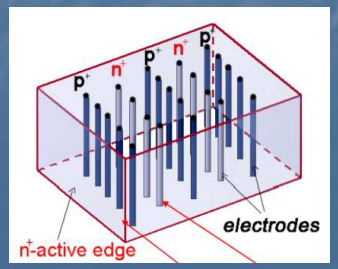


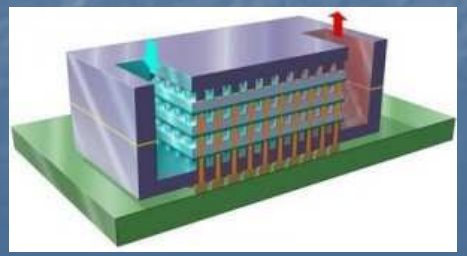





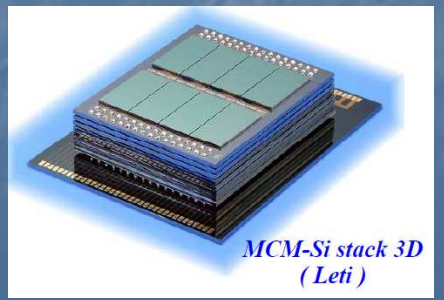






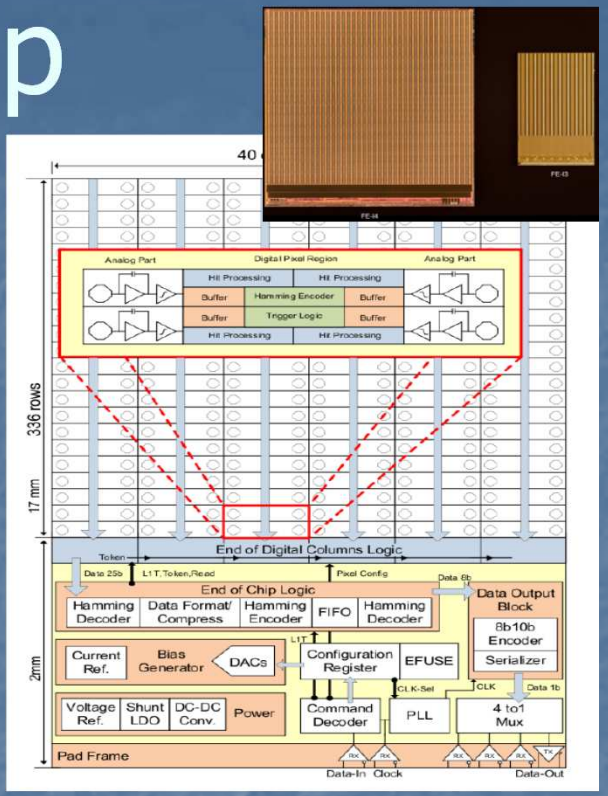



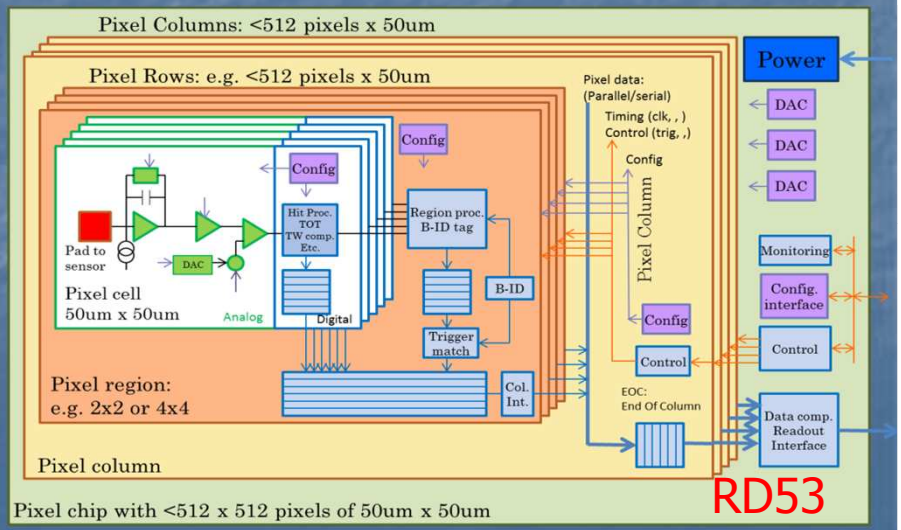
Combined with micro channel cooling
Dream ?.



# System on chip

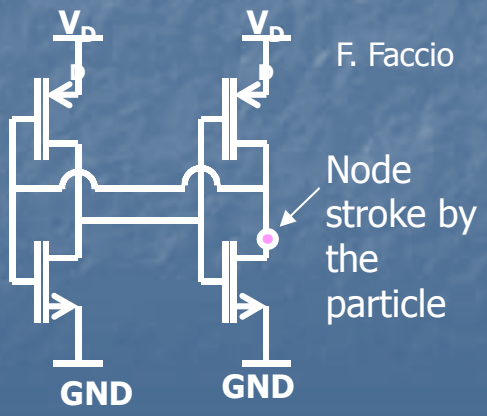
- Large design effort required to design complicated system on chip implementations
  - Large and well integrated design team
    - Intel makes the office floor plan equal to the chip floor plan
  - Significant design time
  - Significant funding
  - Any small mistake makes the design fail
  - Efficient use of modern high level (digital) and low level (analog full custom) design tools
    - These tools are complicated
- Example: FEI4 collaborative effort
  - Large mixed signal pixel chip (19 x 20 mm)
  - Developed in collaboration across multiple institutes (~5) spread across the world
  - Used dedicated tools to monitor/control status and changes of each block
  - Handling radiation effects and SEU.
  - Successfully used for ATLAS IBL upgrade
- Things will get more complicated for future complex chips in 65nm:
  "Full DAQ system" on a single chip
  - RD53 ATLAS/CMS/LCD pixel collaboration

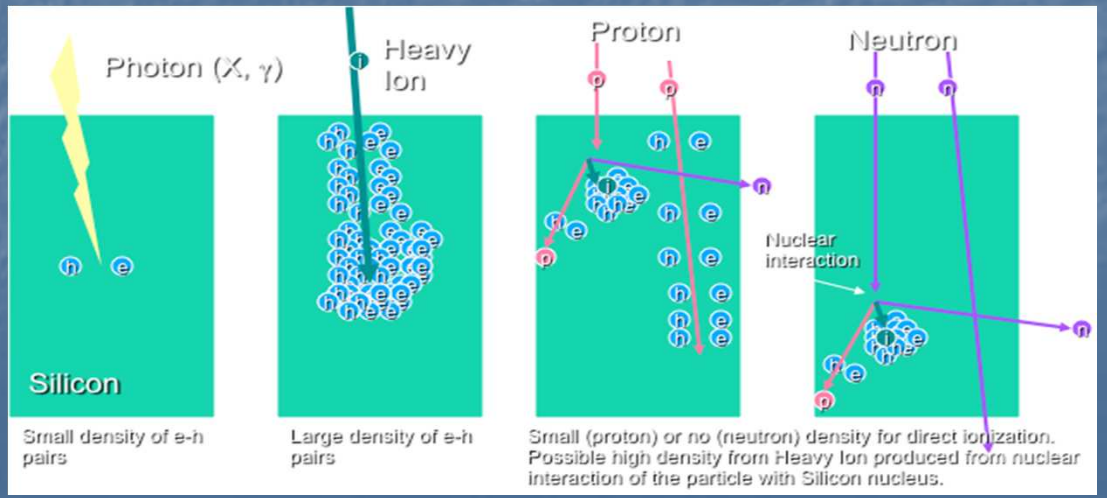


# SEU

- Radiation induced SEU's is a major worry in our front-end chips
  - New technologies get more sensitive (and we get multi bit errors)
- Different types of data must be protected differently:
  - Hit data (loss of single hit, or noise hit)
  - Data flow control (system synchronization)
  - Configuration (chip malfunction until reconfigured)
  - PLL, etc.
- Appropriate design methodologies required (TMR, Hamming)
- Design, test, fault injection, design verification, production testing, etc.
- SEU's provoked by background radiation now becomes "visible" in high complexity high availability commercial applications
  - Cosmic's, Radioactive isotopes (e.g. from materials used in electronics packaging)
  - Automotive, Telecom and network infrastructure, Computer servers (e.g. centralized banking/ reservation systems)
  - They also start to apply special techniques to resolve this and some tools start to appear.



# COTS

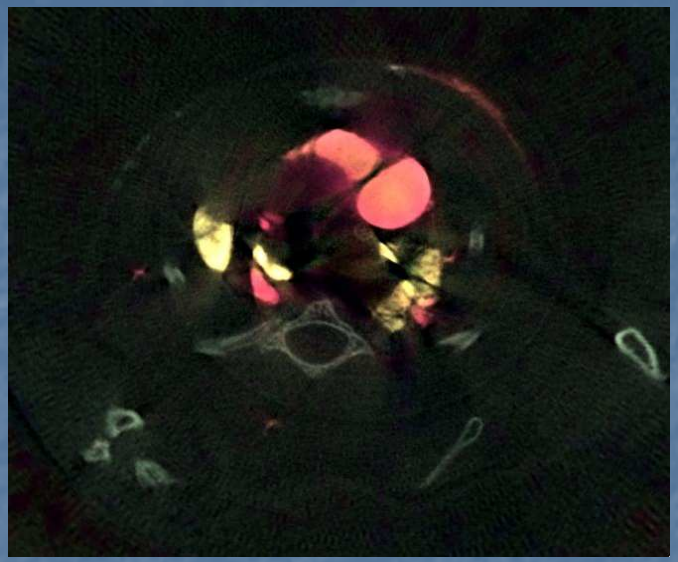
- Use COTS (Commercial Of The shelves) where ever possible (when no radiation !)
- In radiation environments
  - Radiation qualification (TID, SEL, SEU) of a component is a significant workload
    - Predictions from similar circuits can be misleading
  - Difficult to assure that circuits purchased later will have same radiation tolerance (change of process, different fab. , second sourcing, etc.)
  - Mill/Space qualified components will often be hard to get or too expensive (hermetic packaging and qualification)
  - FPGA's: Many HEP applications would like to use FPGA's in moderate radiation environments
    - Modern FPGA can work in modest radiation (TID: 10k – 100krad)
    - Single event latchup has been seen to be OK in several modern FPGA families
    - Single events upsets is the major worry for reliable functioning
      - Antifuse: Normal SEU protection schemes (TMR, Hamming coding, etc.) can be used (can not be reprogrammed)
      - Flash: Normal SEU schemes can be used (do not reprogram when radiation is present)
      - SRAM: SEU is a major issue but tools improving on this exists. Partial reprogramming
    - Special space qualified FPGA's exist but are very expensive and have strict export restrictions

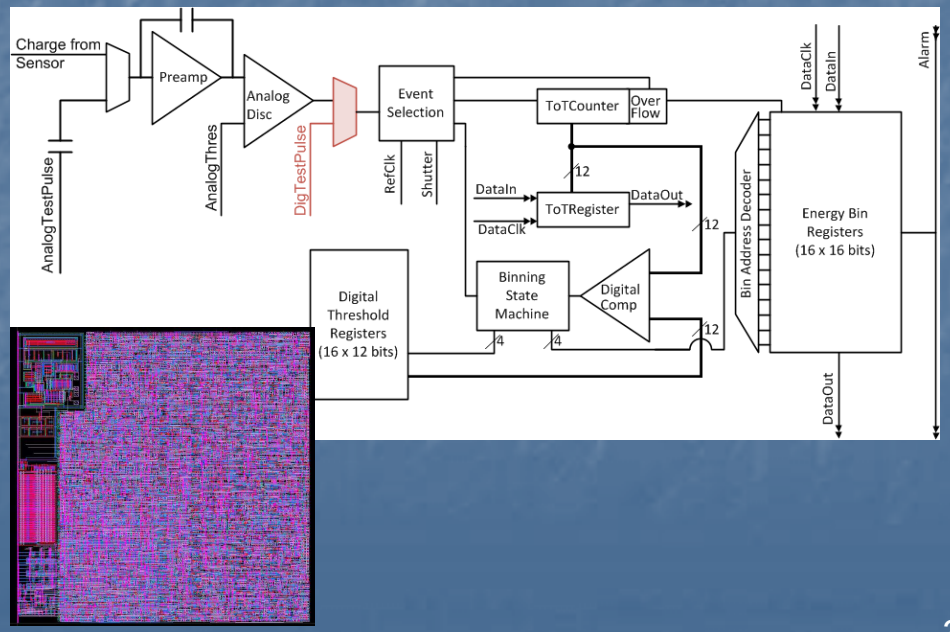
# Synergy

- HEP electronics/detectors can/could have good synergy with several domains
  - Medical: Scanners, Xray
  - Material science: Synchrotron Xray detectors
  - Home security: Scanners, detectors
  - Space: rad tolerant electronics
  - [Military]

# Pixel detector spin off

- High resolution X-ray imaging with spectrum information
- Portable dosimeter
- In Schools !





# Summary

- Ever increasing integration of detector and its electronics
  - **Pixels**, strips, calorimeter, muon, ,
- Use of modern IC, interconnect, opto and power conversion technologies vital to built significantly improved HEP experiments.
- Modern technologies are expensive to get access to and design with but offers unique opportunities and allows cheap large scale production.
- Our community must profit from available technologies the best possible:
  - Use common/shared technologies when possible
  - Exchange of experience across groups: TWEPP, FEE, NSS, MUX
  - We can "never" afford using the latest IC technologies
    - Only when using commercial IC's but they do "not like" our radiation environment
  - Buy IP blocks from industry when possible
- Assure sufficient electronics engineering expertise in HEP is vital.
- Building complex electronics systems across so many groups requires efficient use of modern simulation and verification tools at all levels ( system, sub-system, links, module, ASIC, analog front-end ) and efficient communication and coordination.
- Certain basic technologies/functions are needed by all HEP experiments/sub-detectors and are better made as common efforts
  - IC technology qualification, libraries, IP's, Tools
  - Radiation hard optical links
  - Radiation hard and magnetic field tolerant Power conversion
  - Other ?

If you want to know more on electronics for HEP then come to TWEPP 2014

# Backup

# RD53 Organisation issues

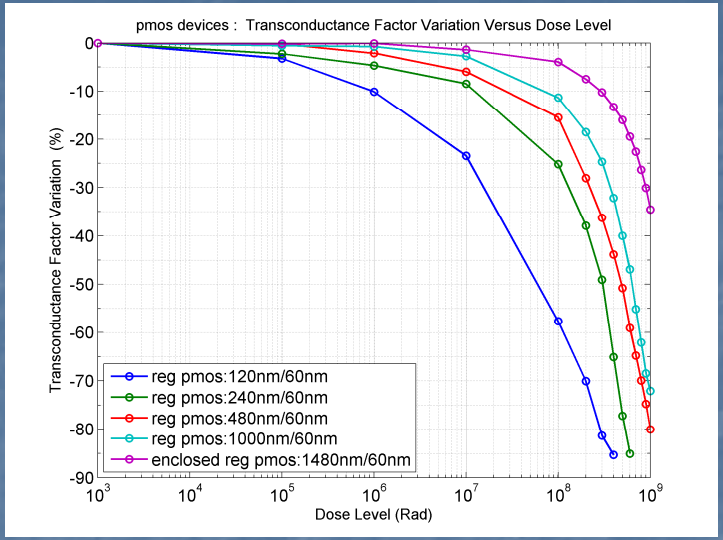
- 19 Institutes (2 new institutes have joined)
  - Bari, Bergamo-Pavia, Bonn, CERN, CPPM, Fermilab, LBNL, LPNHE Paris, **Milano**, NIKHEF, New Mexico, Padova, Perugia, Pisa, **Prague IP/FNSPE-CTU**, PSI, RAL, Torino, UC Santa Cruz.
  - ~100 collaborators
  - 2 institutes requesting to join: LAL/OMEGA, Seville
- Spokes persons: Maurice Garcia-Sciveres, LBNL (ATLAS), Jorgen Christiansen, CERN (CMS)
  - 2 year terms
- Institute Board
  - IB chair: Lino Demaria, Torino
  - Regular IB meetings
  - MOU drafted and ready to be signed
- Management board: Spokes persons, IB chair, WG conveners
  - Monthly meetings
- Mailing lists, INDICO, CDS, TWIKI: http://twiki.cern.ch/RD53 , etc. set up
- Technical Working Groups have started
  - WG conveners
  - Regular WG meetings
- First official RD53 collaboration meeting (pre-RD53 meeting in Nov. 2012)
  - CERN April 10-11, 64 participants: https://indico.cern.ch/event/296570

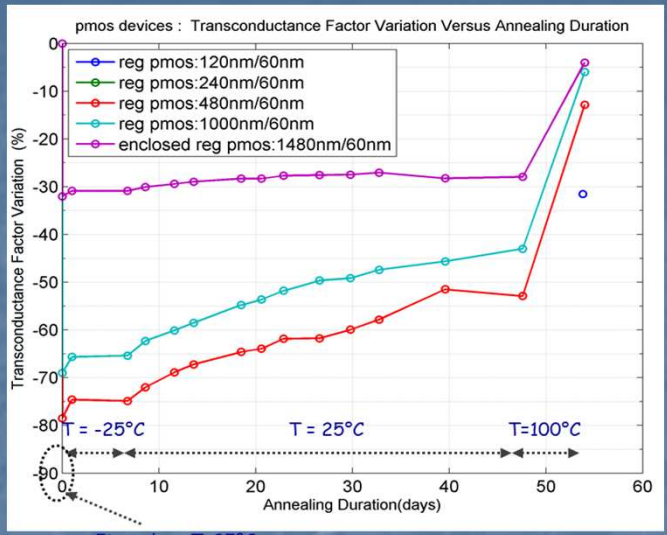
# Radiation WG

- Radiation test and qualification of baseline 65nm technology for radiation levels of 1Grad and $10^{16}$ neu/cm$^2$
- WG convener: Marlon Barbero, CPPM
- Activities and Status:
  - Defining radiation testing procedure
  - Test of 65nm transistors to 1Grad
    - NMOS: Acceptable degradation
    - PMOS: Severe radiation damage above 300Mrad (next slide)
      - Not yet a clear understanding of effects seen at these unprecedented radiation levels
      - ESD damage from manipulation and test systems ?
    - Systematic radiation/annealing studies required to be verified with pixel detector operation
  - Test of circuits to 1Grad
    - Ring oscillators, Pixel chips ( CERN, LBNL)
    - Some digital circuits remains operational up to 1Grad, depending on digital library used. (better than indicated by tests of individual transistors)

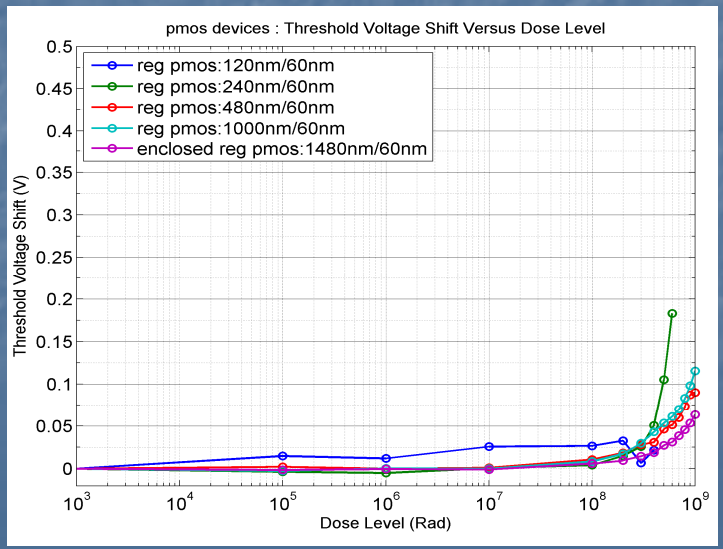
  **Critical to confirm if 65nm is OK for inner layers of pixel detectors**
    - Alternative foundries/technologies or replacement of inner layers after a few years ?
- Plans
  - Systematic radiation and annealing studies of 65nm basic devices and circuits
  - Hadron/neutron radiation tests for NIEL effects
  - Radiation test of basic transistors/structures in alternative technologies (for comparison/understanding)
  - Simulation models of radiation degraded transistors (if possible)
- CERN, CPPM, Fermilab, LBNL, New mexico, Padova

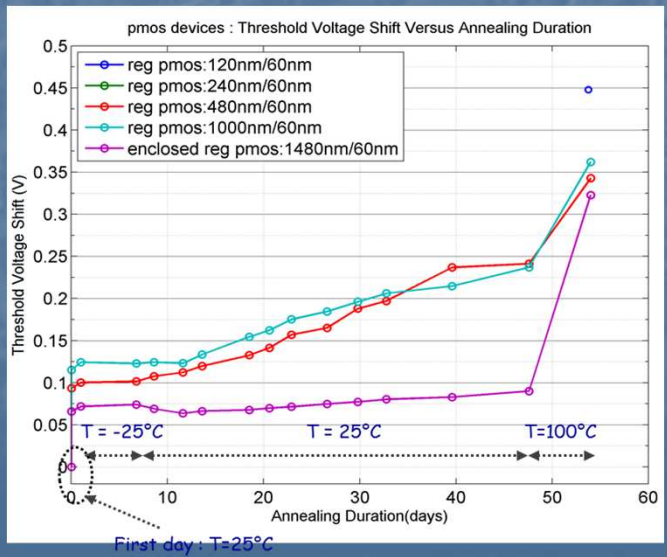
# PMOS Radiation effects 65nm



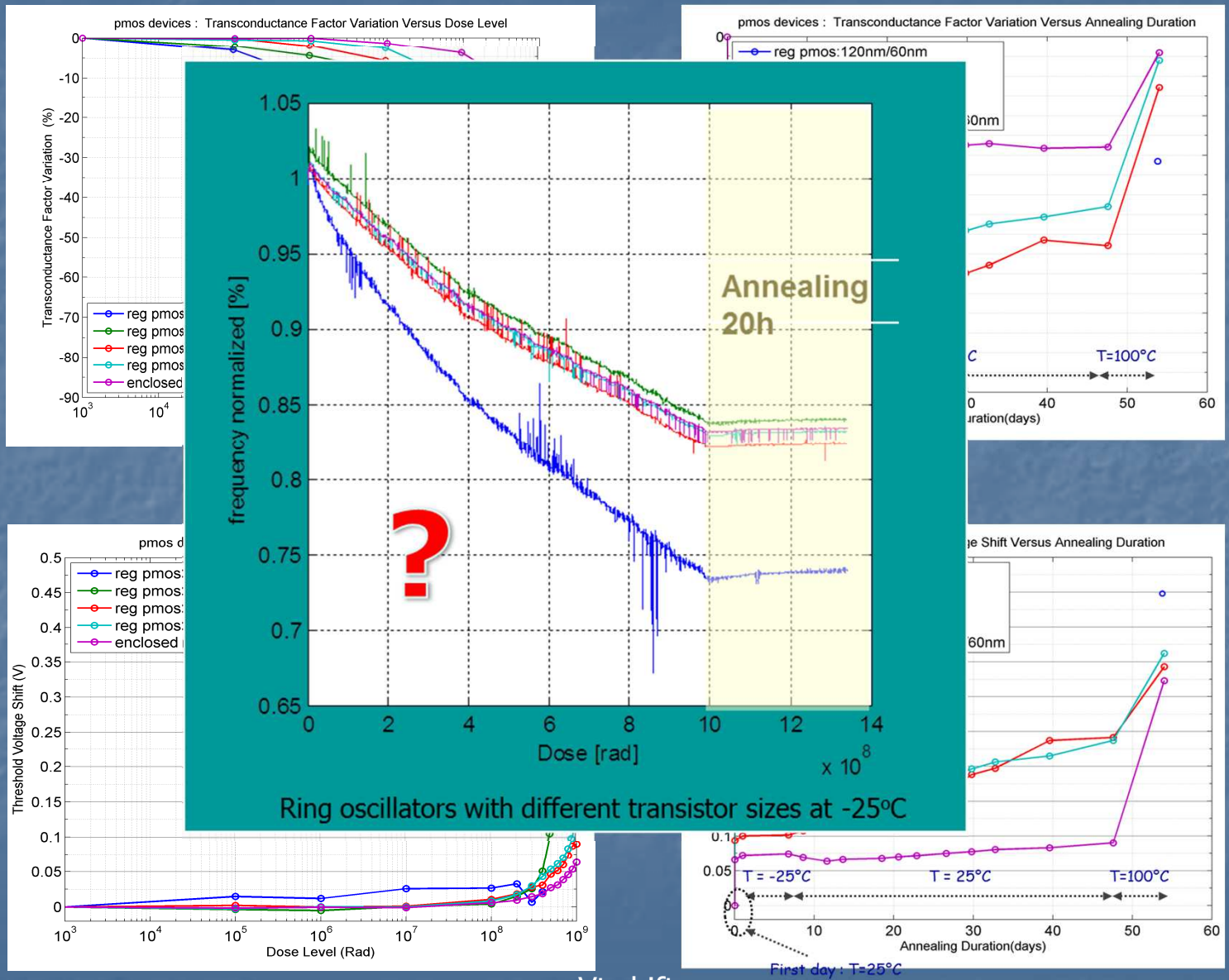

Transconductance



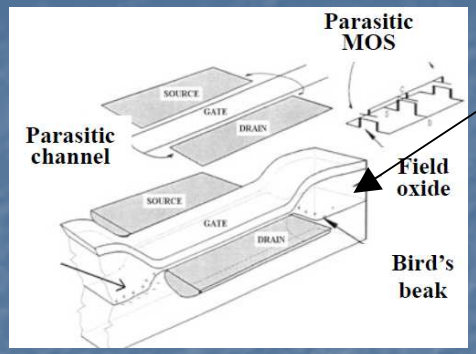

Vt shift

# PMOS Radiation effects 65nm



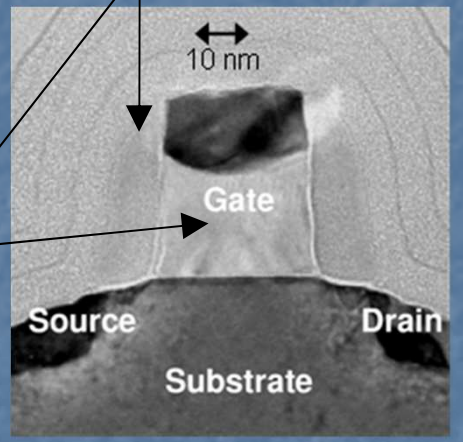

Vt shift

# Radiation effects




Birds beak parasitic device

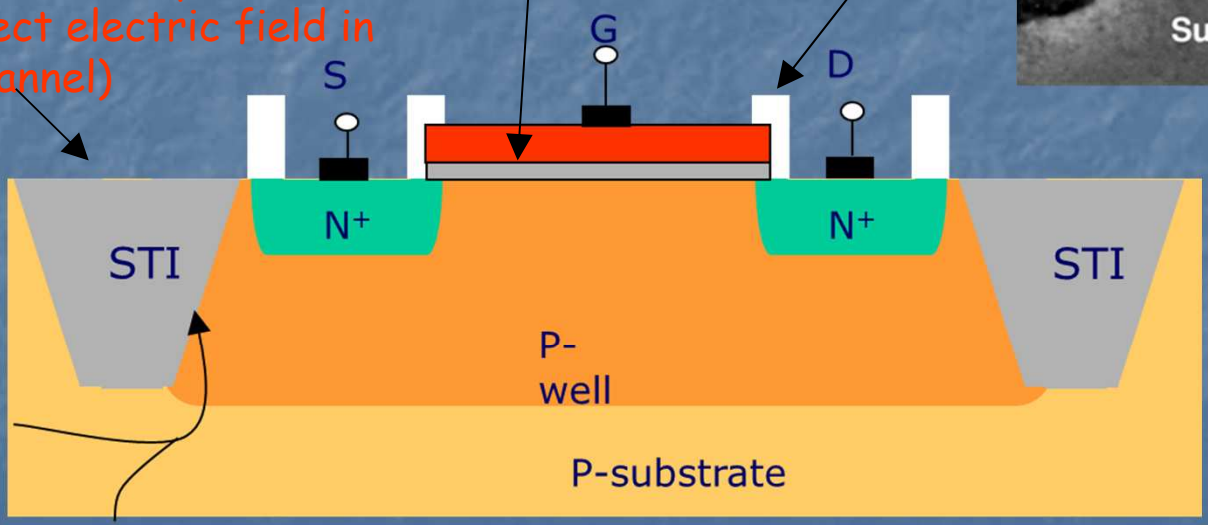
Spacer dielectrics may be radiation-sensitive




Charge buildup in gate oxide and interface states affects Vt

Thick Shallow Trench Isolation Oxide (~ 300 nm); radiation-induced charge-buildup may turn on lateral parasitic transistors and affect electric field in the channel)

Doping profile along STI sidewall is critical; doping increases with CMOS scaling, decreases in I/O devices

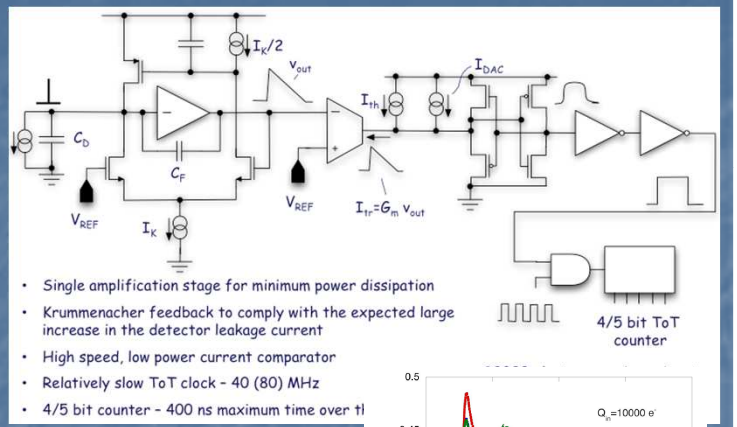


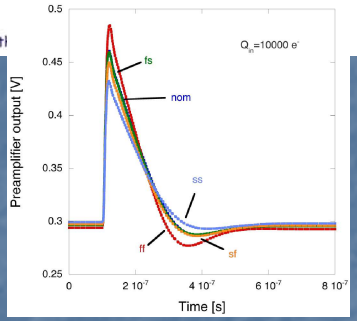

Increasing sidewall doping makes a device less sensitive to radiation (more difficult to form parasitic leakage paths)

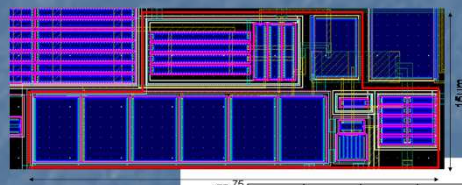
# Analog WG

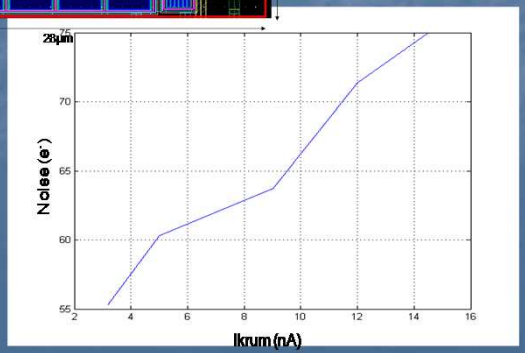
- Evaluation, design and test of appropriate low power analog pixel Front-Ends
- Convener: Valerio Re, Bergamo/Pavia
- Activities and status
  - Analog front-end specifications
    - Planar, 3D sensors, capacitance, threshold, charge resolution, noise, deadtime, ,
  - Alternative architectures –implementations to be compared, designed and tested by different groups
    - TOT, ADC, Synchronous, Asynchronous, Threshold adjust, Auto zeroing, etc.
  - Design / prototyping of FE's ongoing
- Plans
  - Prototyping and test (with radiation) different FEs
    - Some FEs have already been prototyped
    - Others will be prototyped after the summer
  - Test, comparison and choice of most appropriate FE(s)
- Bergamo-Pavia, Bonn, CERN, CPPM, Fermilab, LBNL, Prague IP/FNSPE-CTU, Torino.

Krummenacher – TOT examples



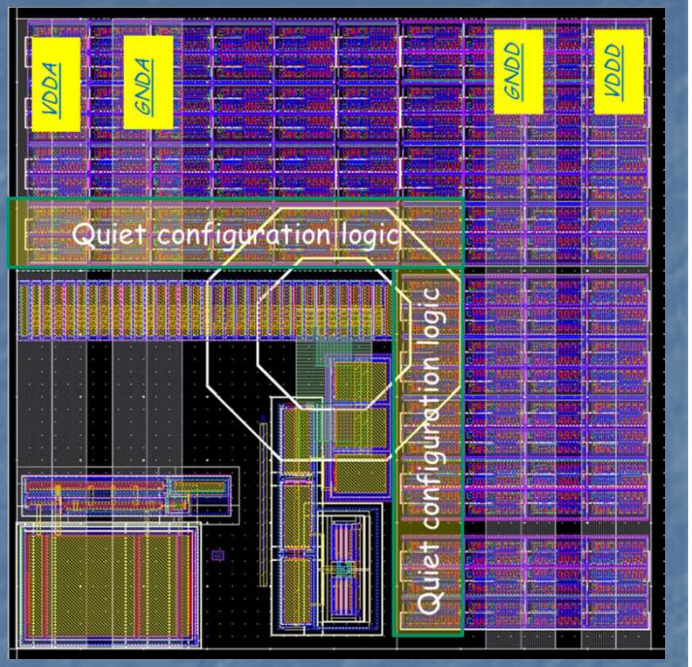



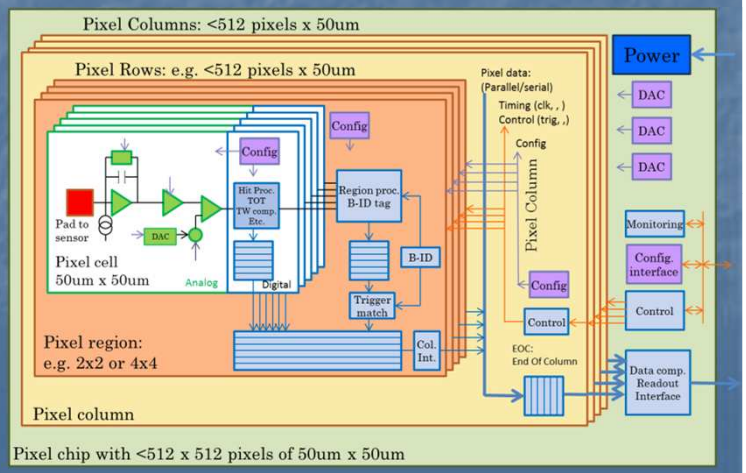



# Top level WG

- Global architecture and floor-plan issues for large mixed signal pixel chip
- Convener: Maurice Garcia-Sciveres, LBNL
- Activities and status
  - Global floorplan issues for pixel matrix
    - 50x50um$^2$ – 25x100um$^2$ pixels with same pixel chip
      - ATLAS – CMS has agreed to initially aim for this
    - Global floor-plan with analog and digital regions
  - Appropriate design flow
  - Column bus versus serial links
  - Simplified matrix structure for initial pixel array test chips
- Plans
  - Submission of common simplified pixel matrix test chips
  - Evaluation of different pixel chip (digital) architectures
    - Using simulation frameworks from simulation WG.
  - Final integration of full pixel chip
- Bonn, LBNL, , , ,



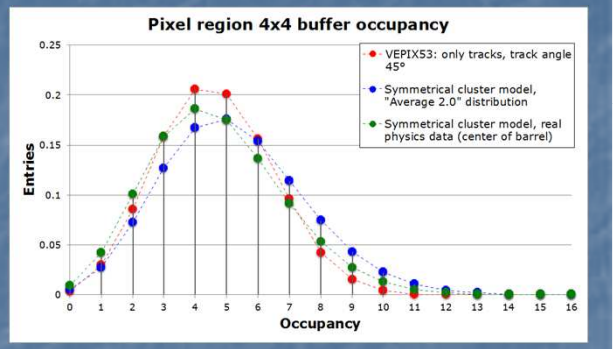
# IP WG

- Make IP blocks required to build pixel chips
- Convener: Jorgen Christiansen, CERN
- Activities and status
  - List of required IPs (30) defined and assigned to groups
    - Review of IP specs June 2014
  - Defining how to make IPs appropriate for integration into mixed signal design flow for full/final pixel chips
    - IP expert panel
    - CERN design flow
  - Design of IP blocks have started
- Plans
  - Common IP/design repository
  - Prototyping/test of IP blocks 2014/2015
  - IP blocks ready 2015/2016
- ~All RD53 institutes

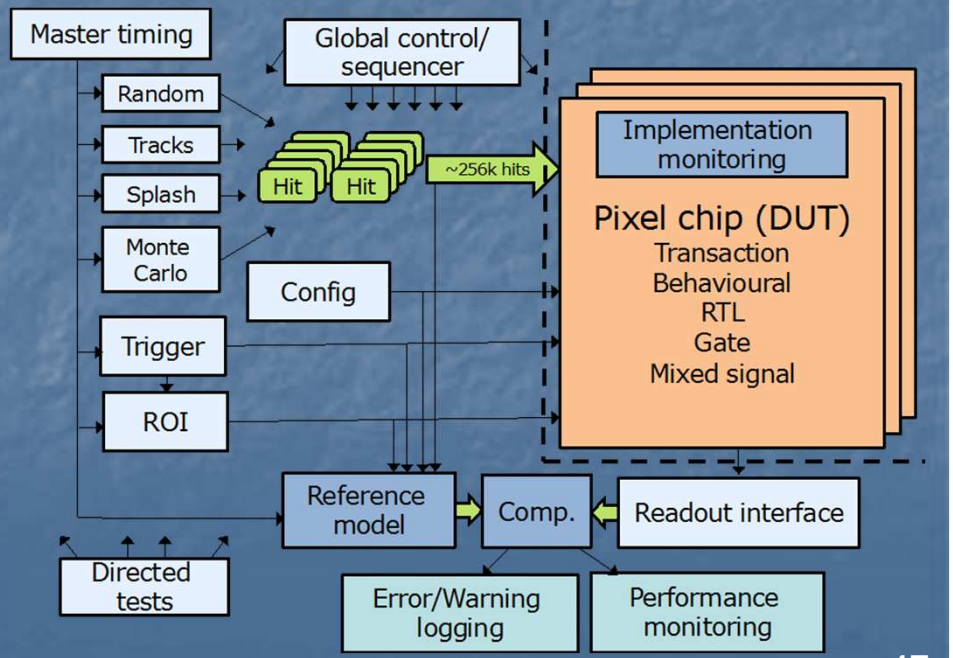
| Country | DE | | FR | NL | IT - INFN | | | | US | FR | UK | US | CZ | Comments |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Group | Bonn | CERN | CPPM | NIKHEF | Bari Pavia Torino (Milano) | Padova | Pisa | Torino | LBNL | LPNHE | RAL Santa Cruz | | (Prague) | |
| ANALOG: Coordination with analog WG | | | | | | | | | | | | | | |
| Temperature sensor. | | | O | | (P) | | | (P) | | | | | (P) | |
| Radiation sensor | | | (P) | | (P) | | | O ? | | | | | (P) | |
| HV leakage current sensor. | | | O | | | | | (P) | | | | | (P) | |
| Band gap reference | | O | O | (P) | O | | | | | | (P) | | | 3 Groups |
| Self-biased Rail to Rail analog buffer | (P) | | (P) | (P) | | | | | | | O | | (P) | |
| MIXED | | | | | | | | | | | | | | |
| 8 – 12 bit biasing DAC | | (P) | | O | | | | | | | | | (P) | |
| 10 - 12 bit slow ADC for monitoring | | O | O | O | | | | | | | | | | 3 Groups |
| PLL for clock multiplication | O | (P) | | (P) | | (P) | (P) | (P) | | | (P) | (P) | | Together |
| High speed serializer ( ~Gbit/s) | O | (P) | | (P) | | | (P) | | | | (P) | (P) | | |
| (Voltage controlled Oscillator) | | | | (P) | | O | (P) | (P) | | | | | | Needed ? |
| Clock recovery and jiter filter | O | (P) | | | | | (P) | | | | (P) | | | |
| Programmable delay | O | (P) | | | | | (P) | | | | (P) | | | |
| DIGITAL | | | | | | | | | | | | | | |
| SRAM for pixel region | (P) | (P) | | | O | | | | | | | (P) | | |
| SRAM/FIFO for EOC. | (P) | (P) | | | (P) | | (P) | | | | | O | | |
| EPROM/EFUSE | (P) | O | (P) | | | | | | | | | | | |
| DICE storage cell / config reg | (P) | | O | | | (P) | | (P) | | | | | (P) | Or TMR ? |
| LP Clock driver/receiver | (P) | | | | O | | | | | | (P) | | | |
| (Dedicated rad hard digital library) | (P) | (P) | (P) | | | | O | | | (P) | (P) | | | If needed |
| (compact mini digital library for pixels) | (P) | (P) | (P) | | | | O | | | (P) | (P) | | | If needed |
| IO: Coordination with IO WG | | | | | | | | | | | | | | |
| Basic IO cells for radiation | (P) | O | | | | | | | | | | | | |
| Low speed SLVS driver (<100MHz) | (P) | (P) | | | O | | (P) | (P) | | | | | (P) | |
| High speed SLVS driver (~1Gbits/s) | (P) | (P) | | | O | | (P) | (P) | | | | | (P) | Together |
| SLVS receiver | (P) | (P) | | | O | | (P) | | | | | | (P) | |
| 1Gbits/s drv/rec cable equalizer | | | | | | | | | | | | | | New |
| C4 and wire bond pads | (P) | O | | | | | | | | | | | | |
| (IO pad for TSV) | O | | (P) | | | | | | | (P) | | (P) | | |
| Analog Rail to Rail output buffer | O | | (P) | | | | | | | (P) | | (P) | | |
| Analog input pad | O | | | | | | | | | (P) | | | | |
| POWER | | | | | | | | | | | | | | |
| LDO(s) | | (P) | (P) | O | | | (P) | (P) | | | (P) | | | |
| Switched capacitor DC/DC | | (P) | | | | | | | O | | | | (P) | |
| Shunt regulator for serial powering | | | O | | | | | | | | | | | |
| Power-on reset | | | | | | | | | | | | | | New |
| Power pads with appropriate ESD | (P) | O | | | | | | | | | | | | |
| SOFT IP: Coordination with IO WG | | | | | | | | | | | | | | |
| Control and command interface | | (P) | | (P) | | | O | | | (P) | | | | |
| Readout interface (E-link ?) | | (P) | | (P) | | | O | | | (P) | | | | |
| Summary | | | | | | | | | | | | | | |
| ATLAS/CMS/Neutral | A | N | A | A | C | C | C | C | C | A | A | N | A | A | ATLAS | CMS | Neutral |
| O's | | 7 | 6 | 5 | 2 | 2 | 5 | 1 | 1 | 4 | 1 | 1 | | 1 | 1 | | 16 | | 14 | 7 |
| (P)'s | | 14 | 16 | 8 | 5 | 2 | 2 | 2 | 1 | 10 | 7 | | 7 | 9 | 6 | 9 | 49 | | 24 | 25 |

# Simulation/verification WG

- Simulation and verification framework for complex pixel chips
- Convener: Tomasz Hemperek, Bonn
- Activities and status
  - Simulation framework based on system Verilog and UVM (industry standard for ASIC design and verification)
    - High abstraction level down to detailed gate/transistor level
    - Benchmarked using FEI4 design
  - First basic version of framework available on common repository
    - Internal generation of appropriate hit patterns
    - Used for initial study of buffering architectures in pixel array
  - Integration with ROOT to import hits from detector simulations and for monitoring and analysing results.
- Plans
  - Refine/finalize framework with detailed reference model of pixel chip
  - Import pixel hit patterns from detector Monte-Carlo simulation
  - Modelling of different pixel chip architectures and optimization
  - Verification of final pixel chip
- Bonn, CERN, Perugia




Buffer occupancy comparison between simulation and analytical statistical model



# RD53 Outlook

- 2014:
  - Release of CERN 65nm design kit. RD53 eagerly awaiting NDA issues to be resolved.
  - **Detailed understanding of radiation effects in 65nm**
    - Radiation test of few alternative technologies.
    - Spice models of transistors after radiation/annealing
  - **IP/FE block responsibilities defined** and appearance of first FE and IP designs/prototypes
  - Simulation framework with realistic hit generation and auto-verification.
  - Alternative architectures defined and efforts to simulate and compare these defined
  - **Common MPW submission 1**: First versions of IP blocks and analog FEs
- 2015:
  - Common MPW submission 2: Near final versions of IP blocks and FEs.
  - Final versions of IP blocks and FEs: Tested prototypes, documentation, simulation, etc.
  - IO interface of pixel chip defined in detail
  - **Global architecture defined and extensively simulated**
  - **Common MPW submission 3: Final IPs and FEs, Initial pixel array(s)**
- 2016:
  - **Common engineering run: Full sized pixel array chip**.
  - Pixel chip tests, radiation tests, beam tests , ,
- 2017:
  - Separate or common ATLAS – CMS final pixel chip submissions.

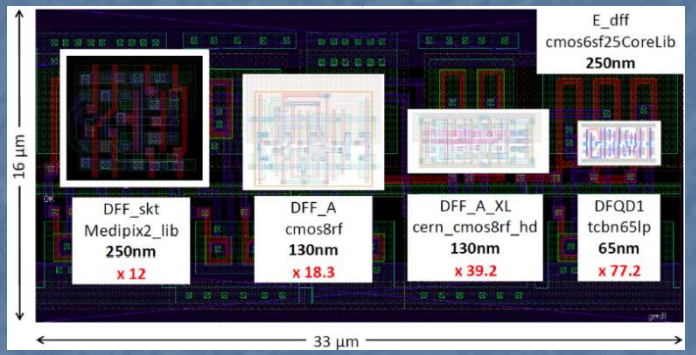
# RD53 Summary

- RD53 has gotten a good start
  - Organization structure put in place
  - Technical work in WGs have started

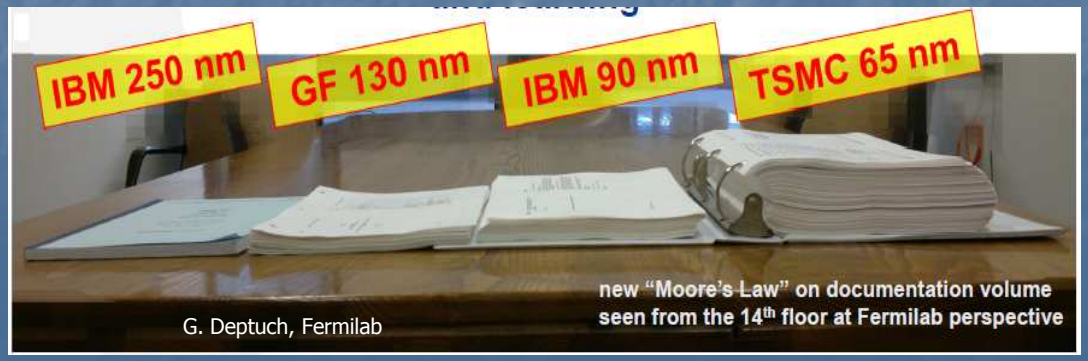
  The development of such challenging pixel chips across a large community requires a significant organisation effort.
- Radiation tolerance of 65nm remains critical
  - Design work has started in 65nm (FEs, IPs)
  - Annealing effects/scenario to be understood
  - Backup: Inner layer replacement versus alternative technology
- RD53 is now a recognized collaboration requested to report in relevant HEP/pixel meetings, conferences and workshops:
  - ATLAS/CMS meetings
  - ACES2014: https://aces.web.cern.ch/aces/aces2014/ACES2014.htm
  - Front-end electronics workshop: http://indico.cern.ch/event/276611/overview
  - Pixel/Vertex
- Funding for RD53 work starts to materialize in institutes
- CMS and ATLAS rely fully on RD53 for their pixel upgrades

# Why 65nm Technology

- Mature technology:
  - Available since ~2007
- High density and low power
- Long term availability
  - Strong technology node used extensively for industrial/automotive
- Access
  - CERN frame-contract with TSMC and IMEC
    - Design tool set
    - Shared MPW runs
    - Libraries
    - Design exchange within HEP community
- Affordable (MPW from foundry and Europractice, ~1M NRE for full final chips)
- Significantly increased density, speed, , , and complexity !

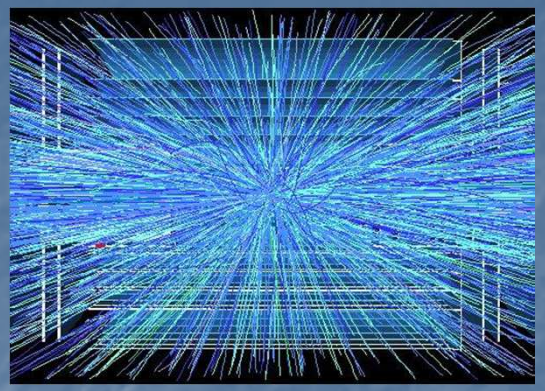



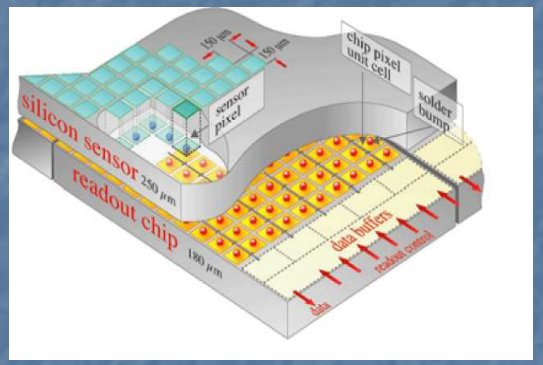

X. Llopart CERN

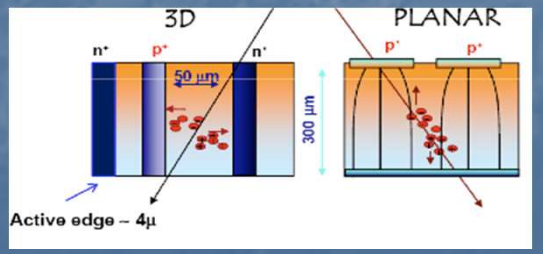


# CMS Phase 2 pixel challenges

- Very high particle rates: ~500MHz/cm$^2$ (inner layer)
  - Hit rates: ~2 GHz/cm$^2$ (factor ~16 higher than current detectors)
  - Assuming max 140 (200) pileup and 25ns crossings
- Smaller pixels: ~¼ (~50x50um$^2$ or 25x100um$^2$)
  - Increased resolution
  - Improved two track separation (jets)
  - Outer layers with larger pixels, using same pixel chip
    - Lower power – low material, lower cost
- Participation in first/second level trigger ? (NO)
- Increased readout rates: 100kHz -> 500KHz - 1MHz
  - Data rate: 10x trigger X >10x hit rate **= >100x !**
- Unprecedented hostile radiation: ~1Grad, ~10$^{16}$ Neu/cm$^2$
  - Hybrid pixel detector with separate readout chip and sensor.
    - Monolithic seems unfeasible for this very high rate hostile radiation environment
  - Phase2 pixel will get in 1 year what we now get in 10 years
- Low mass -> Low power, Critical and very challenging
- Pixel sensor(s) not yet determined
  - Planar, 3D, (Diamond, HV CMOS)
  - Possibility of using different sensors in different layers/locations
  - Do we need/want charge information ? (assume yes for track interpolation)
  - Final sensor decision may come relatively late.
- Complex, high rate and radiation hard pixel chip required and critical -> RD53

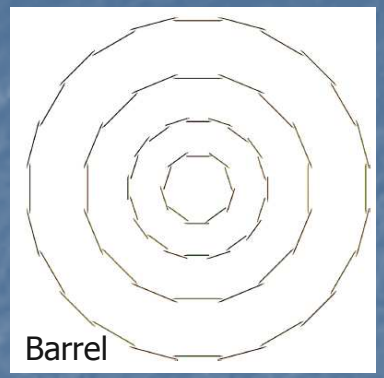


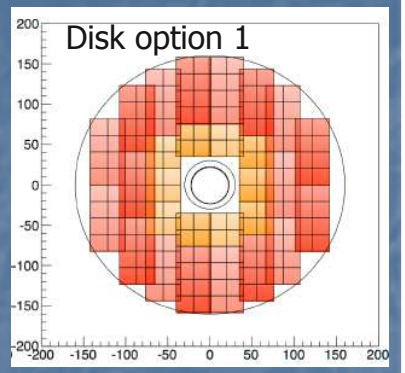


# Layout

- Based on phase 1 layout with additional forward disks (2 x 10)
- Detailed detector/physics simulation for phase 2 detector not yet available
- First iterations on-going:
  - Fit layout constraints
  - Estimate vertex/impact-parameter resolution
  - Minimize number of different module types
  - Minimize overlap
  - Replace inner part if needed
  - Cooling
  - Size of pixel modules: 4x1, 4x2, (2x2)
  - Size of pixel chip: e.g. 23 x 21+2 mm$^2$
  - Electronics services

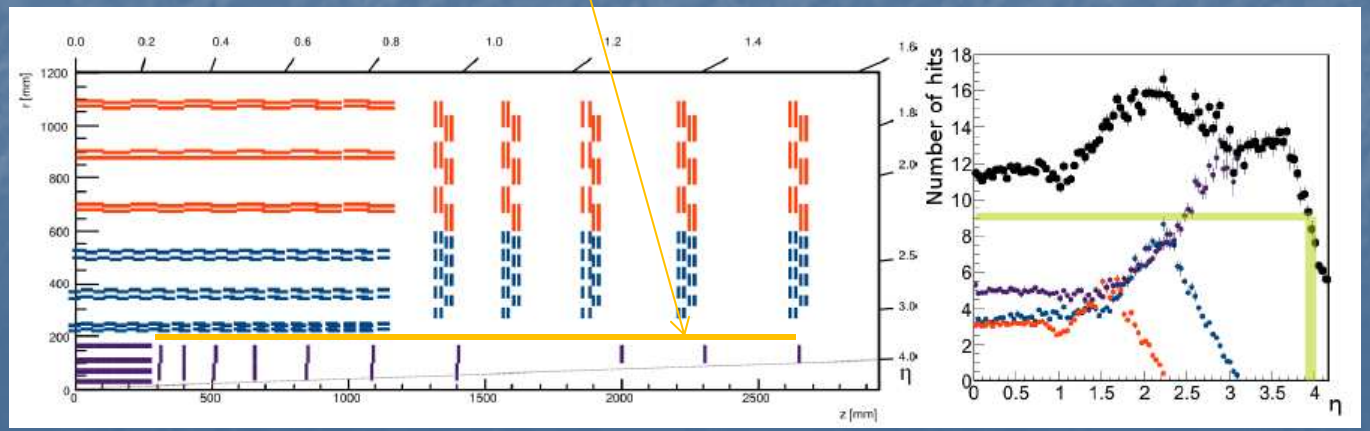


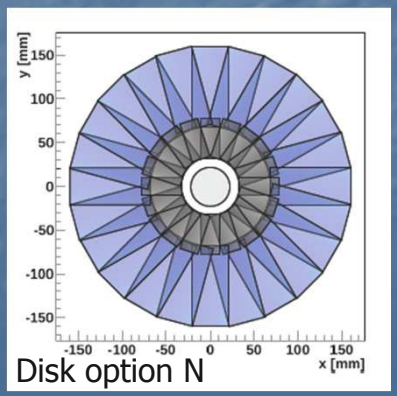




G. Sguazzoni

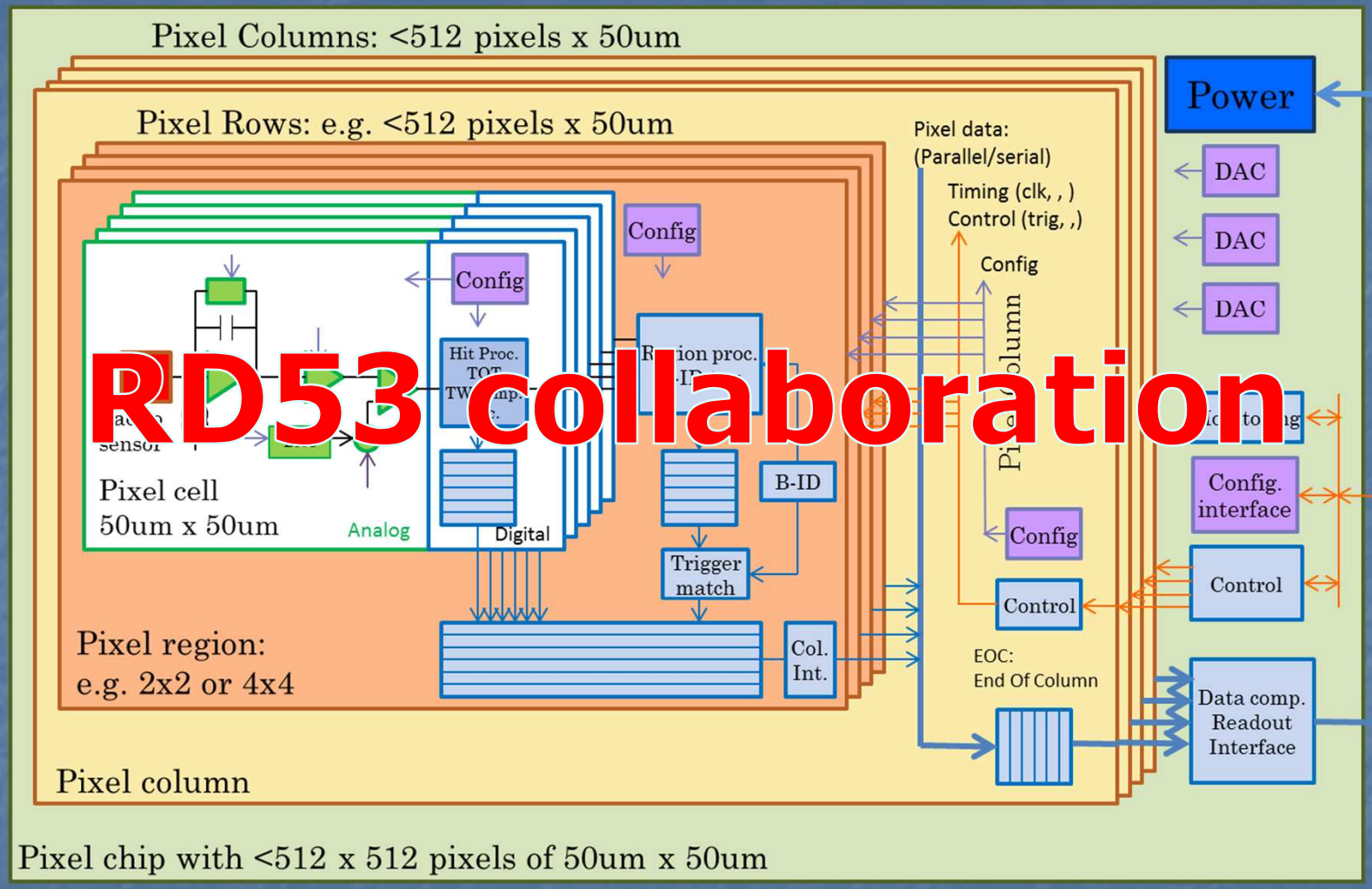
| #Layer | R | ΔR | #faces | Active length in XY | Overlap | Module Size |
|---|---|---|---|---|---|---|
| 1 | 31 | 3 | 10 | 21 (=1 chip) | 0.85 | 4x1 |
| 2 | 63 | 3 | 20 | 21 (=1 chip) | 1.05 | 4x1 |
| 3 | 103 | 3 | 16 | 42 (=2 chips) | 1.01 | 4x2 |
| 4 | 156 | 3 | 24 | 42 (=2 chips) | 0.92 | 4x2 |

*Dimensions in [mm]*



# 3rd generation pixel architecture

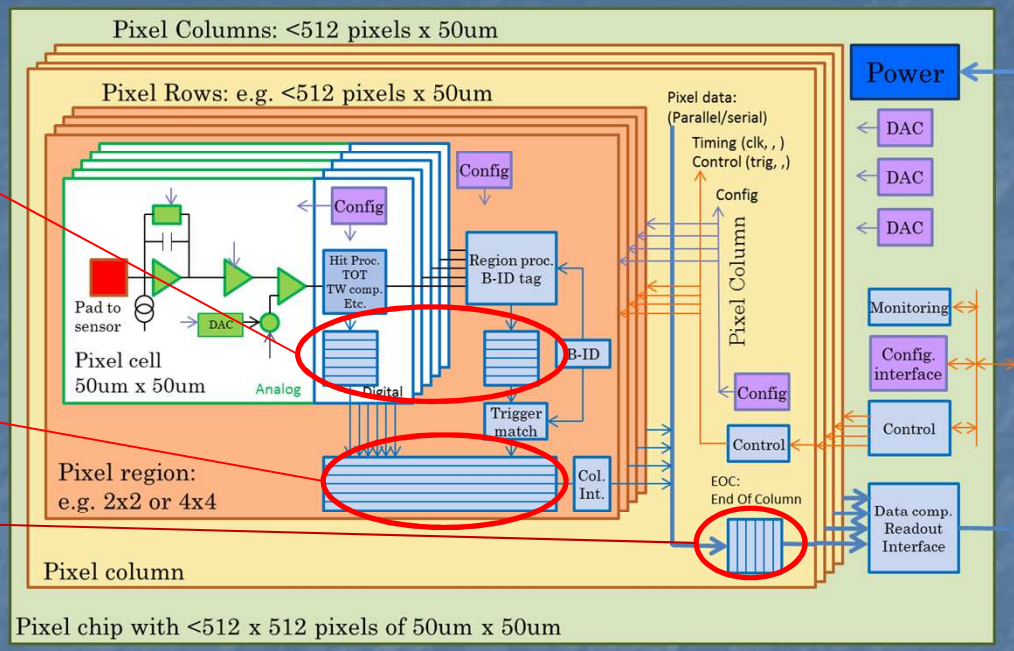





- 95% digital (as FEI4)
- Charge digitization (TOT or ADC)
- ~200k pixel channels per chip
- Pixel regions with buffering
- Data compression in End Of Column
- Chip size: ~20 x 20 mm$^2$

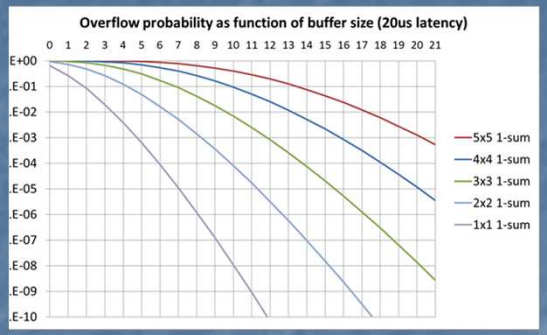
# Buffering requirements

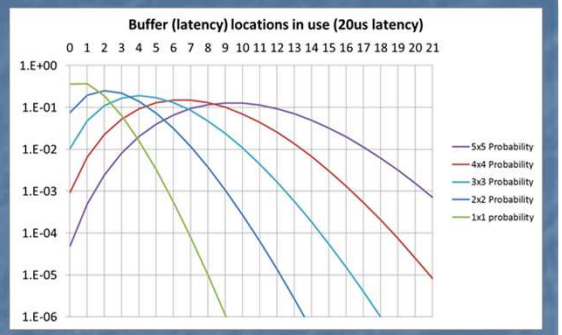
- Data buffering
  - A. **During trigger latency**
    - Location: Pixel region
    - Size: Hit rate, Trigger latency, PR organization/sharing, Data per hit ( TOT/ADC, BX-ID, etc.)
    - Different buffer schemes possible
  - B. Data out of PR to EOC
    - Location: PR region
    - Small FIFO
  - C. Assemble and compress all hits
    - FIFO buffer per pixel column to align event fragments
    - Buffers for compression/extraction ?.
    - Output FIFO
- Acceptable losses:
  - Hit loss at worst case locations (L1)
    - Whish: <0.1%
    - Acceptable: <1%, in worst case locations.
  - Event loss: Never, as implies system de-sync.

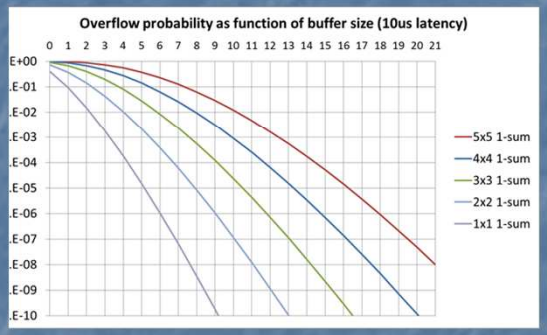


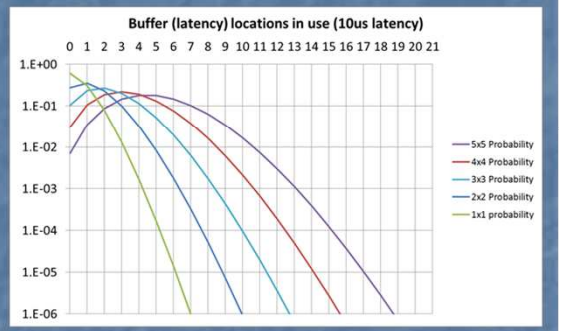
# Hit buffer in pixel regions

- Hit losses (2GHz/cm$^2$) 4x4:
  - **16 hit buffer**
    - Loss 10us: $10^{-7}$
    - Loss 20us: $10^{-3}$
  - **8 hit buffer**
    - Loss 10us: $10^{-2}$
    - Loss 20us: $10^{-1}$
- Current estimates indicates that 16 hit buffer is feasible in 65nm
  - Uncertainty on radiation tolerance and implications on physical size of memory elements !

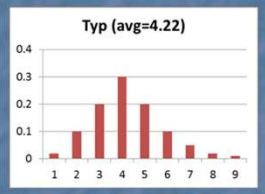



| Required buffer locations (Bits/pixel) | | | | |
|---|---|---|---|---|
| PR | 20us, 1% | 20us, 0.1% | 10us, 1% | 10us, 0.1% |
| 1x1 | 4 (56) | 5 (70) | 3 (42) | 4 (56) |
| 2x2 | 7 (45) | **9 (59)** | 5 (33) | 6 (39) |
| 3x3 | 10 (51) | 12 (61) | 6 (31) | 8 (41) |
| 4x4 | 14 (65) | **16 (74)** | 8 (37) | 11 (51) |
| 5x5 | 18 (79) | 21 (92) | 11 (48) | 13 (57) |

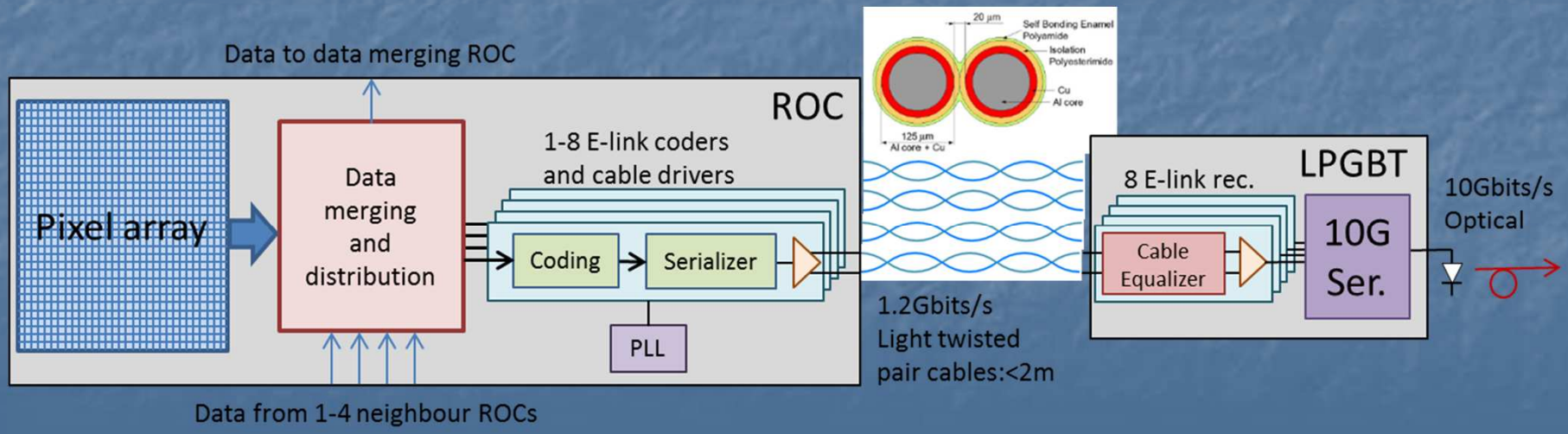



Cluster size distribution

Hit rate: 2GHz/cm$^2$

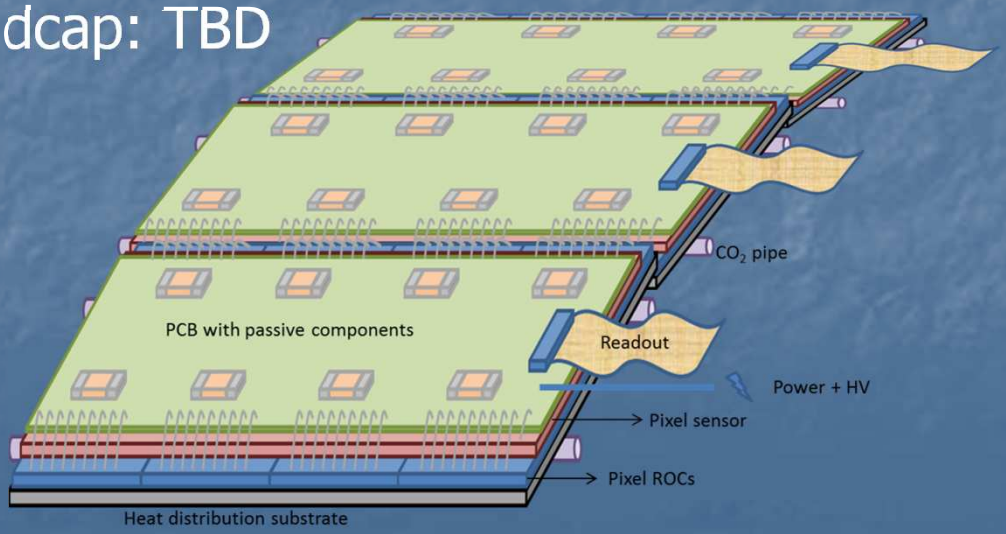
# Readout

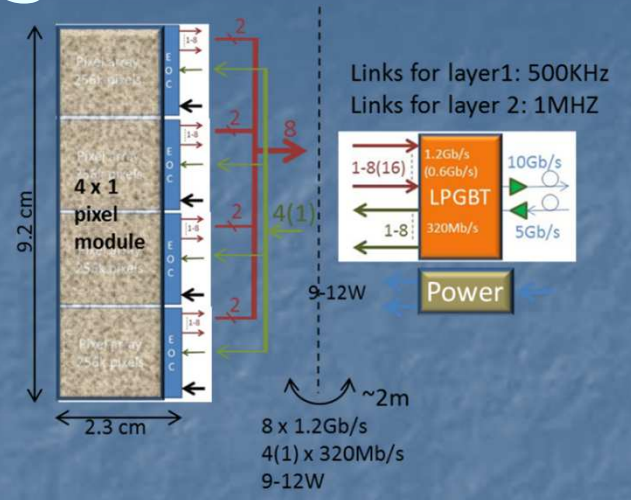
- High speed electrical links: 1.2Gbits/s
  - Limited speed:
    - Radiation damage on pixel chip
    - Distance: ~2m.
    - Very light cable
    - Modularity and flexibility:
      - Multiple links per chip for very high rate regions
      - Merging data from multiple chips (2-4) for low rate regions
    - Appropriate interface at input of LPGBT
- ~5K low mass E-links for 500KHz trigger rate

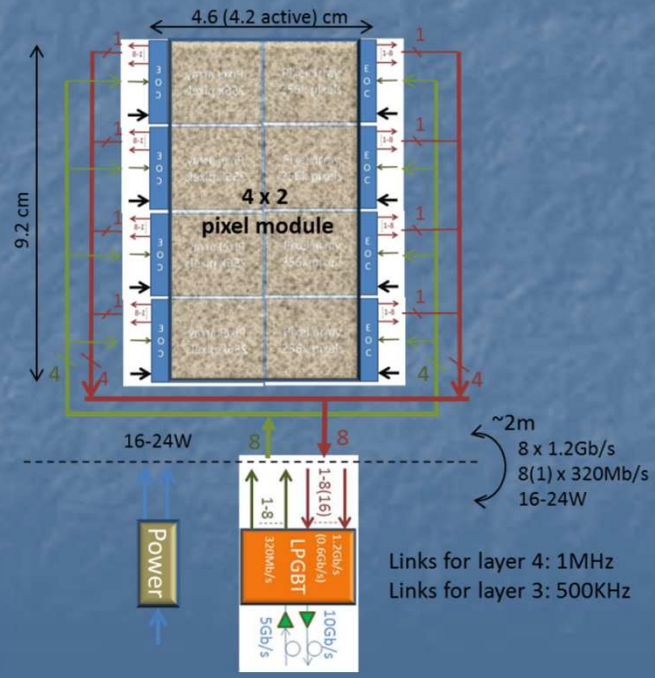


# Pixel modules

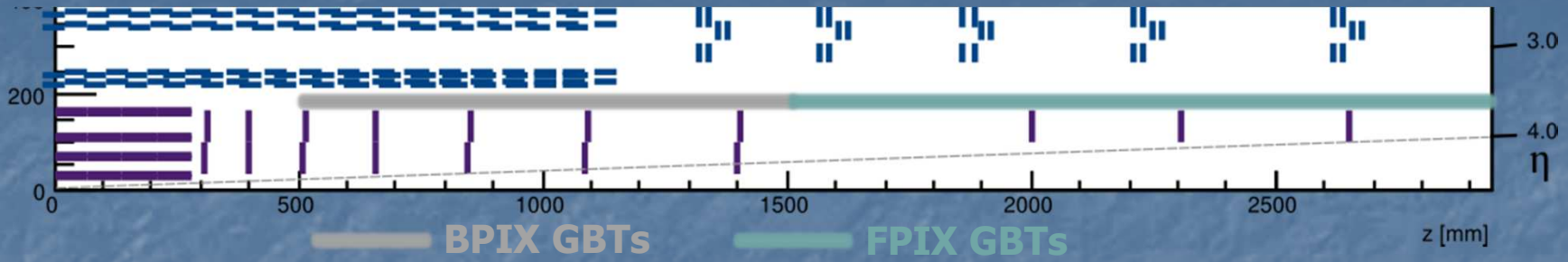
- 4x1 pixel module for layer 1 & 2
  - Different link configurations:
    Trigger: 500kHZ (1MHz)
    - Layer 1: 8 (16) x 1.2Gbits/s E-links
    - Layer 2: 4 (8) x 1.2Gbits/s E-links
- 4x2 pixel module for layer 3 & 4
  - Different link configurations
    Trigger: 500kHZ (1MHz)
    - Layer 3: 8(16) x 1.2Gbits/s E-links
    - Layer 4: 4(8) x 1.2Gbits/s E-links
      On-chip data merging between 2-4 pixel chips for low rates
- Endcap: TBD



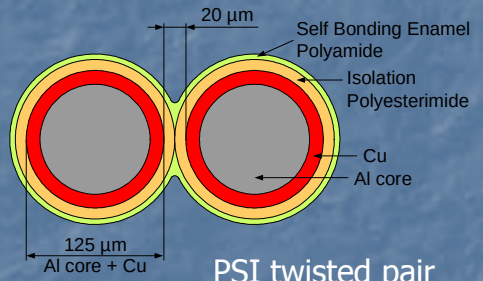



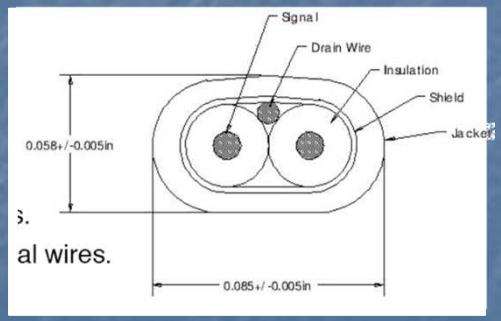
# Readout cabling




- ~2m cabling from pixel module to LPGBT
  - Assume that LPGBT and opto can survive on service cylinder (100Mrad)
- Data rate: 1.2Gb/s (initial proposal/guess)
  - Appropriate interface to LPGBT
  - Optimal for minimal mass per Gbits/s ?
- Cable types:
  - PSI twisted pair: Cupper cladded aluminium, no shield
    - Phase1: 320Mb/s over 1m
    - Phase2: 1.2Gbits/s over 2m with active cable compensation ? Crosstalk ?
  - Habia UBT 3601 ST 2
  - Twinax cable: 4-6Gb/s over 4-6m




PSI twisted pair




Twinax

| | Estimated mass in g/m | | |
|---|---|---|---|
| | PSI | HABIA | TWINAX |
| Cu | 0.027 | 0.339 | 0.083 |
| Alu | 0.058 | 0.330 | 1.390 |
| Insulator | 0.011 | 0.194 | 1.994 |
| **Total** | **0.096** | **0.863** | **3.467** |

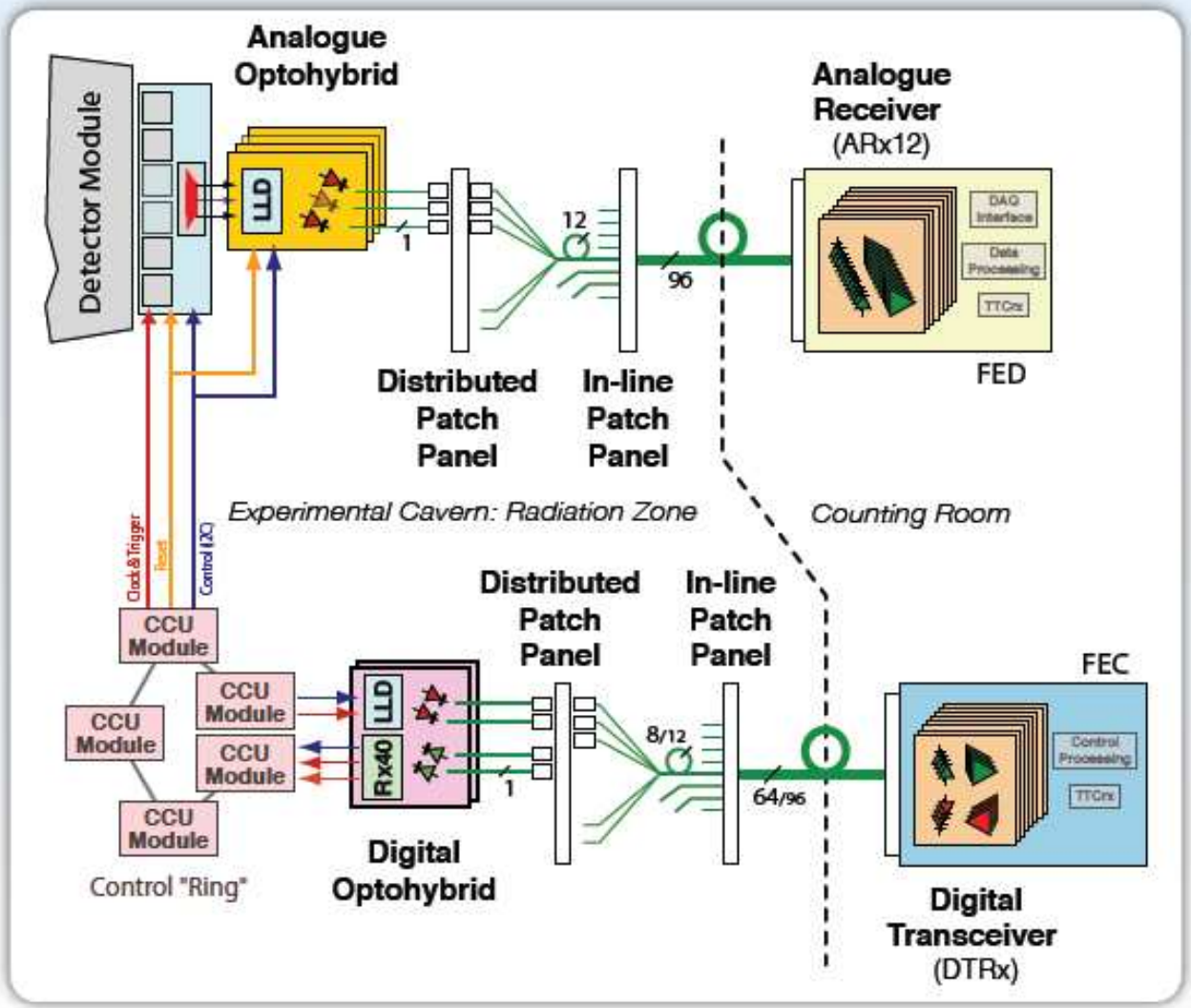
# Getting data into DAQ

# Data and Link types

- Readout - DAQ:
  - Unidirectional
  - Event frames.
  - High rate
  - Point to point
- Trigger data:
  - Unidirectional
  - High constant data rate
  - Short and constant latency
  - Point to point
- Detector Control System
  - Bidirectional
  - Low/moderate rate ("slow control")
  - Bus/network or point to point
- Timing: Clock, triggers, resets
  - Precise timing (low jitter and constant latency)
  - Low latency
  - Fan-out network (with partitioning)

- We often keep these data types physically separate and each link type has its own specific implementation
- Multiple exceptions
  - Merge timing and control/monitoring: CMS CCU, LHCb SPECS, ,
  - Combine readout and control: ALICE DDL (Used for DCS ?),
  - Use same link implementation for readout and trigger data
    - But never have readout and trigger data on same physical link
  - Down: Control data with Timing. UP: Monitoring data with Readout: ATLAS pixel/SCT, ,

# Example: CMS tracker links




| Readout System | |
|---|---|
| INL | 1% |
| SpNR | 48 dB |
| BWtyp | 70 MHz |
| Gain | 0.8 V/V |
| ~40000 Fibres | |

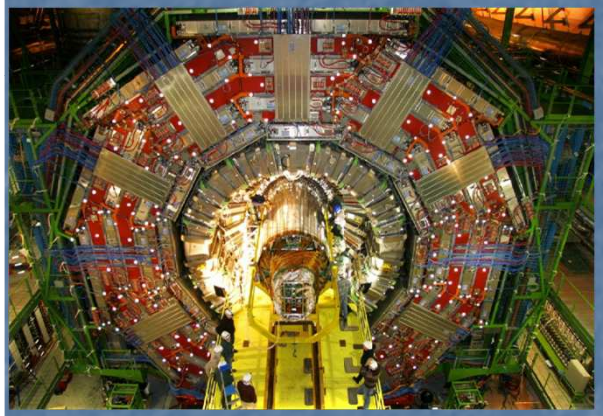
| Control System | |
|---|---|
| Data-Rate | 80Mb/s |
| BER | 10-12 |
| ~2500 Fibres | |

| |
|---|
| Length: 40-65m |
| Low Mass & Volume |
| Non-Magnetic |
| Radiation Resistant |

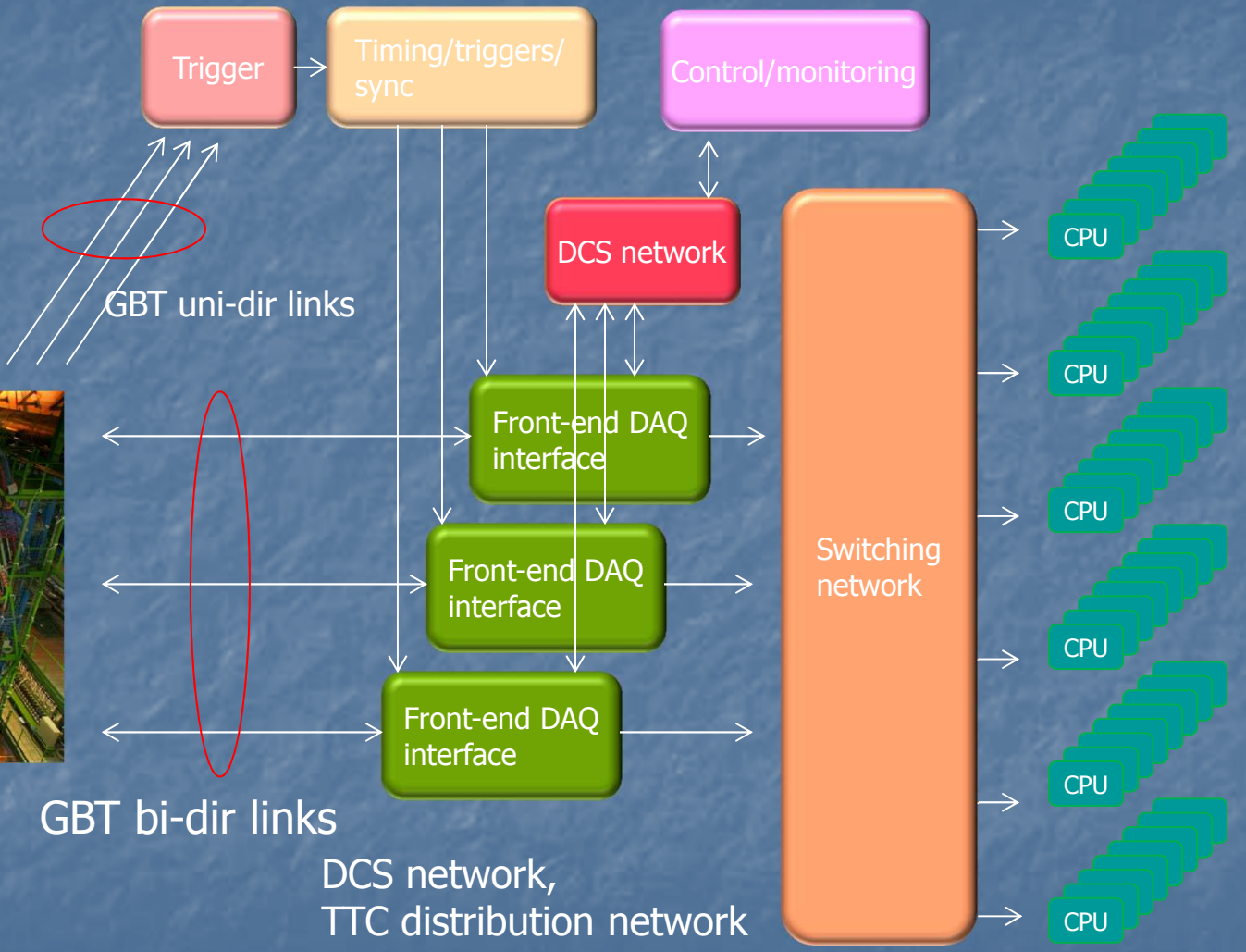
# How can this look

10K – 1G rad


Max 4T

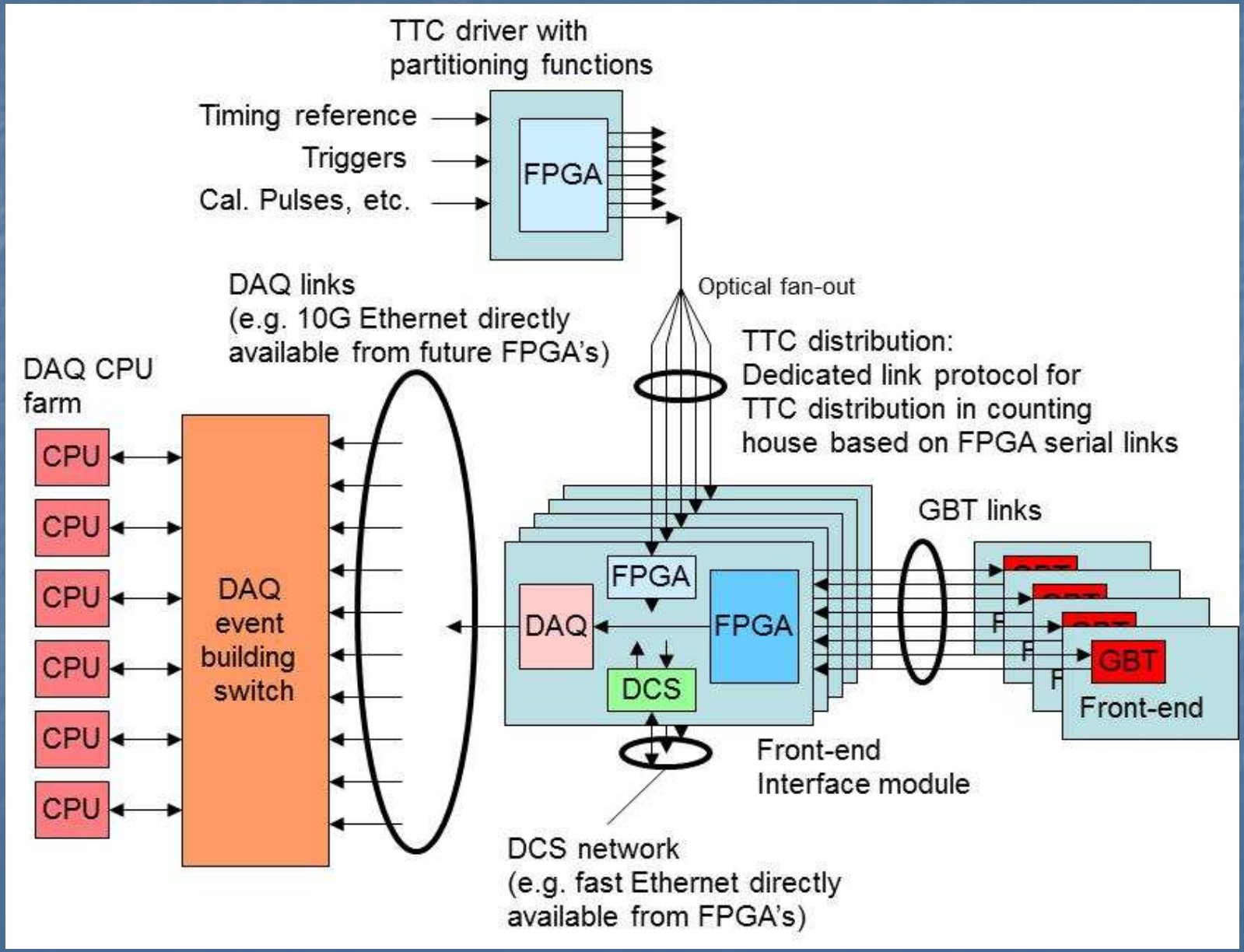



~zero mass

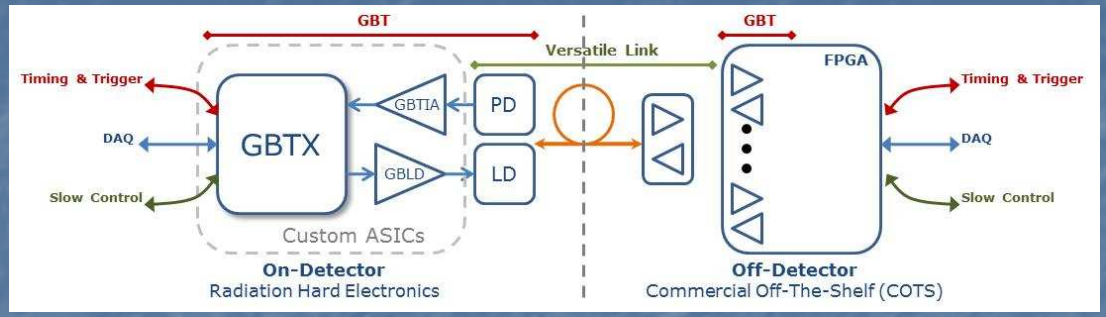


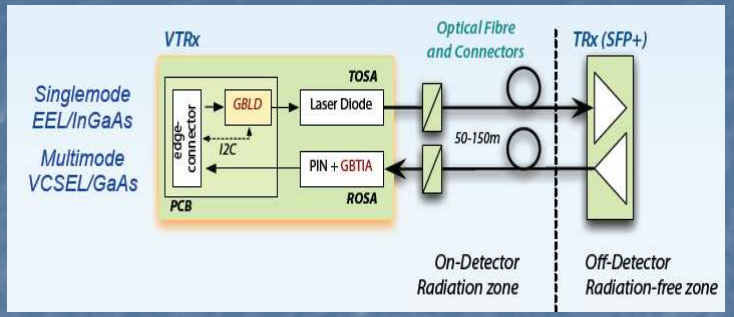

DCS network,
TTC distribution network
and DAQ network
Fully in counting house (COTS)

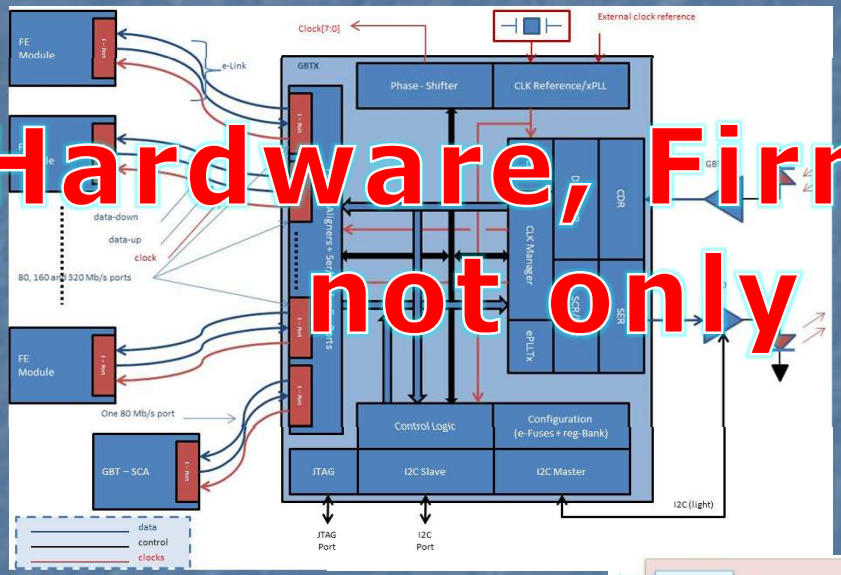
# DAQ interface



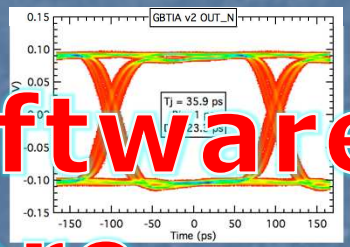
# GBT, Versatile, GLIB



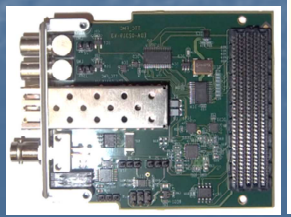



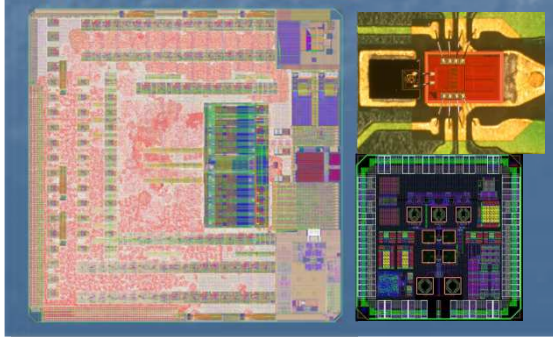



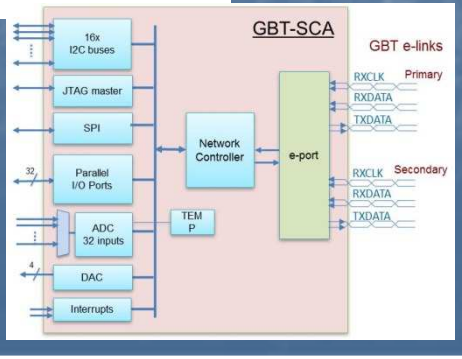













**Hardware, Firmware, Software, not only Dream-ware**