The Belle II upgrade

B factories
- motivation for upgrade

SuperKEB

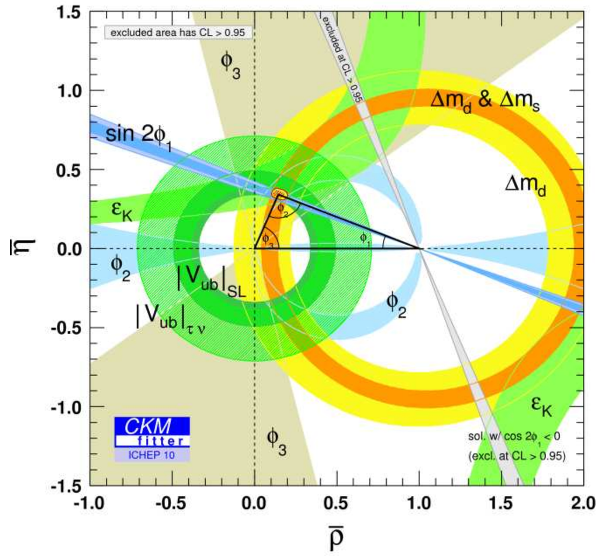
Belle II
- detector overview
- closer look: PXD

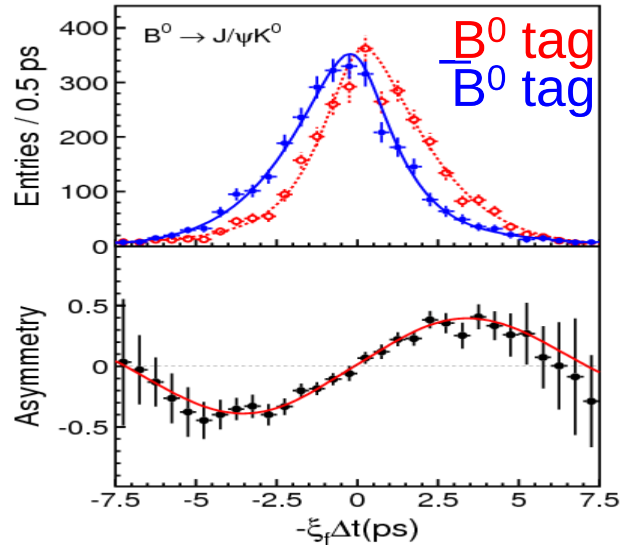
The DEPFET sensor
- principle & properties
- Belle II DEPFET module
  - test beams
  - radiation hardness
  - material
  - gated operation
- System aspects

Conclusions

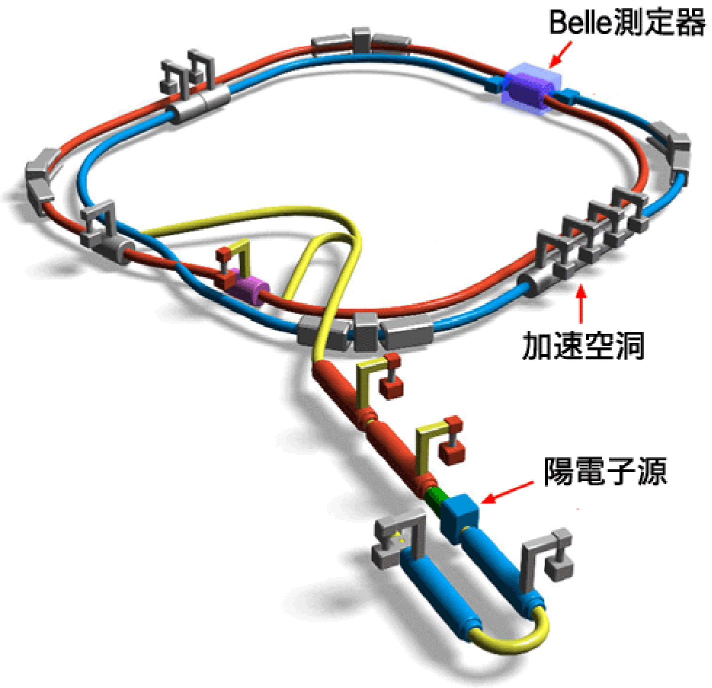
B-factory Detectors – a huge success!

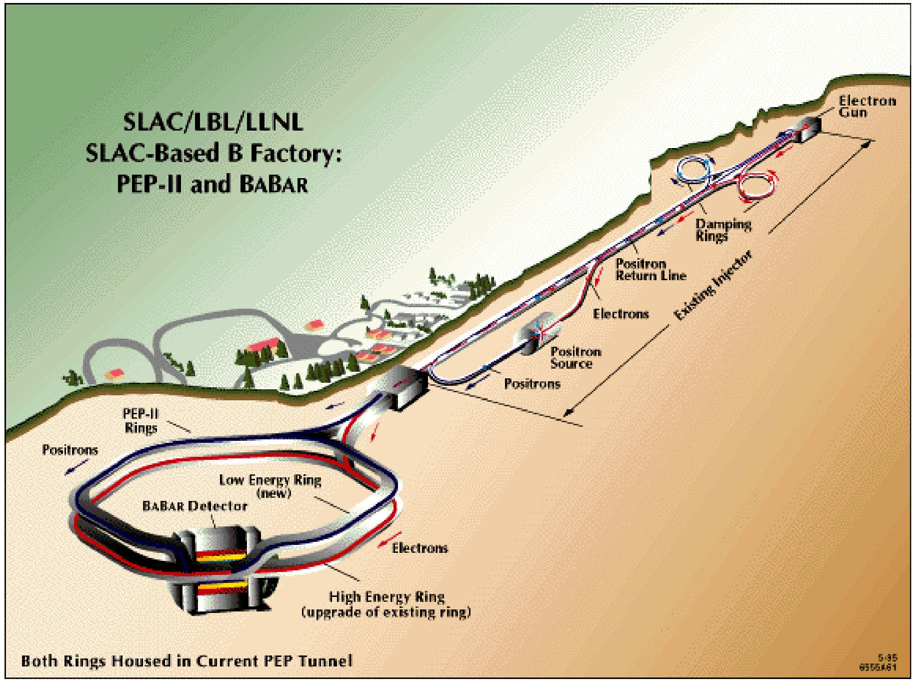
- Measurements of CKM matrix elements and angles of the unitarity triangle
- Observation of direct CP violation in B decays
- Measurements of rare decays (e.g., B→τν, Dτν)
- b→s transitions: probe for new sources of CPV and constraints from the b→sγ branching fraction
- Forward-backward asymmetry (A_{FB}) in b→sll has become a powerfull tool to search for physics beyond SM.
- Observation of D mixing
- Searches for rare τ decays
- Observation of new hadrons





Asymmetric B factories





$\sqrt{s}=10.58$ GeV

$e^+ \rightarrow \Upsilon(4s) \leftarrow e^-$

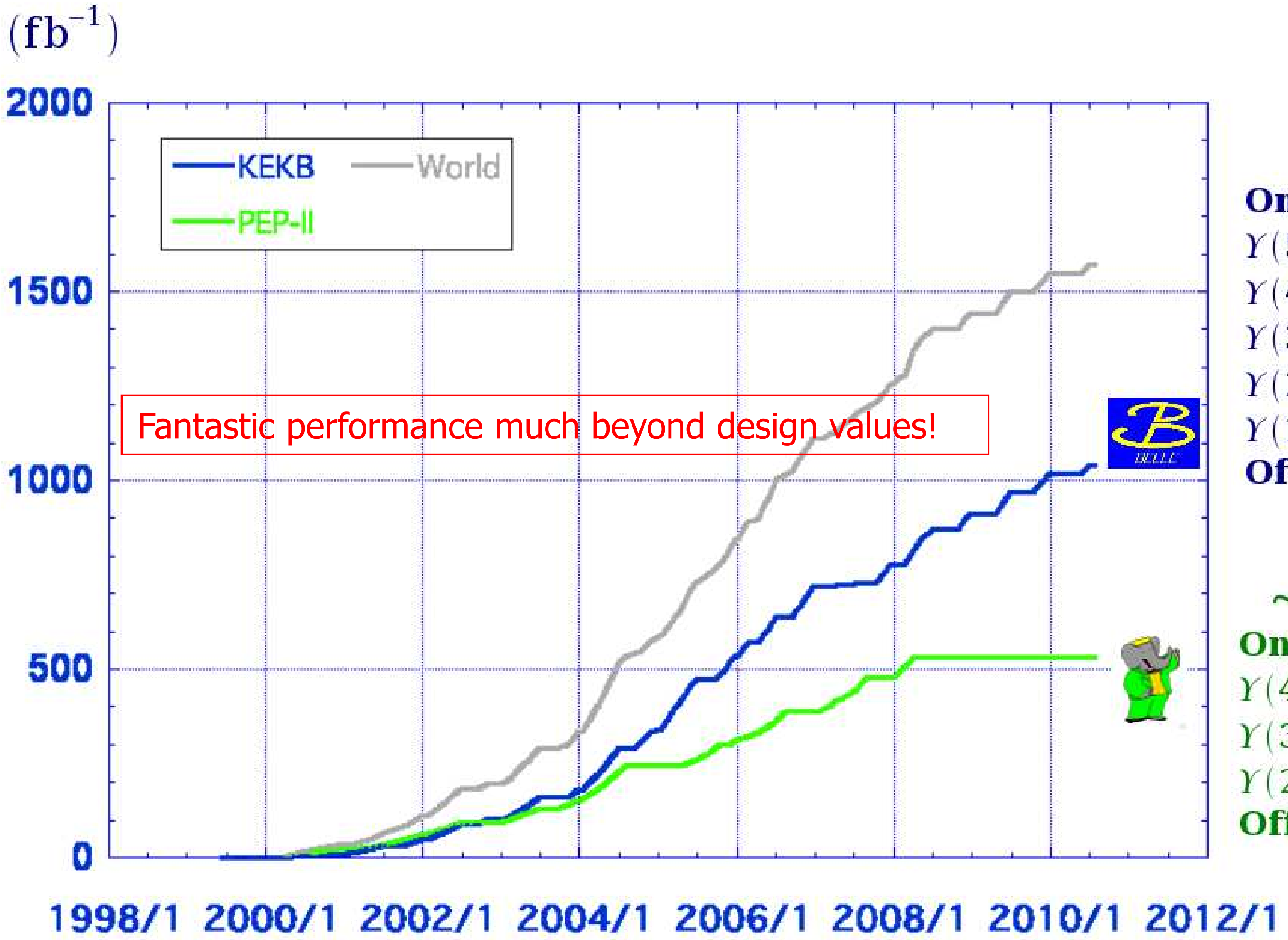
$\Upsilon(4s) \rightarrow B\,\bar{B}$

$\Delta z \sim c\beta\gamma t_B$

$\sim 200\mu m$

BaBar	$p(e^-)=9$ GeV	$p(e^+)=3.1$ GeV	$\beta\gamma=0.56$
Belle	$p(e^-)=8$ GeV	$p(e^+)=3.5$ GeV	$\beta\gamma=0.42$
Belle II	$p(e^-)=7$ GeV	$p(e^+)=4$ GeV	$\beta\gamma=0.28$

Luminosity at the B Factories



> 1 ab^{-1}

On resonance:

$\Upsilon(5S)$: 121 fb^{-1}

$\Upsilon(4S)$: 711 fb^{-1}

$\Upsilon(3S)$: 3 fb^{-1}

$\Upsilon(2S)$: 24 fb^{-1}

$\Upsilon(1S)$: 6 fb^{-1}

Off reson./scan:

~ 100 fb^{-1}

~ 550 fb^{-1}

On resonance:

$\Upsilon(4S)$: 433 fb^{-1}

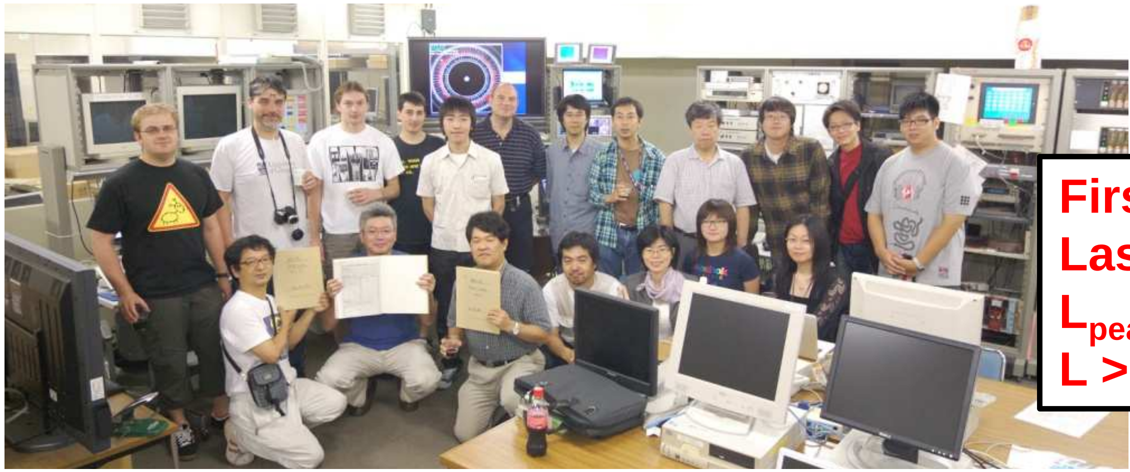
$\Upsilon(3S)$: 30 fb^{-1}

$\Upsilon(2S)$: 14 fb^{-1}

Off resonance:

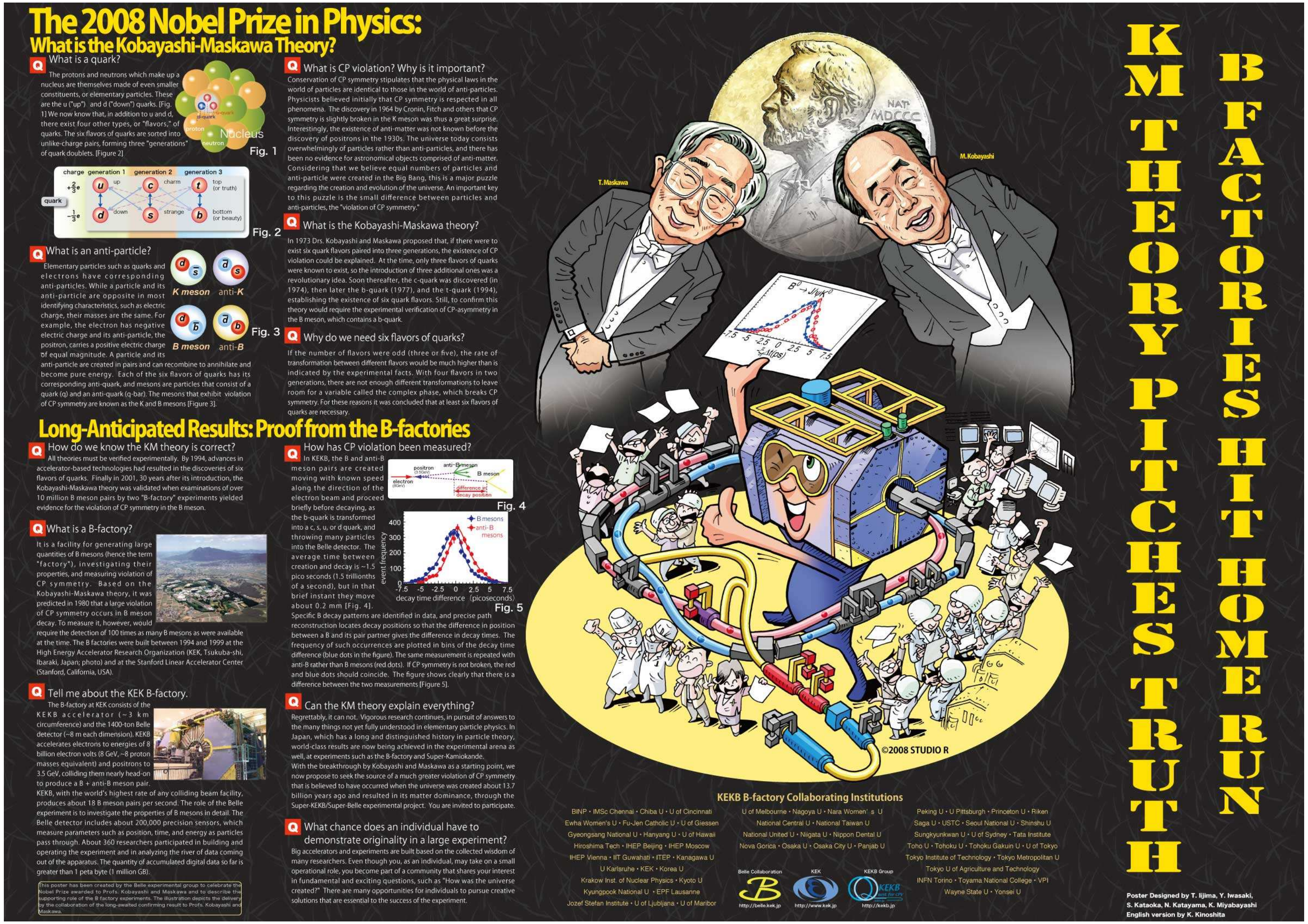
~ 54 fb^{-1}

Last KEKB beam abort: June 30, 2010



First physics run on June 2, 1999
Last physics run on June 30, 2010
$L_{peak} = 2.1 \times 10^{34}/cm^2/s$
$L > 1 ab^{-1}$

Nobel Prize in Physics 2008



Confirmation by Babar and Belle

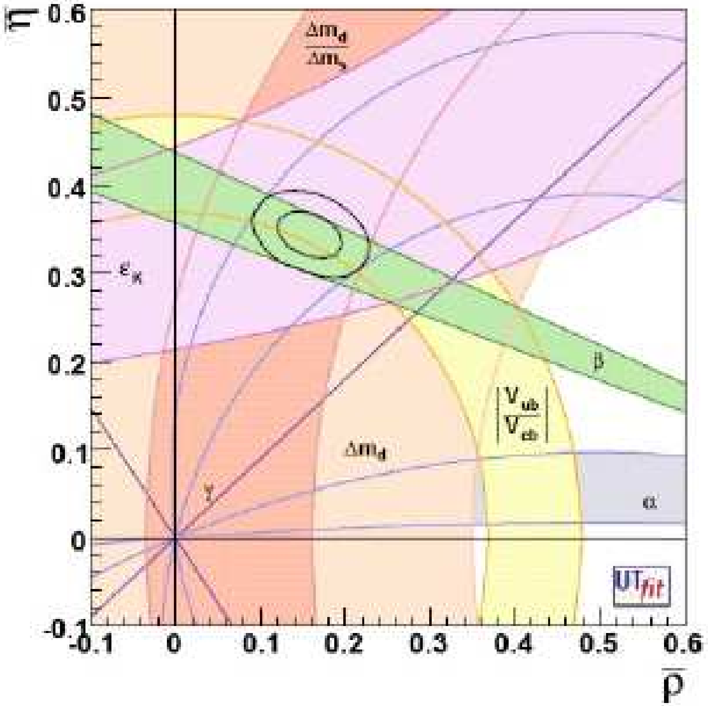
Are we done yet ?

Motivation for Upgrade

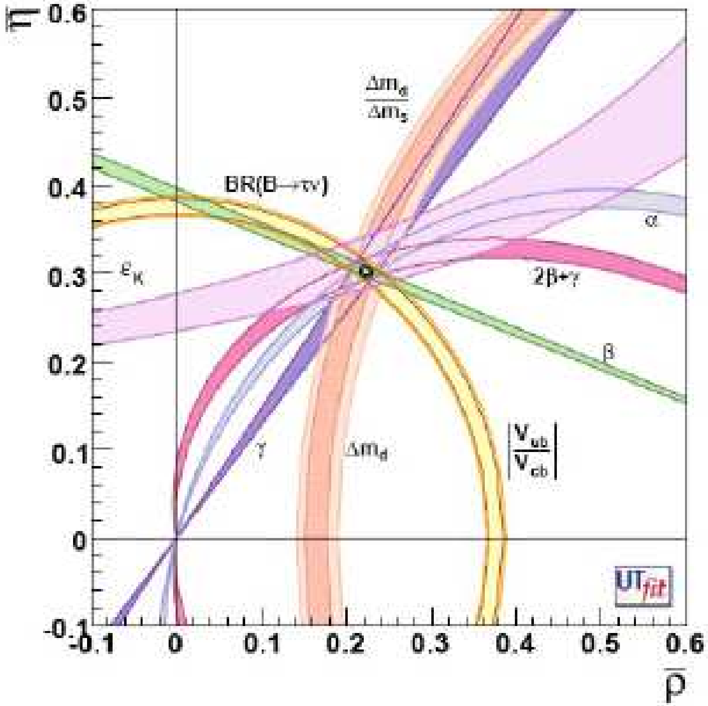
Measure CKM elements as precisely as possible
Overconstrain unitarity triangle
Look for deviations from SM

$\Phi_1/\beta = (21.\pm1\ 0.9)^o$
$\Phi_2/\alpha = (88.4\ \pm5.6)^o$
$\Phi_3/\gamma = (70\ \pm29)^o$

=> Need about 50 ab^{-1}

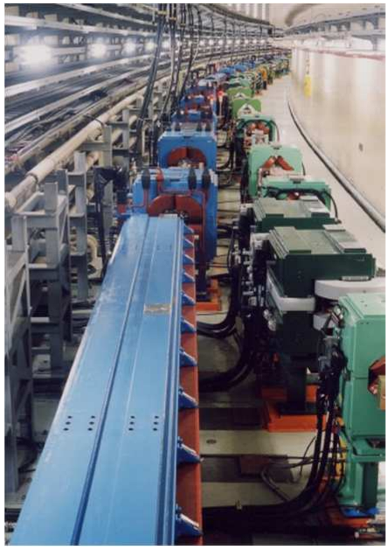


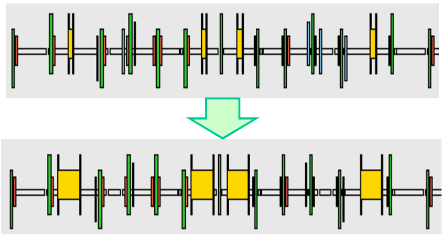
Babar/Belle

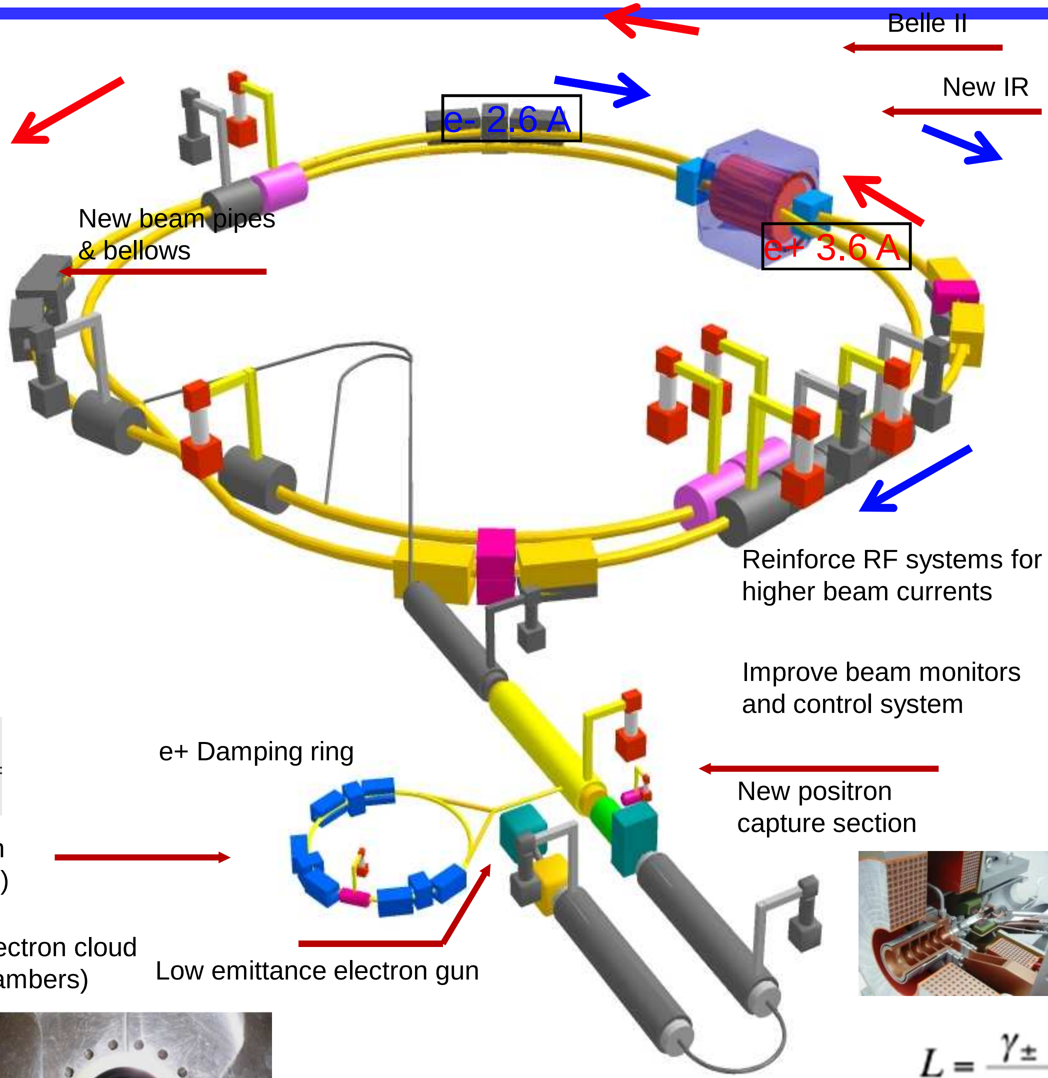


With 50 ab^{-1} (same central values)

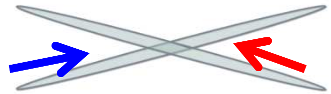
KEKB to SuperKEKB







Colliding bunches



New superconducting final focusing magnets near the IP

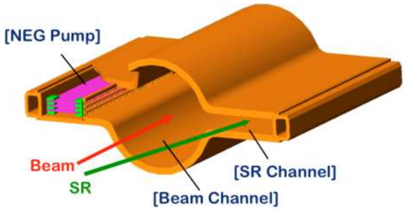
Reinforce RF systems for higher beam currents

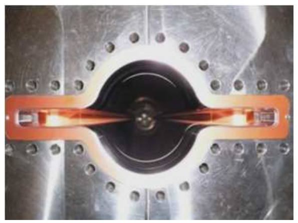
Improve beam monitors and control system

New positron capture section

Redesign the lattice to squeeze the emittance (replace short dipoles with longer ones, increase wiggler cycles)

Replace beam pipes to suppress electron cloud (TiN-coated beam pipe with antechambers)



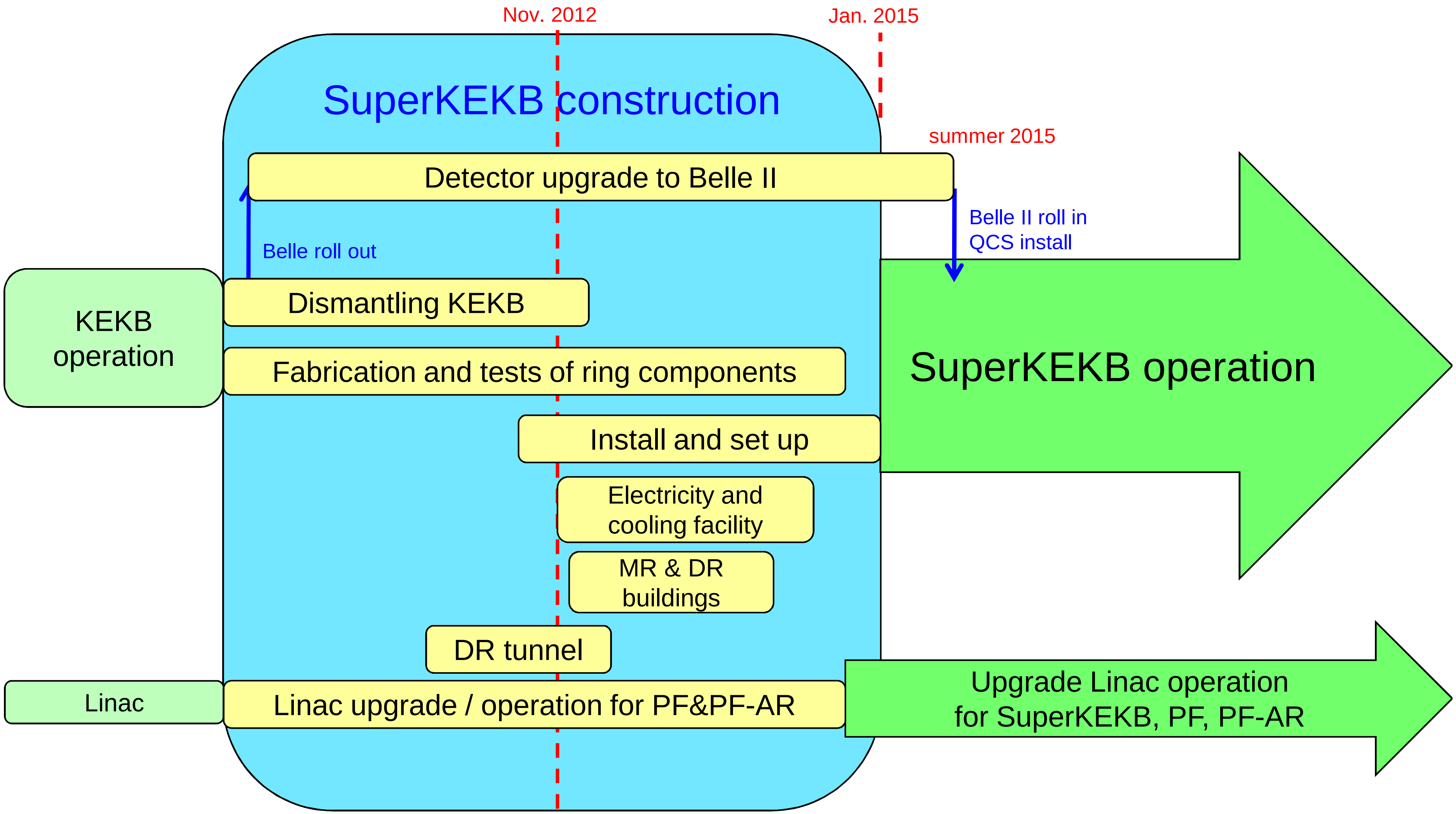


$$L = \frac{\gamma_\pm}{2er_e}\left(1+\frac{\sigma_y^*}{\sigma_x^*}\right)\left(\frac{I_\pm \xi_{\pm y}}{\beta_y^*}\right)\left(\frac{R_L}{R_y}\right)$$

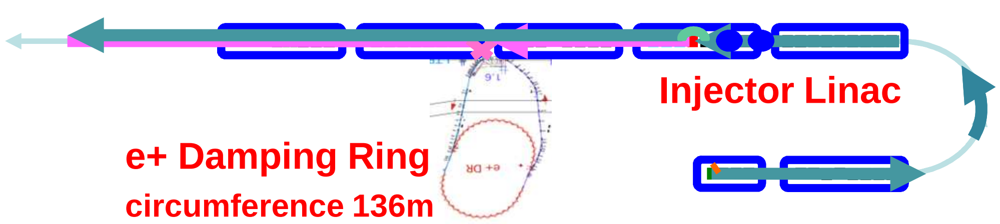
To get x40 higher luminosity

SuperKEKB Schedule

Calendar	2010	2011	2012	2013	2014	2015	2016	2017	· · ·
Japan FY	2010	2011	2012	2013	2014	2015	2016	2017	· ·



superKEKB construction



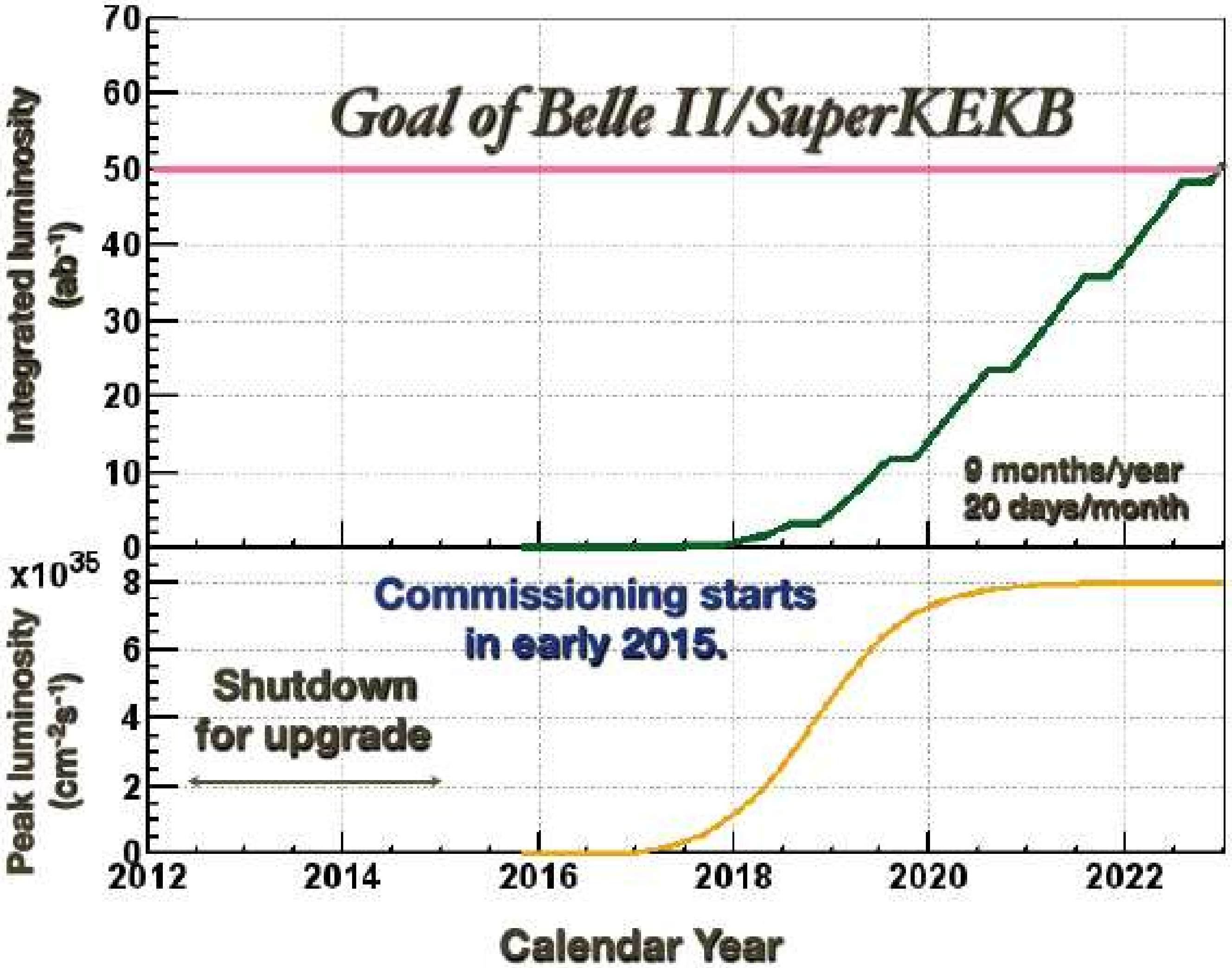
beam pipes after baking and TiN coating. They are temporary stocked until moved to tunnel

Tunnel construction for new bending ring

100 new bending pipes are installed

Machine upgrade on schedule

SuperKEKB luminosity profile



Requirements for the Belle II detector

Critical issues at L= 8 x 10^{35}/cm^2/sec

- **Higher background (×10-20)**

  - radiation damage and occupancy
  - fake hits and pile-up noise in the EM Calorimeter

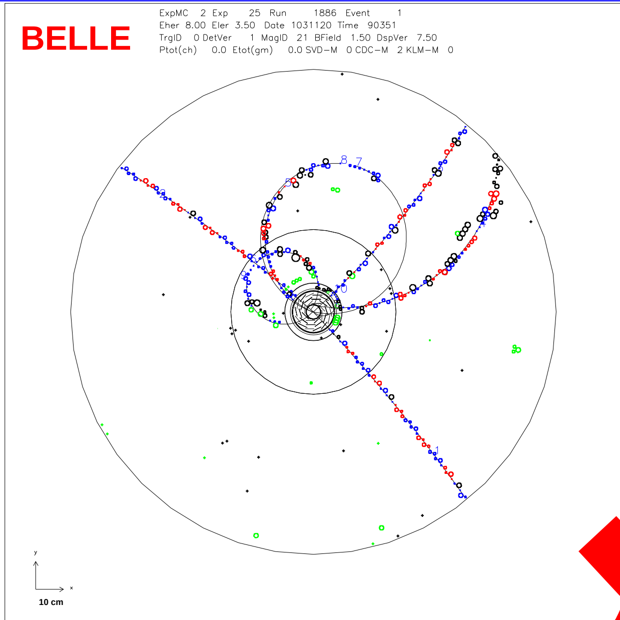
- **Higher event rate (×10)**

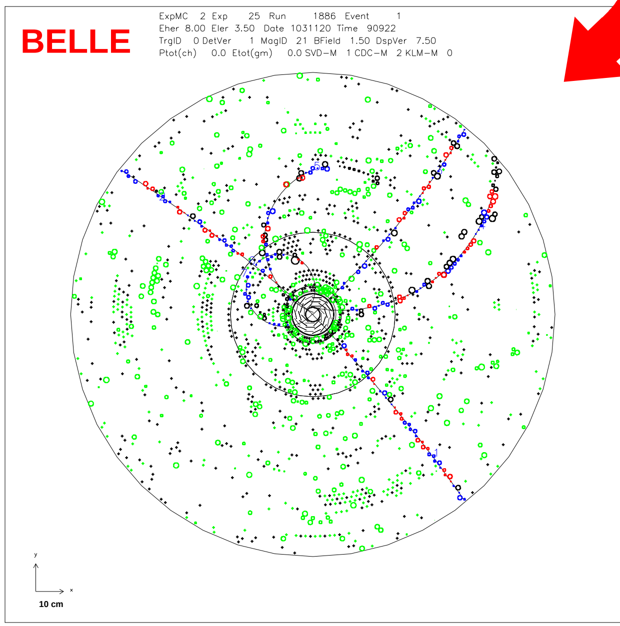
  - higher rate trigger, DAQ and computing

- **Special features required**

  -- $\gamma\beta$ reduced by a factor of 2: compensated by improved vertexing

Result: significant upgrade

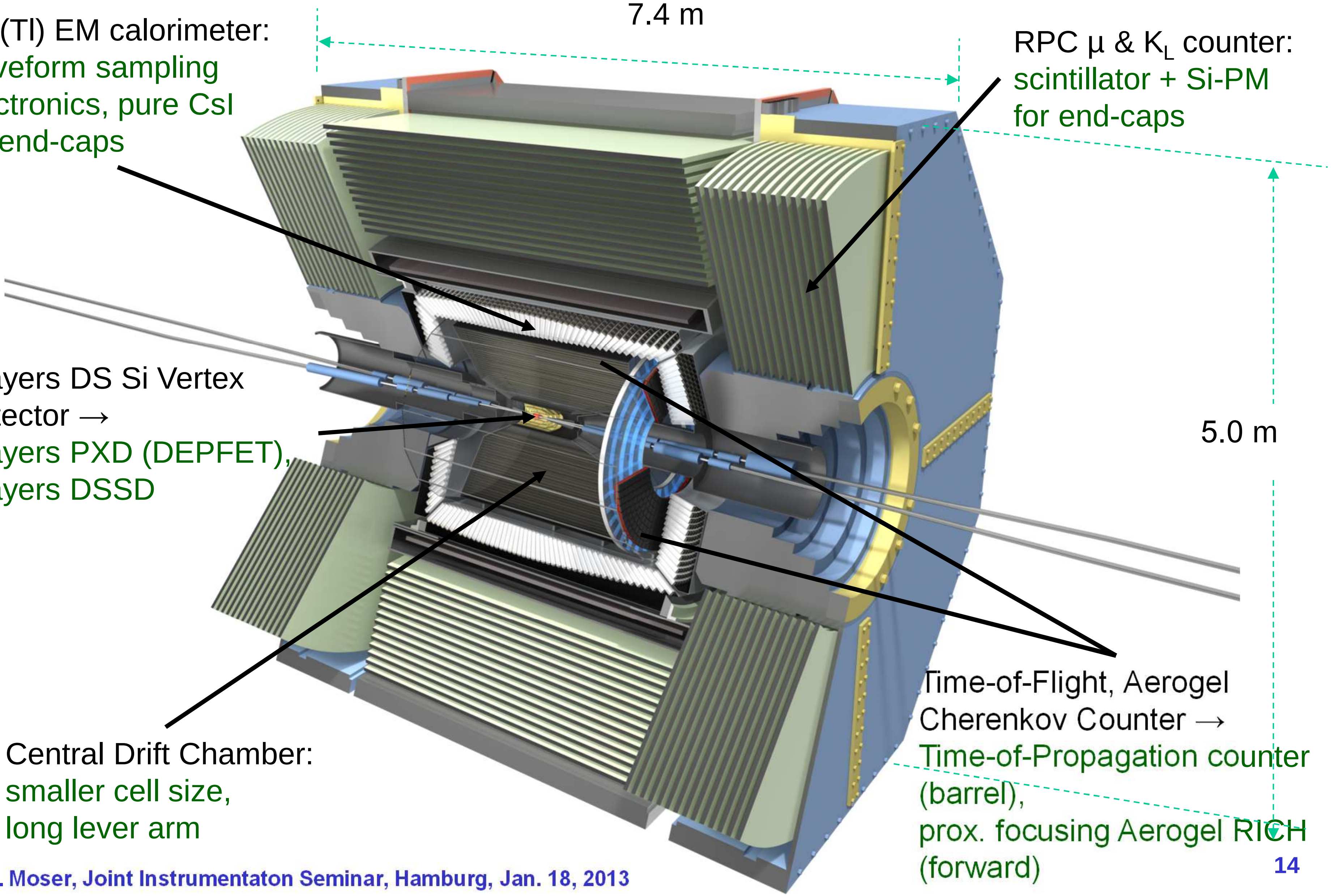




Belle II: design concept

CsI(Tl) EM calorimeter:
waveform sampling electronics, pure CsI for end-caps

RPC μ & K_L counter:
scintillator + Si-PM for end-caps



4 layers DS Si Vertex Detector →
2 layers PXD (DEPFET),
4 layers DSSD

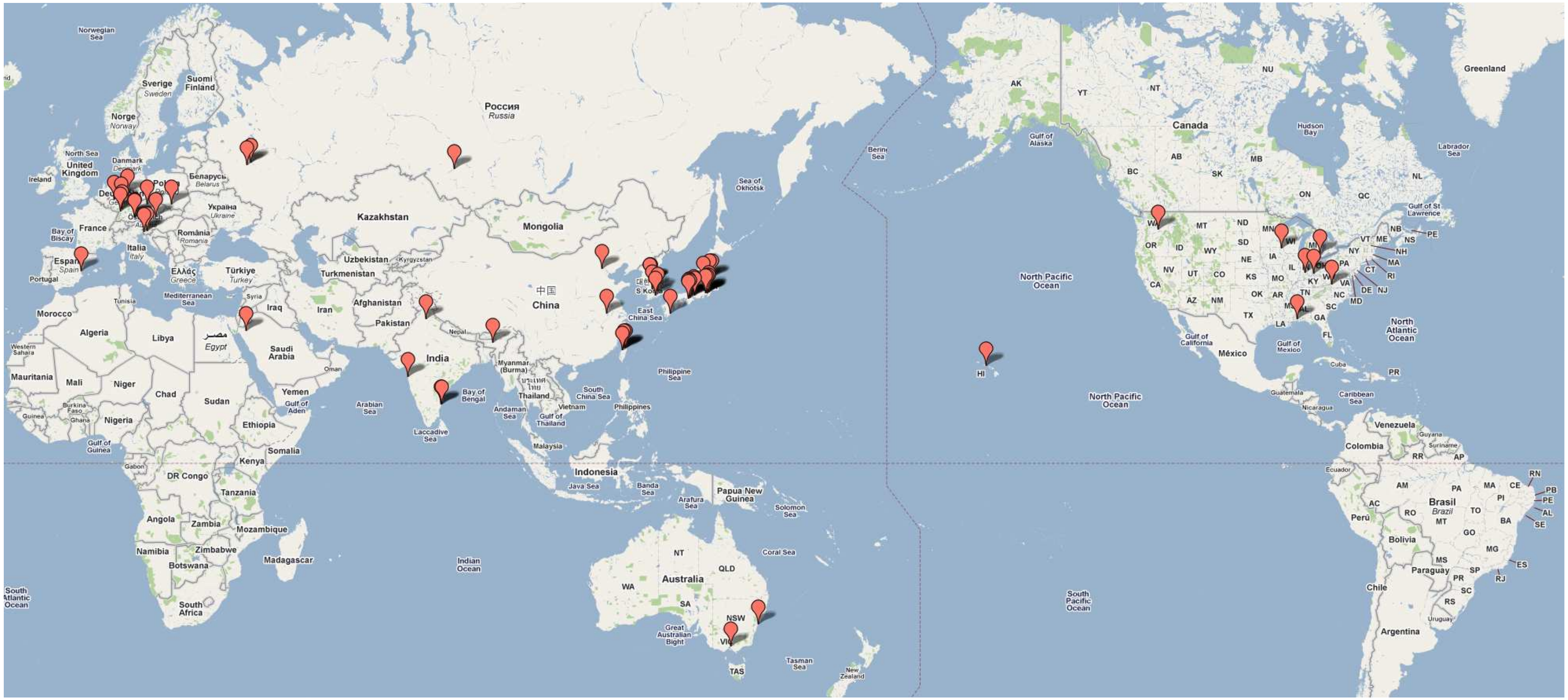
Central Drift Chamber:
smaller cell size,
long lever arm

Time-of-Flight, Aerogel Cherenkov Counter →
Time-of-Propagation counter (barrel),
prox. focusing Aerogel RICH (forward)

Belle II Collaboration

15 countries,
~60 institutions (9 German)

~400 collaborators

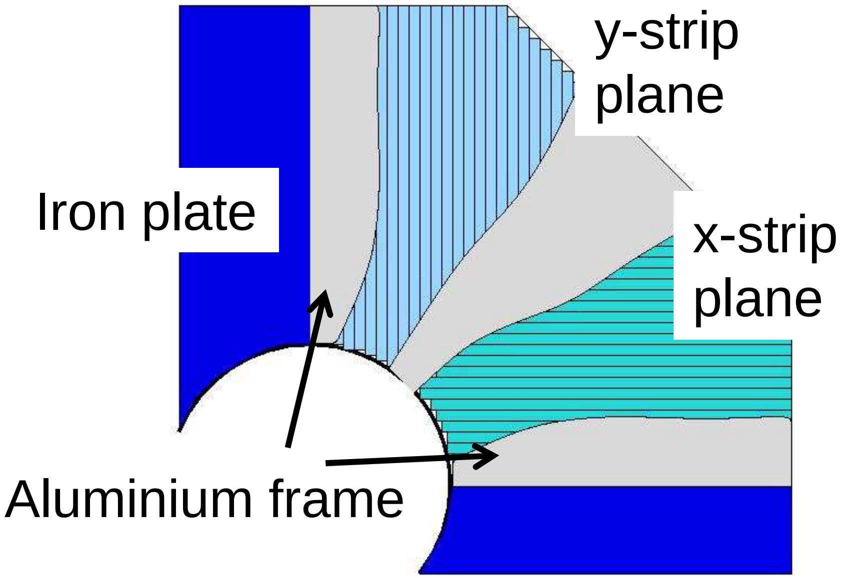


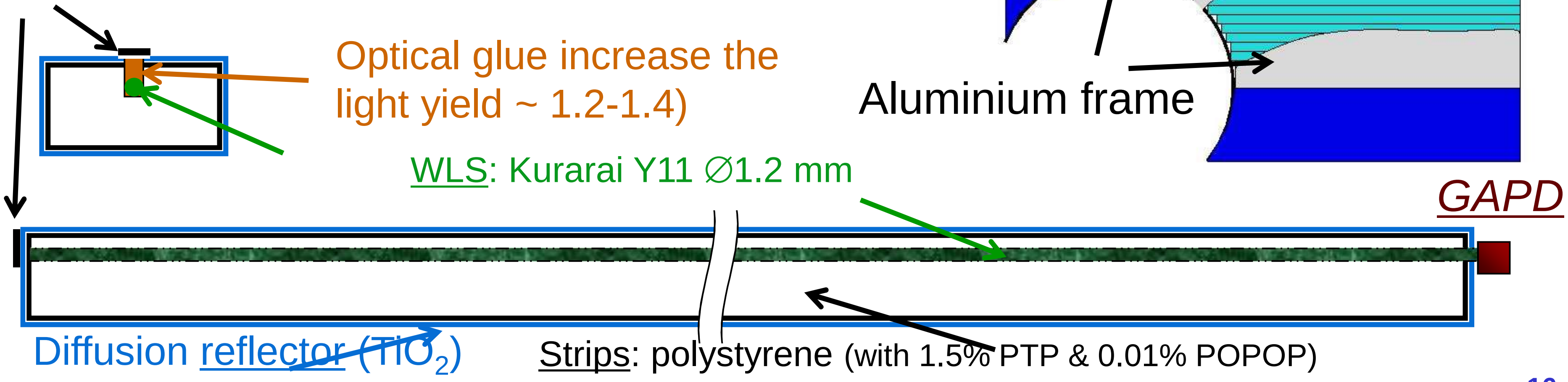
Endcap KLM upgrade

Replace RPCs with Scintillator-based approach

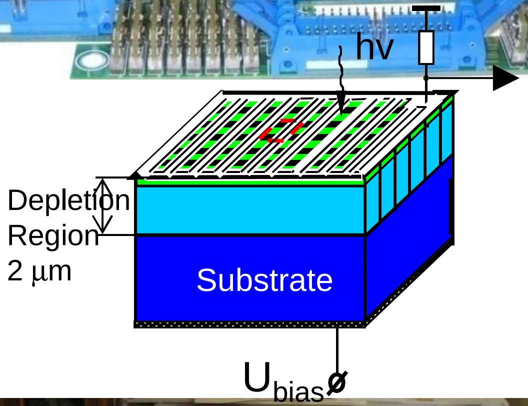
- » Two independent (x and y) layers per superlayer made of orthogonal strips with WLS read out
- » Photo-detector = avalanche photodiode in Geiger mode (SiPM)
- » ~150 strips in one 90º sector

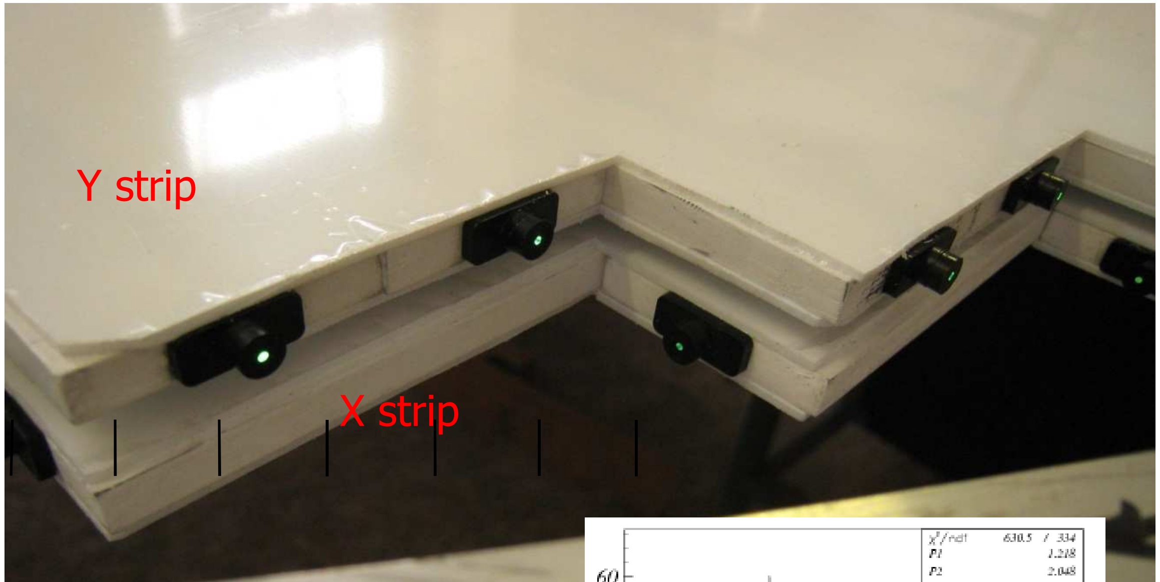
  (max L=280cm, w=25mm)
- » ~16800 read out channels
- » Geometrical acceptance > 99%

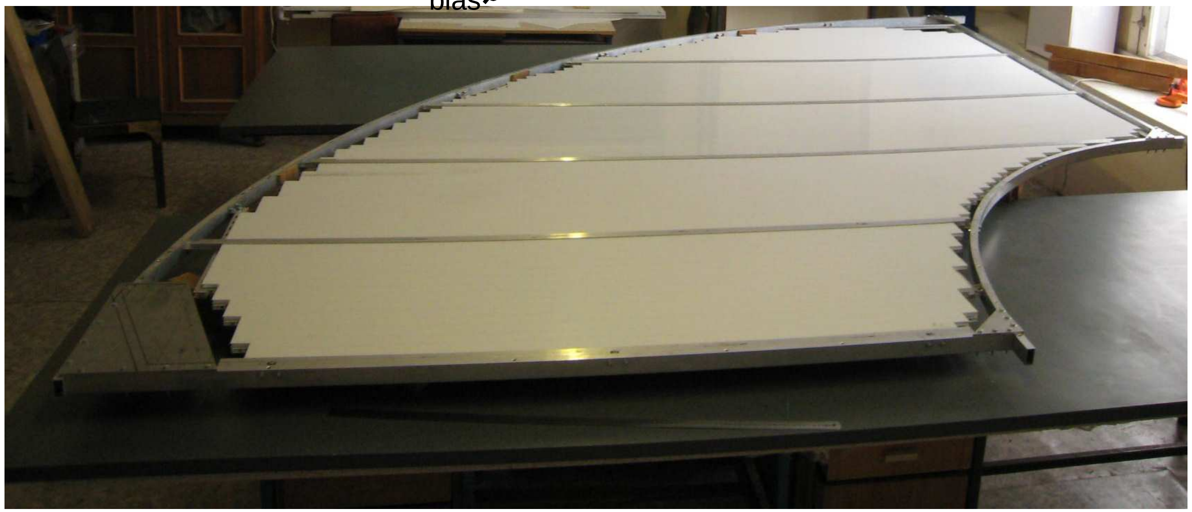


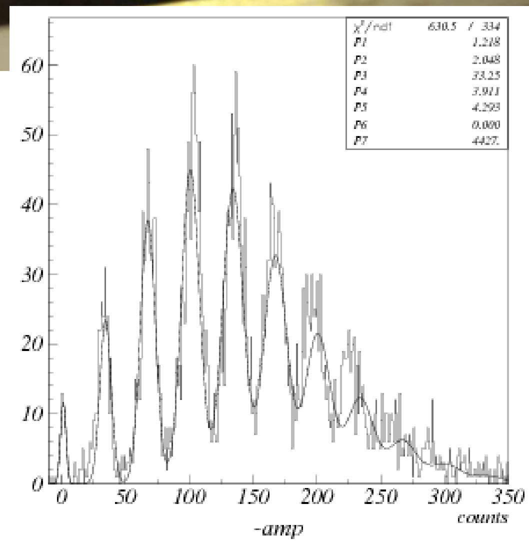


Endcap KLM upgrade





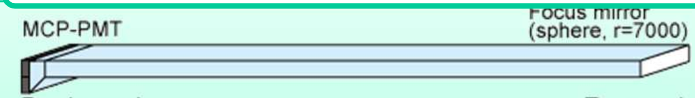




Single p.e. resolution with TARGET WFS ASIC readout

Particle Identification

Barrel PID: Time of Propagation Counter (TOP)

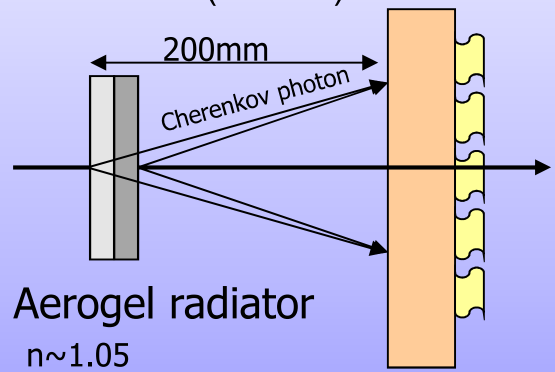


Quartz radiator

Focusing mirror

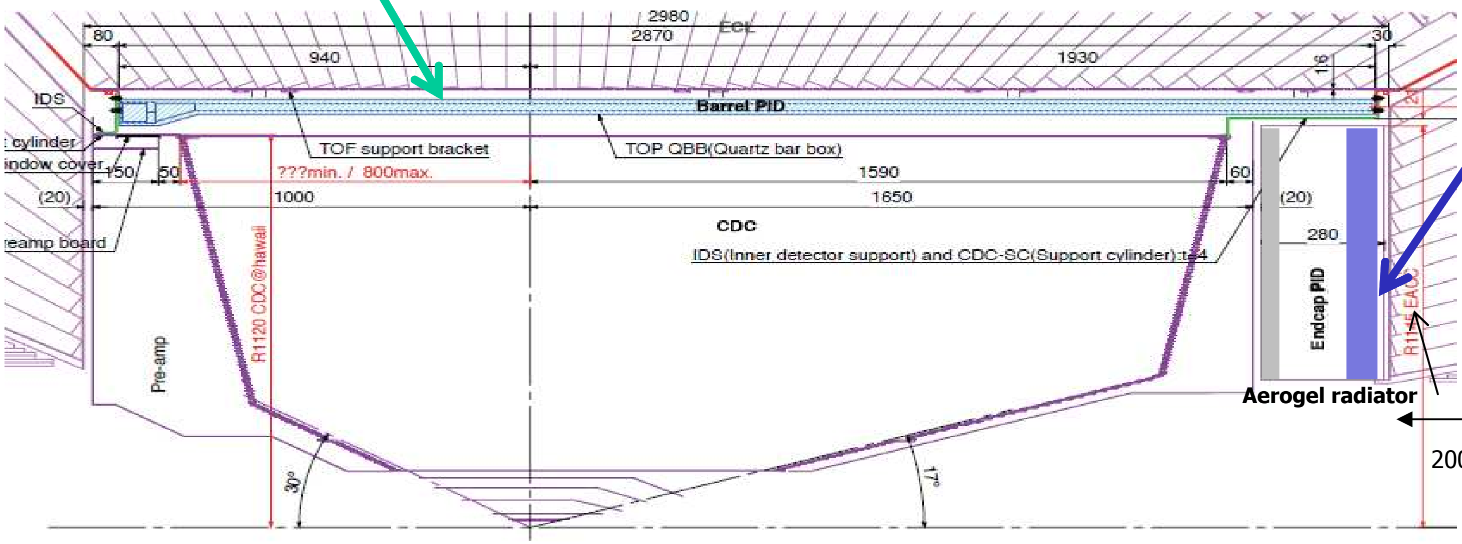
Small expansion block
Hamamatsu MCP-PMT (measure t, x and y)

Endcap PID: Aerogel RICH (ARICH)



Aerogel radiator
n~1.05

Hamamatsu HAPD
+ new ASIC



Hamamatsu HAPD + readout

200

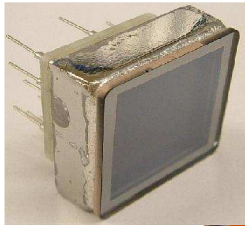
TOP (Barrel PID)

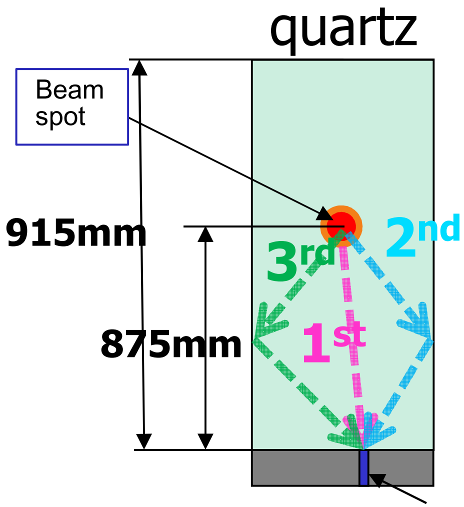
» Quartz radiator
  - 2.6m^L x 45cm^W x 2cm^T
  - Excellent surface accuracy

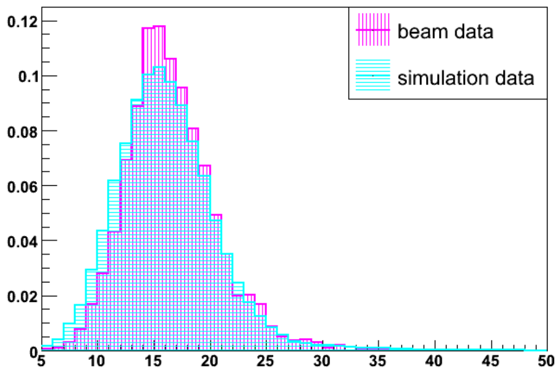
» MCP-PMT
  - Hamamatsu 16ch MCP-PMT
    - Good TTS (<35ps) & lifetime
    - Multialkali photo-cathode → SBA

» Beam test in 2009
  - # of photons consistent
  - Good time resolution

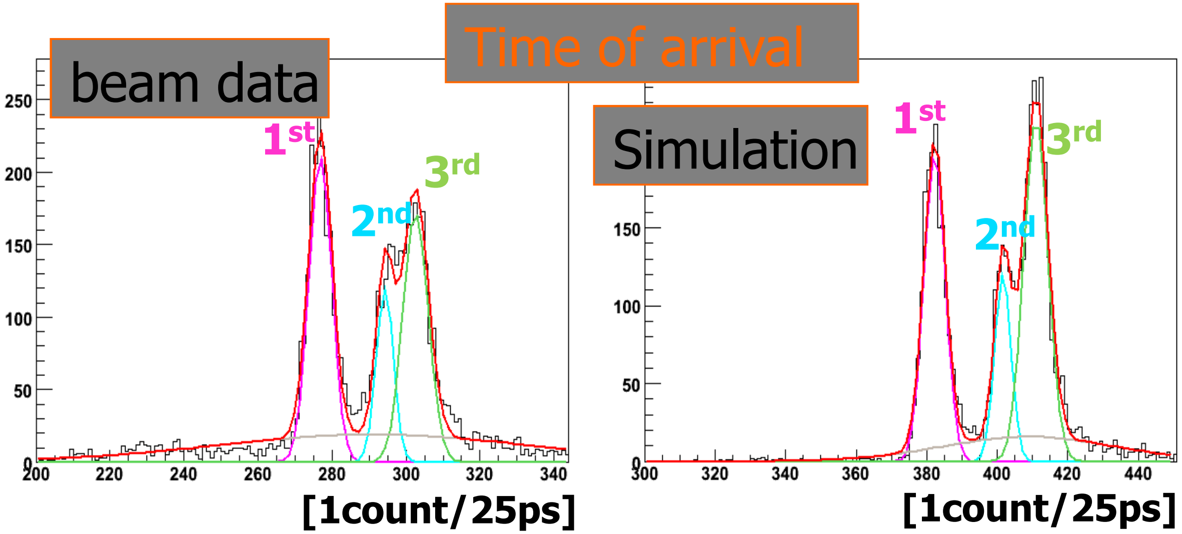
SL10 MCP-PMT





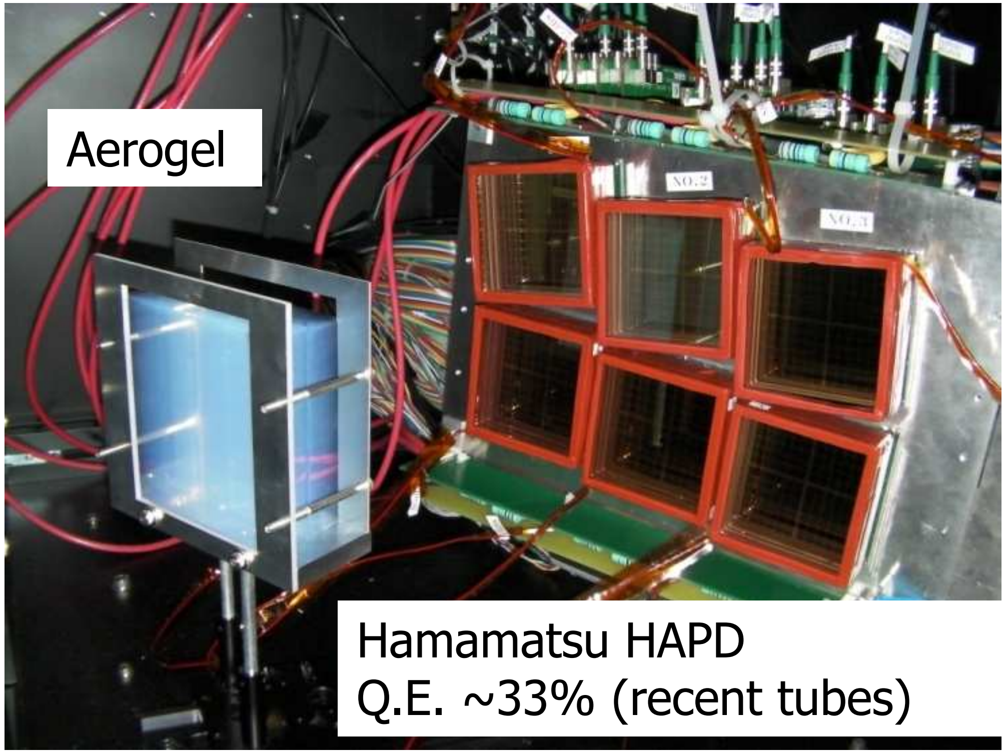


# of photons



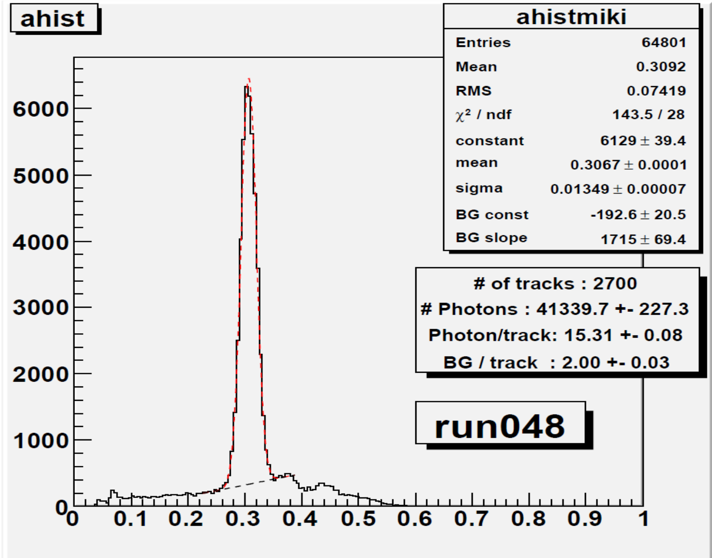
Aerogel RICH (endcap PID)

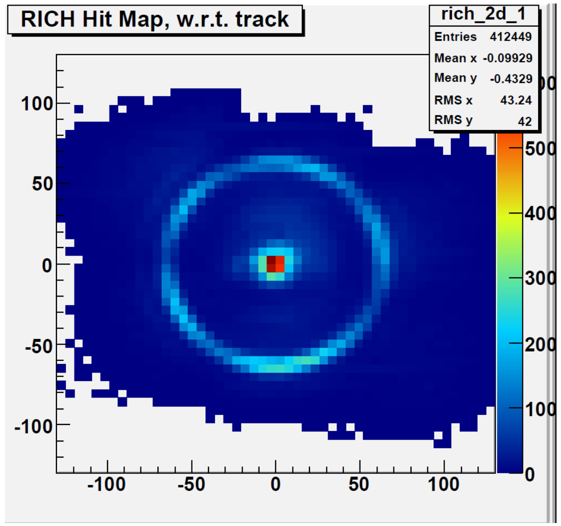
Test Beam setup



6.6 σ p/K at 4GeV/c !

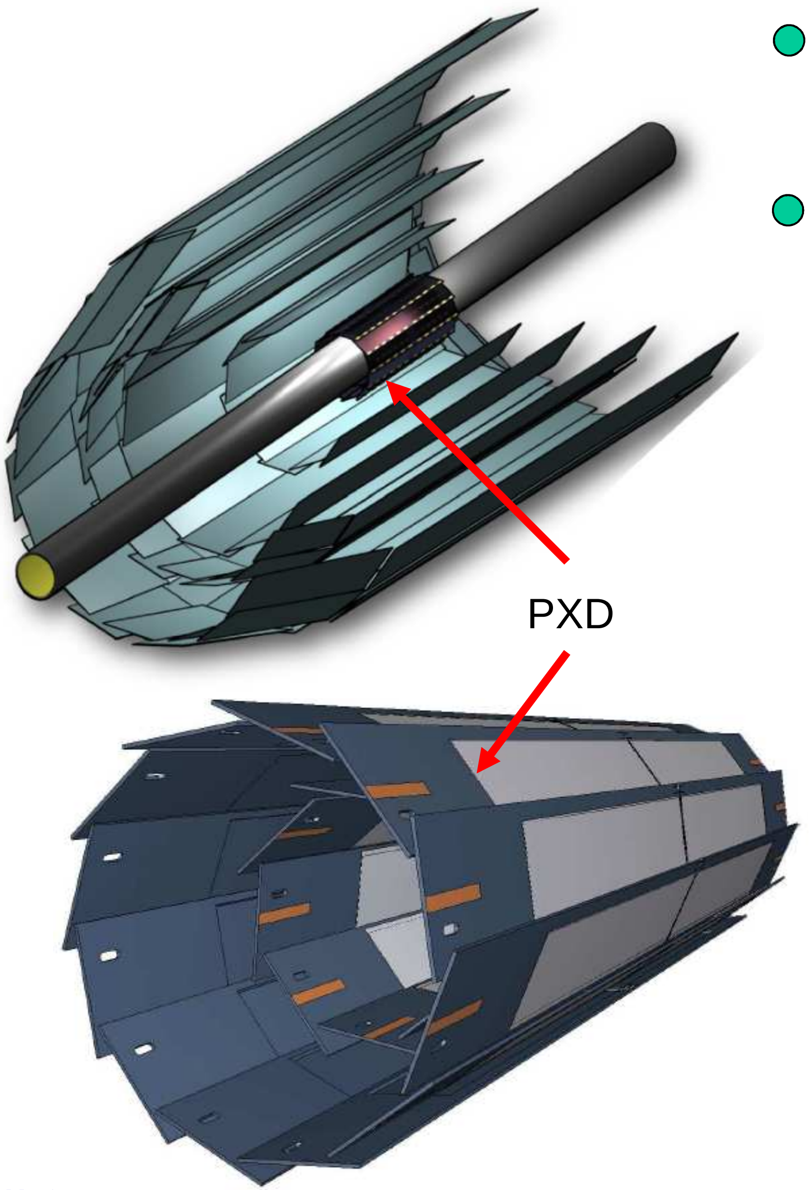
Cherenkov angle distribution





Clear Cherenkov image observed

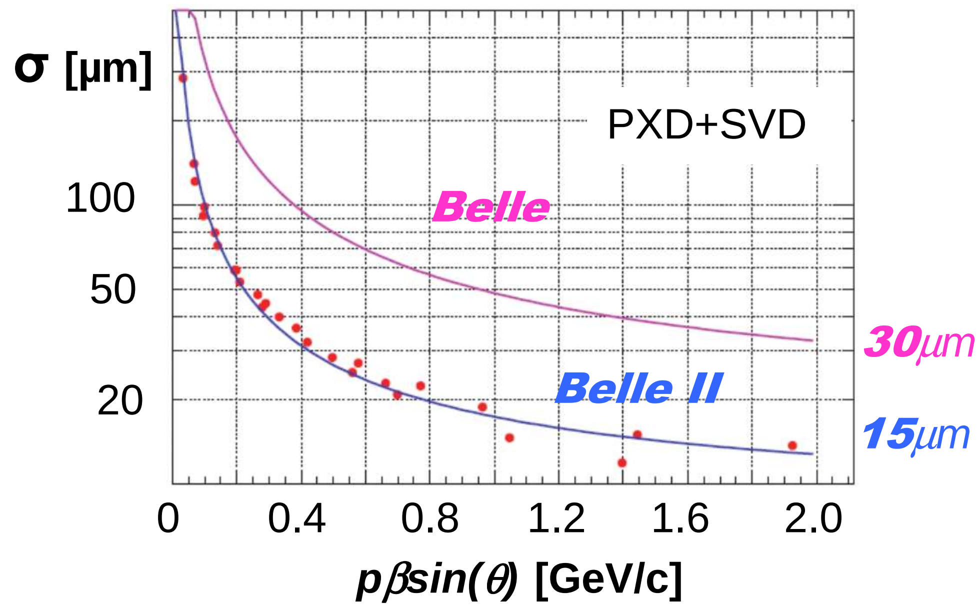
Silicon Tracking System @ Belle II



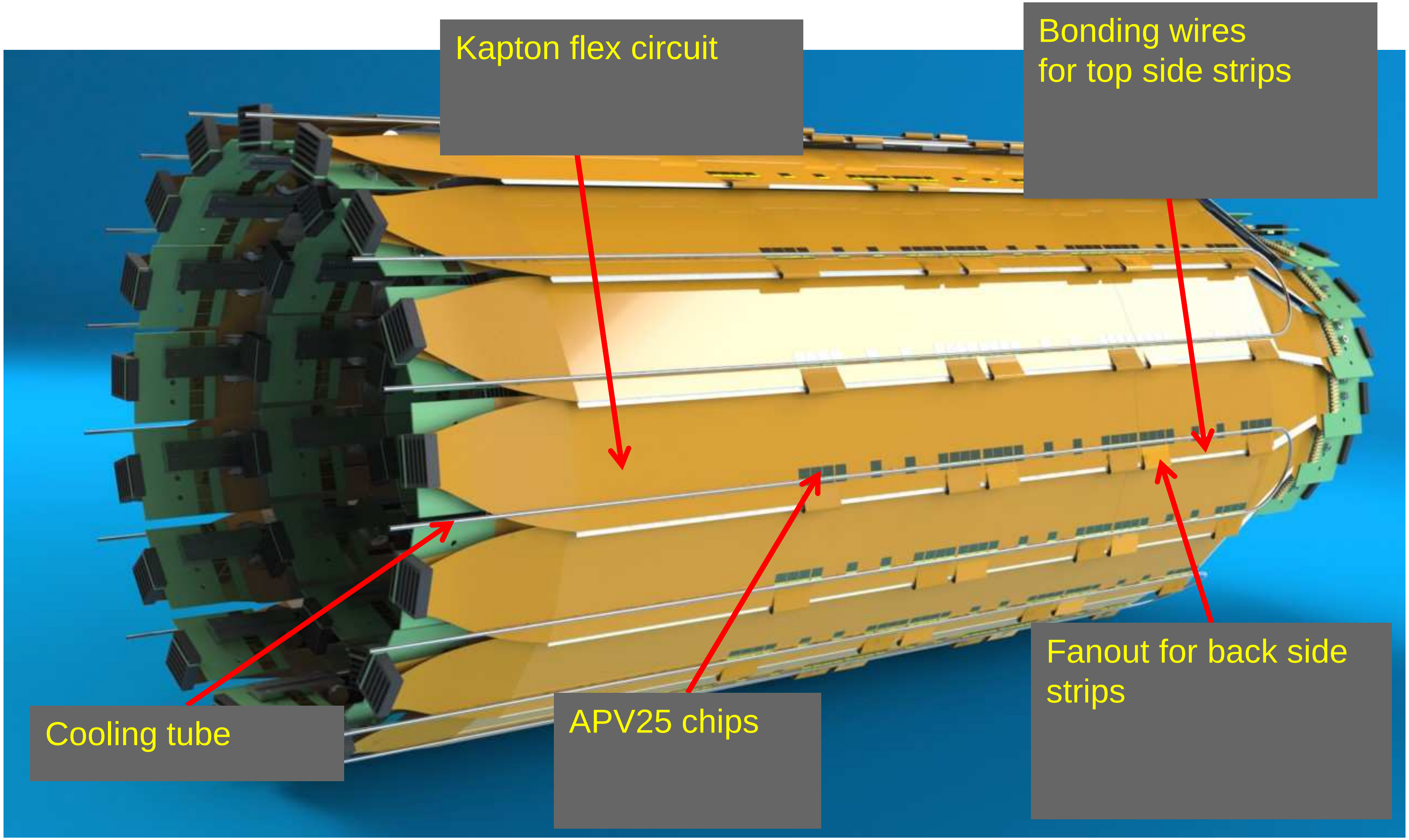
- SVD: 4 layer Si strip detector (DSSD)
  (R = 3.8, 8.0, 11.5, 14.0 cm)

- PXD: 2 layer Si pixel detector (DEPFET technology)
  (R = 1.4, 2.2 cm)
  monolithic sensor
  thickness 75 µm (!),
  pixel size 50 x 55 µm² to 50 x 85µm² (depending on layer and z)

Significant improvement in z-vertex resolution



Silicon Vertex Detector



APV25 readout chip adapted to Belle-II

- Origami PCB
  - 3-layer design
  - 237μm thick (nominal)
- PA0, PA1 and PA2
  - 2-layer design
  - 145μm thick (nominal)

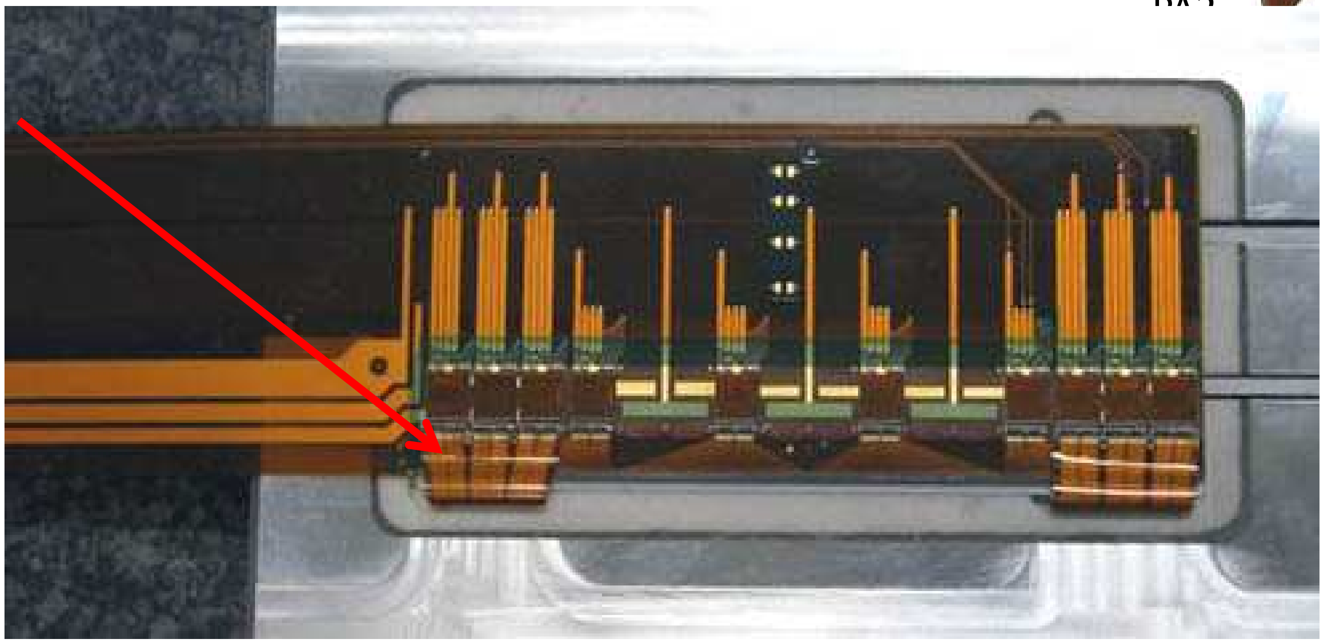
PA1

PA0

glued onto hybrid

Thinned APV25 (300μm→~100μm)

~0.55%X_0/layer



DEPFET

Each pixel is a p-channel FET on a completely depleted bulk

A deep n-implant creates a potential minimum for electrons under the gate ("internal gate")

Signal electrons accumulate in the internal gate and modulate the transistor current (g_q ~ 400 pA/e$^-$)

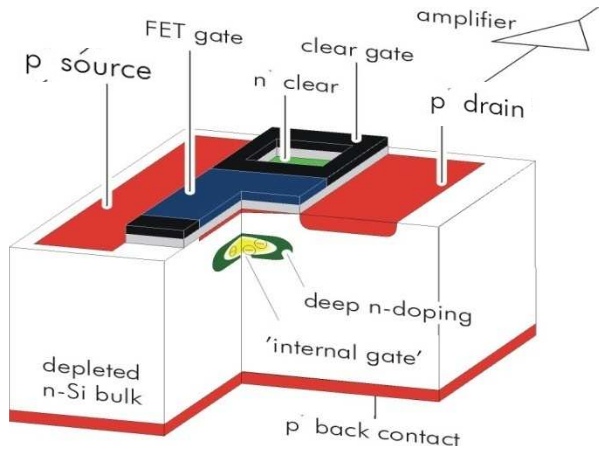
Accumulated charge can be removed by a clear contact ("reset")

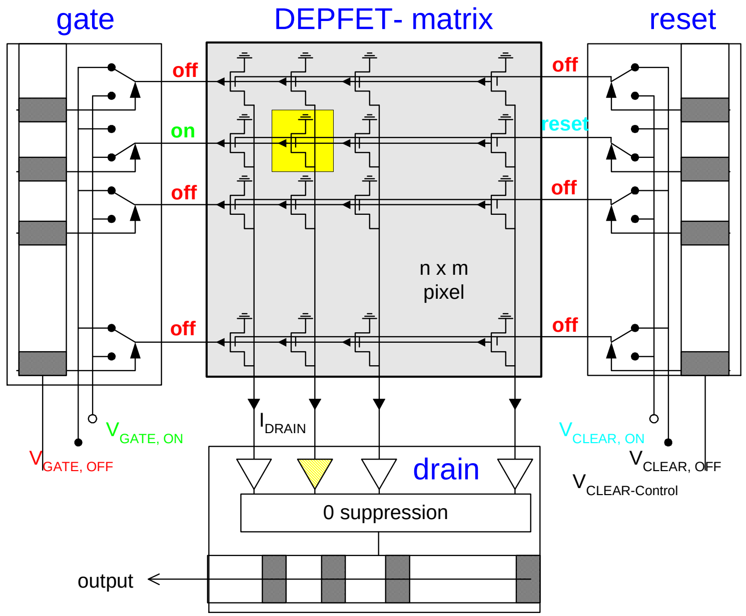
Fully depleted:
⇒large signal, fast signal collection

Low capacitance,
internal amplification: => low noise

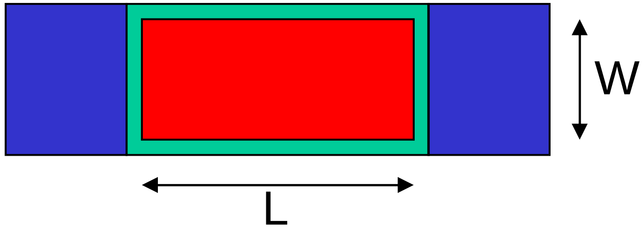
High S/N even for thin sensors

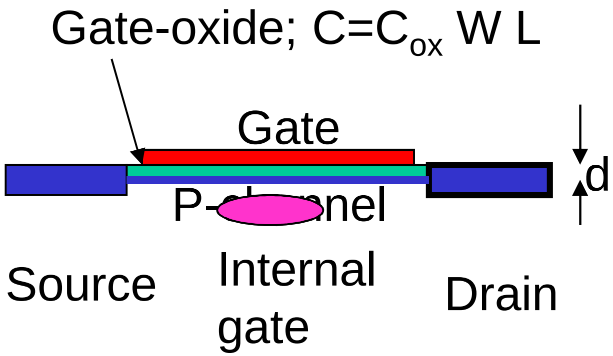
Rolling shutter mode (column parallel) for matrix operation
⇒20 µs frame readout time
=> Low power (only few lines powered),





How does it work?





FET in saturation:

$$I_d = \frac{W}{2L}\mu C_{ox}(V_G - V_{th})^2$$

$$I_d = \frac{W}{2L}\mu C_{ox}\left(V_G + \frac{\alpha q_s}{C_{ox}WL} - V_{th}\right)^2$$

I_d: source-drain current
C_{ox}: sheet capacitance of gate oxide
μ: mobility (p-channel: holes)
V_g: gate voltage
V_{th}: threshold voltage

A charge q in the internal gate influences a mirror charge αq in the channel
(α <1, for stray capacitance)
This mirror charge is equivalent to a change of the gate voltage:

$\Delta V = \alpha q / C = \alpha q / (C_{ox} W L)$

Transconductance:

$$g_m = \frac{dI_d}{dV_G} = \frac{W}{L}\mu C_{ox}(V_G - V_{th})$$

$$g_m = \sqrt{2\frac{W\mu C_{ox} I_d}{L}}$$

Conversion factor:

$$g_q = \frac{dI_d}{dq_s} = \alpha\frac{W}{L^2}\mu\left(V_G + \frac{\alpha q_s}{C_{ox}WL} - V_{th}\right) = \alpha\sqrt{2\frac{I_d\mu}{L^3 W C_{ox}}}$$

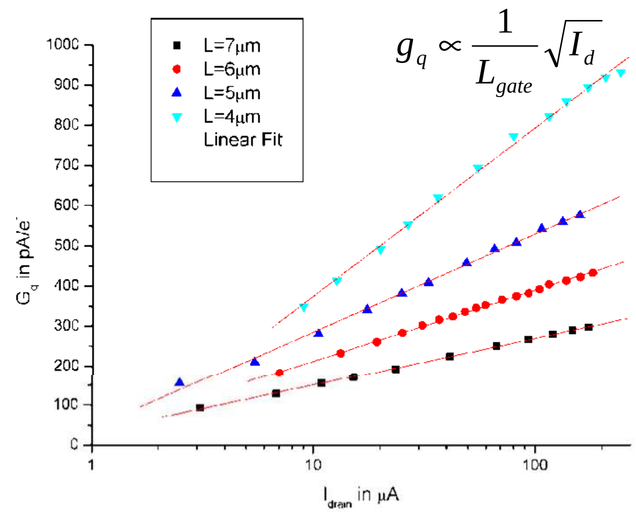
$$g_q = \alpha\frac{g_m}{WLC_{ox}} = \alpha\frac{g_m}{C}$$

Gain and Noise

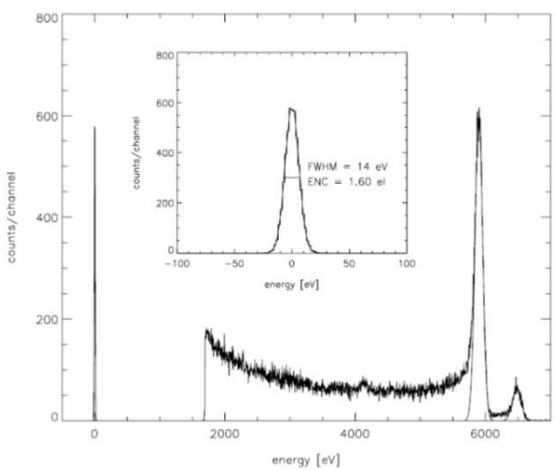
Measurements in good agreement
Typical values:

g_q ~ 400 pA/e (for L = 6 µm)

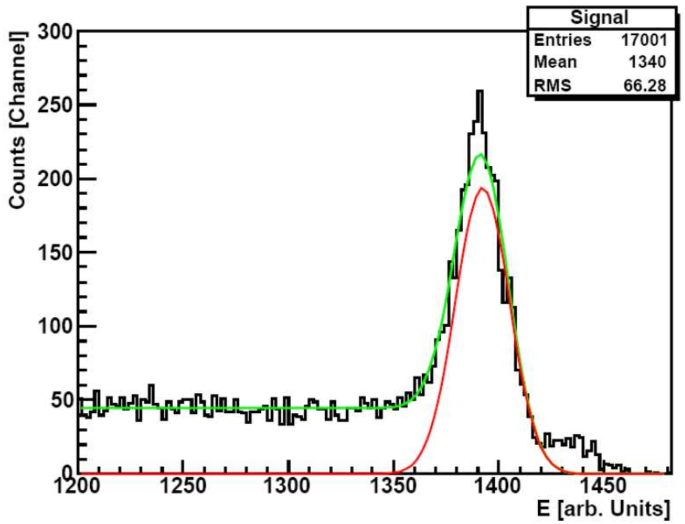
Could be pushed up to 1 nA/e



$$ENC = \sqrt{\alpha \frac{8kT g_m}{3 g_q^2}\frac{1}{\tau} + 2\pi a_f C_{tot}^2 + qI_{Leak}\tau}$$



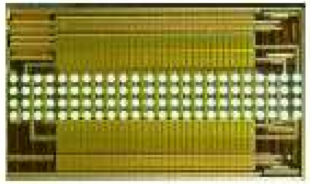
1.6 e ENC at τ=10 µs



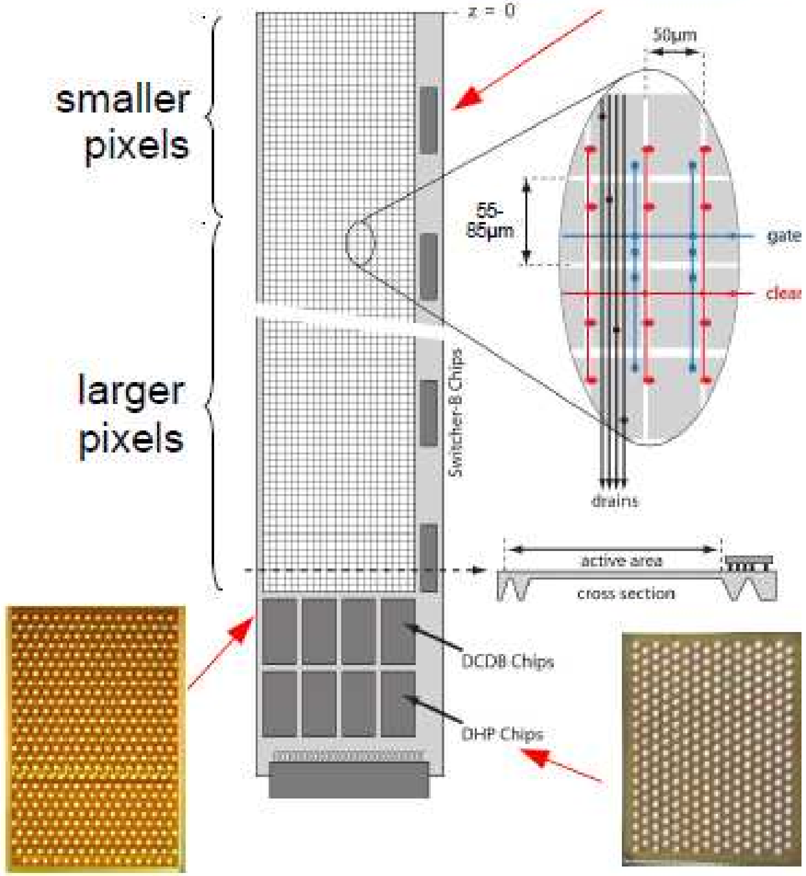
40 e ENC at τ=20ns (50MHz)

Sensor Module/Ladder

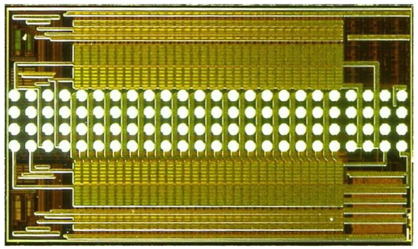
- PXD ladder is built of two half modules
  - module length restricted by wafer size
  - yield considerations

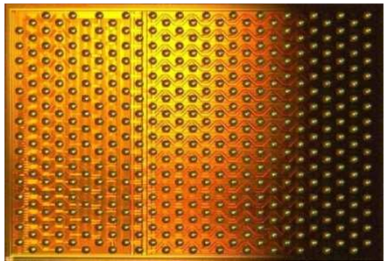


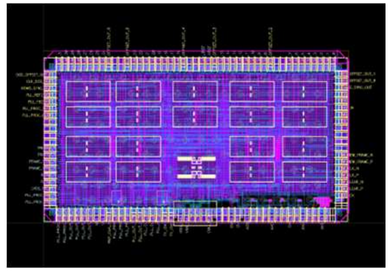
Half Module	Inner layer	Outer layer
# (half) modules	8 (16)	12 (24)
Radius	14 mm	22 mm
Pixel size	50x55 μm² 50x60 μm²	50x70 μm² 50x85 μm²
Thick ness	75 μm	75 μm
# pixels	1536(z) x 250(R-ϕ)	1536(z) x 250(R-ϕ)
Size	15x68 mm²	15x85 mm²



ASICs for control and readout







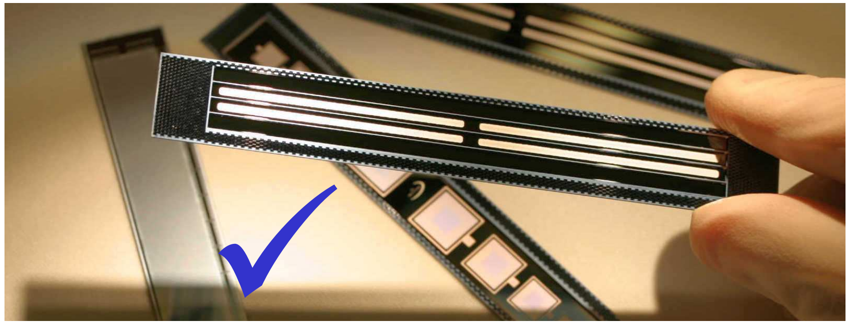
Switcher
Control of gate and clear
32 x 2 channels
Switches up to 30V
AMS 0.18 µm HV technology
Tested up to 36 Mrad

DCDB
Amplification and digitization of DEPFET signals
256 input channels
8-bit ADC per channel
92 ns sampling time
UMC 189nm
Rad hard design

DHP
Signal processor
Common mode correction
Pedestal subtraction
0-supression
Timing and trigger control
IBM 90 nm
Rad hard design
Convert to TSMC 65nm

All three chips fabricated and tested

Sensor Thinning



Need thin (50µm-75µm) self supporting all silicon module

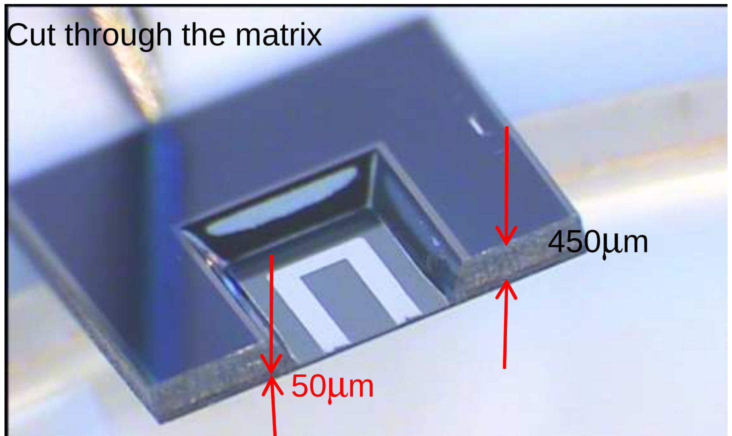
Process backside e.g. structured implant

Wafer bonding SOI process

Thinning of top wafer (CMP)

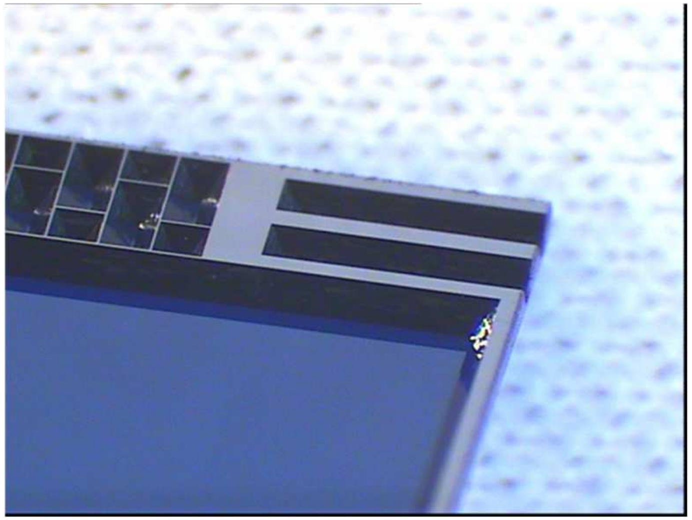
Processing

etching of handle wafer (structured)

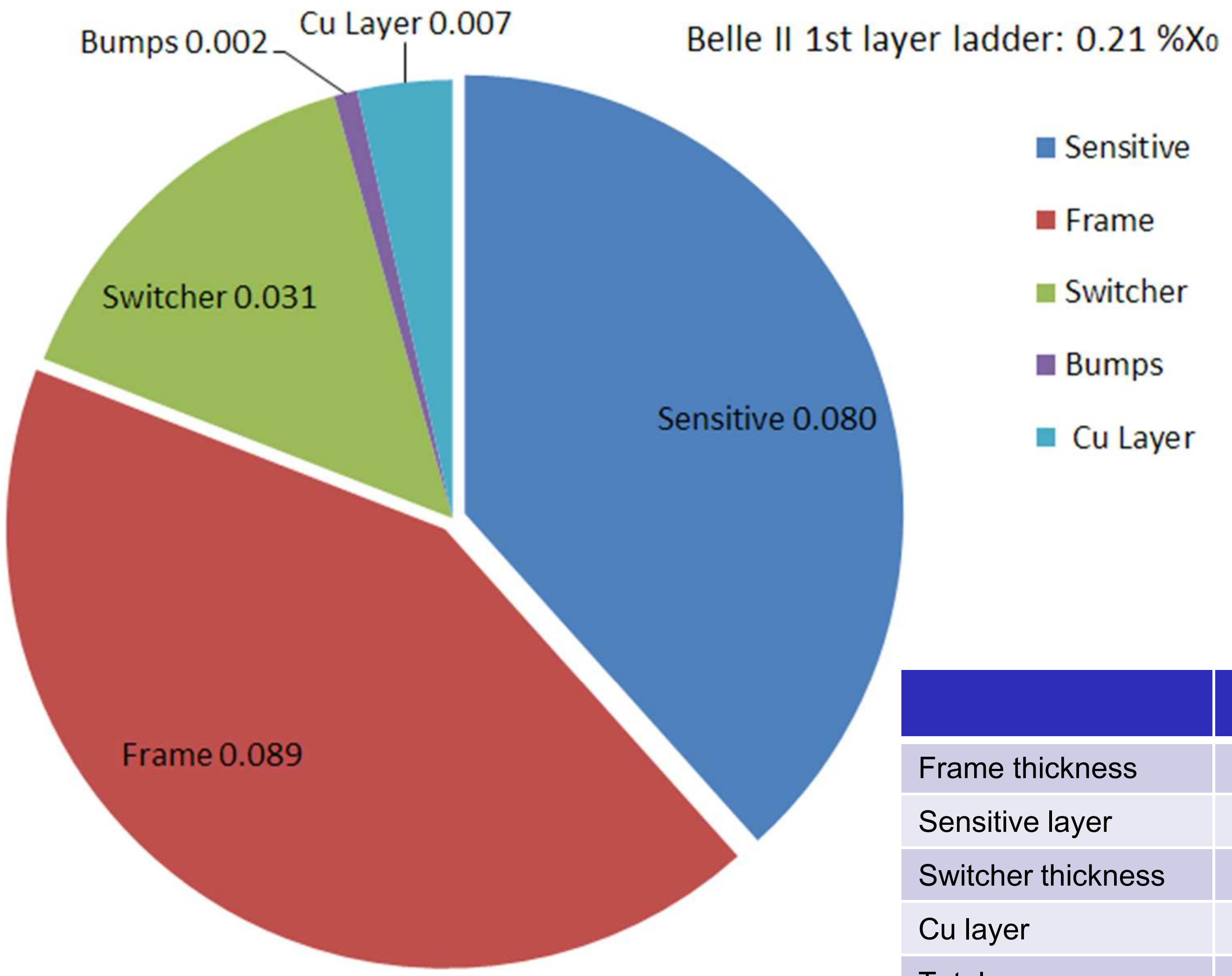


µ-joint between half-ladders

- v-grooves in support silicon
- butt-joint between two half-ladders
- reinforced with 3 ceramic inserts
- 2x300µm dead area per ladder
- mechanical tests → remarkably robust!!
- bowing: up to 1 mm sag (over 10 cm)
- tension: 40 to 60 N, then the Si broke



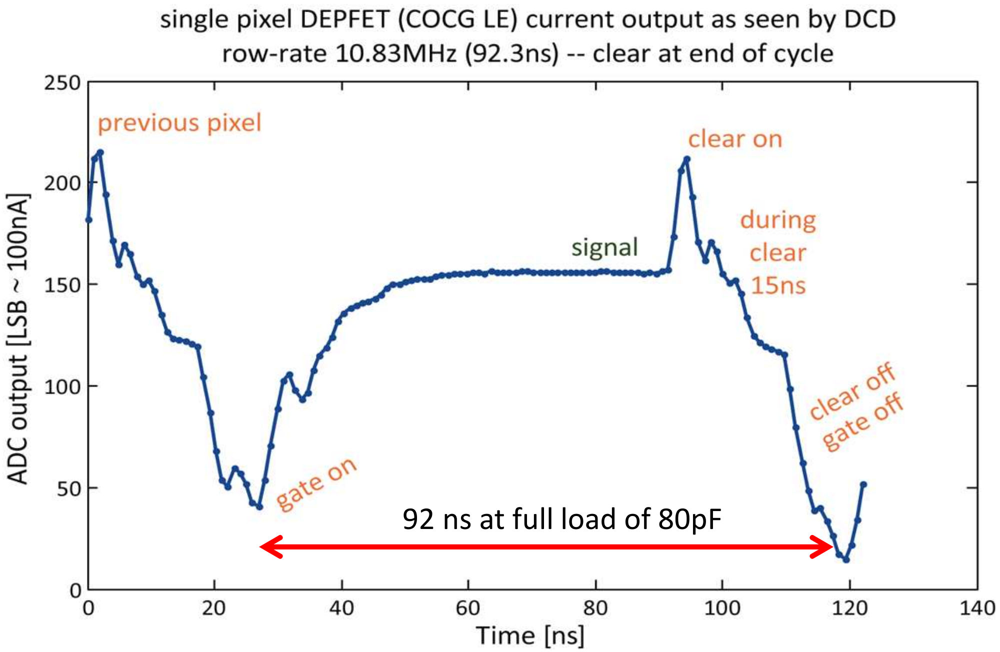
All-silicon module – material budget (single layer)

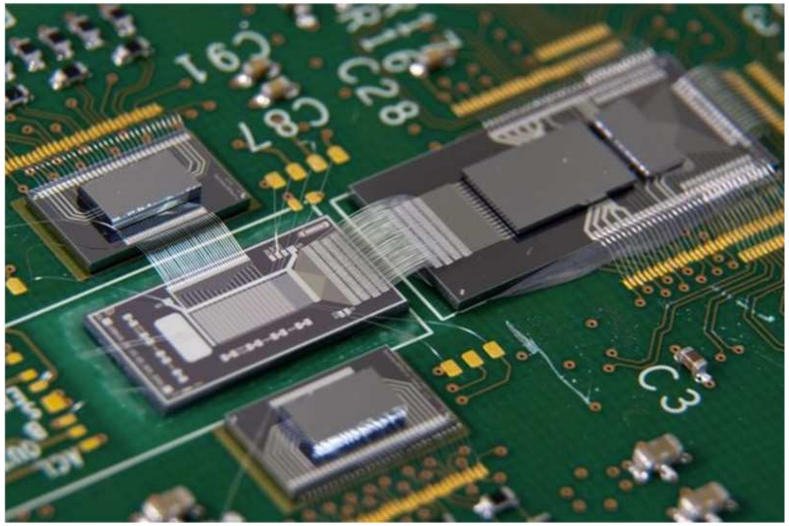


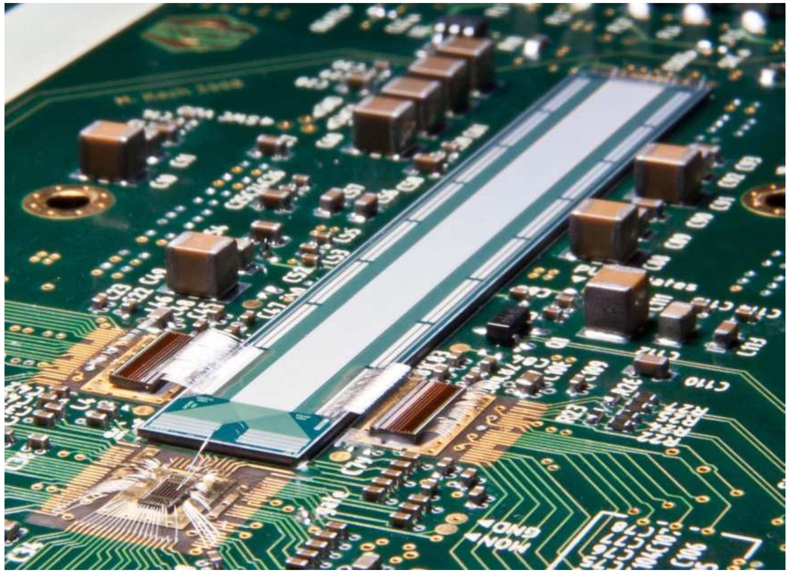
	Belle II
Frame thickness	525 µm
Sensitive layer	75 µm
Switcher thickness	500µm
Cu layer	only on periphery
Total	0.21 %X0

PXD6 testing in the lab

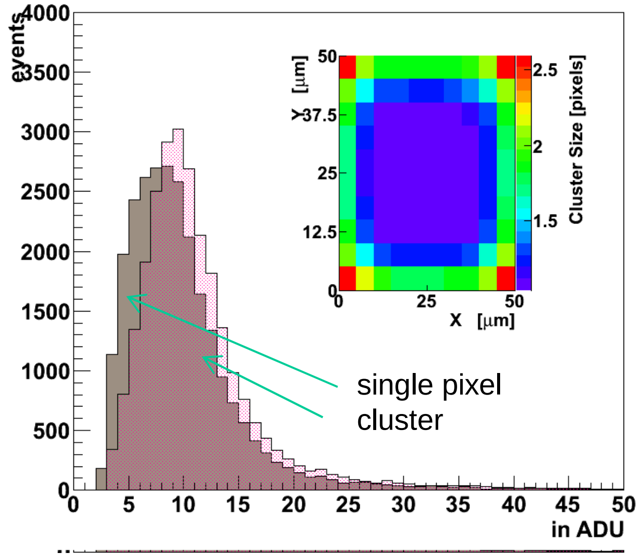
- bench tests in the lab
  - ↳ determine best operating point (Clear, ClearGate, Drift..)
  - ↳ in-pixel studies with laser
  - ↳ radioactive source tests
  - ↳ **read-out speed…**
- goal @Belle II
  - 320 MHz system clock
  - 50 kHz frame rate (20µs r/o time per frame)
  - 768 rows, 4-fold r/o → **~100 ns per row**

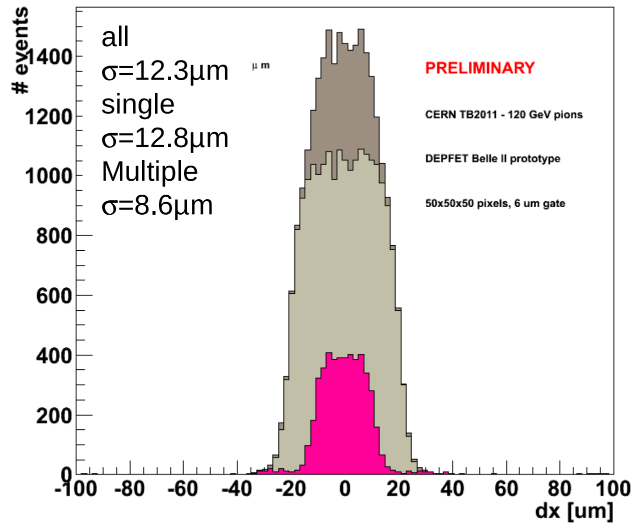






Test Beam





Test beam at CERN, October 2011

a) PXD6, 50µm, L=4µm, standard ox: S/N ~ 40
b) PXD6, 50µm, L=6µm, thin ox: S/N ~ 20

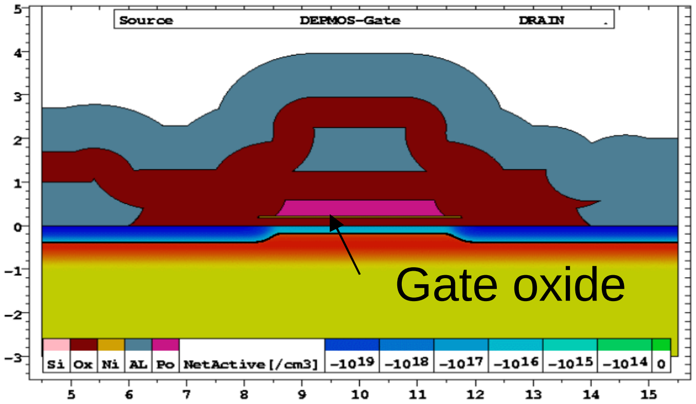
thin oxide not yet optimized => smaller S/N
DCD V1 does not allow optimal Idrain
final sensors are 50% thicker

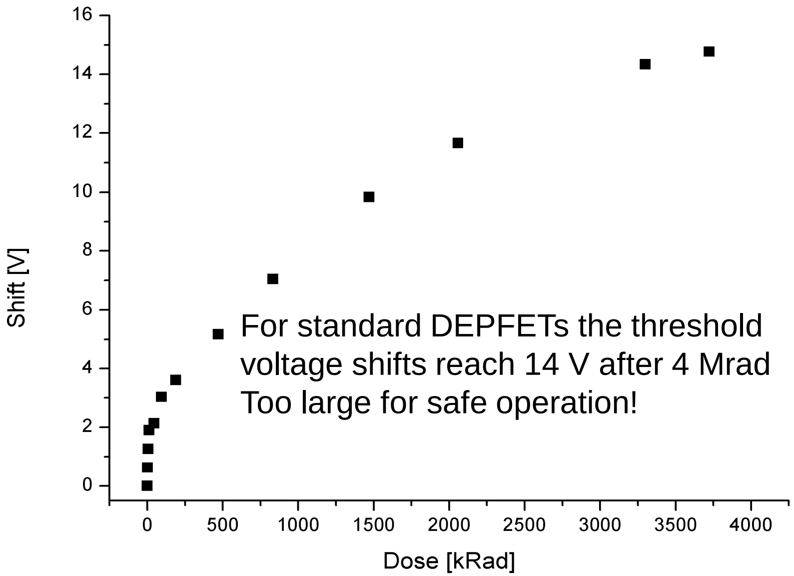
=> S/N > 40 expected for optimal settings

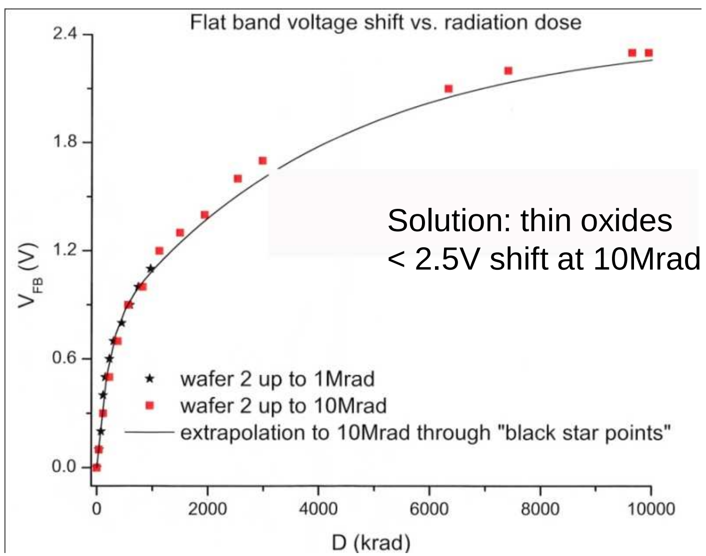
Readout speed up to 320 MHz (100ns readout time)

Radiation Hardness

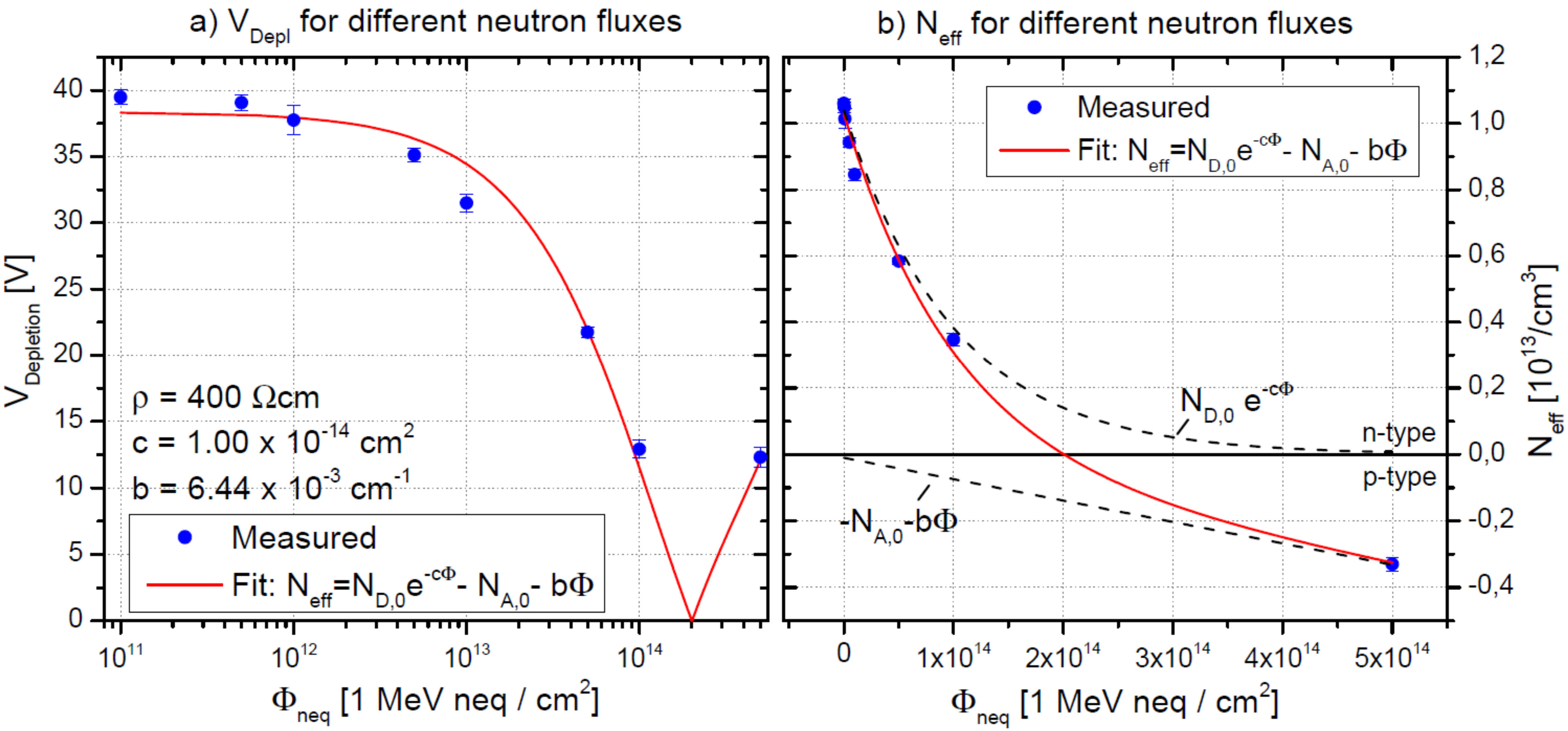
DEPFET based on a MOS structure
problem with ionising radiation:
Creation of fixed (positive) charges in the oxide layer and at the interface
Attracts electrons at the Si/SiO_2 interface
Need more negative gate voltages to compensate
=> Shift of transistor threshold







Neutron irradiations

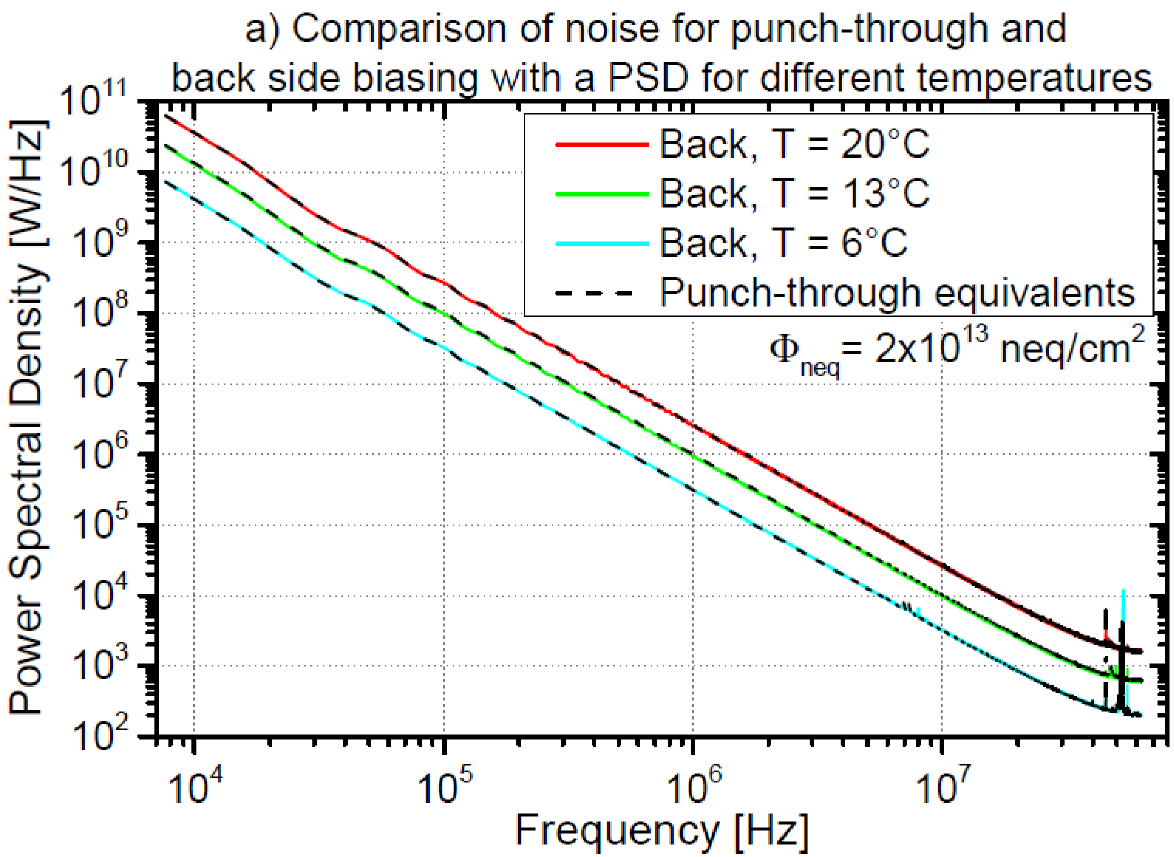


- Type Inversion at an equivalent neutron flux of approximately $2x10^{14}$ neq/cm^2
→ No Type Inversion expected during BELLE II operations

- Measured leakage current after a neutron flux of $2x10^{14}$ neq/cm^2 was roughly $6x10^{-4}$ A/cm^3

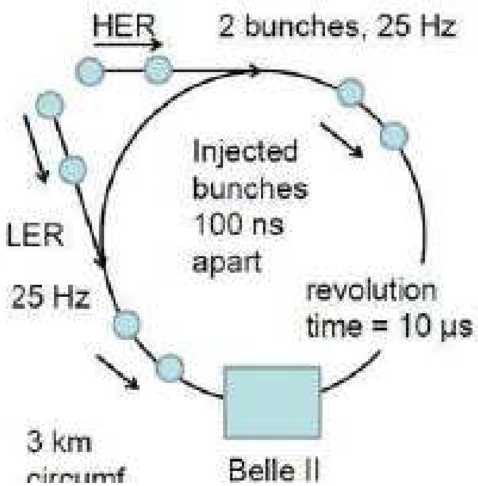
Punch Through Bias

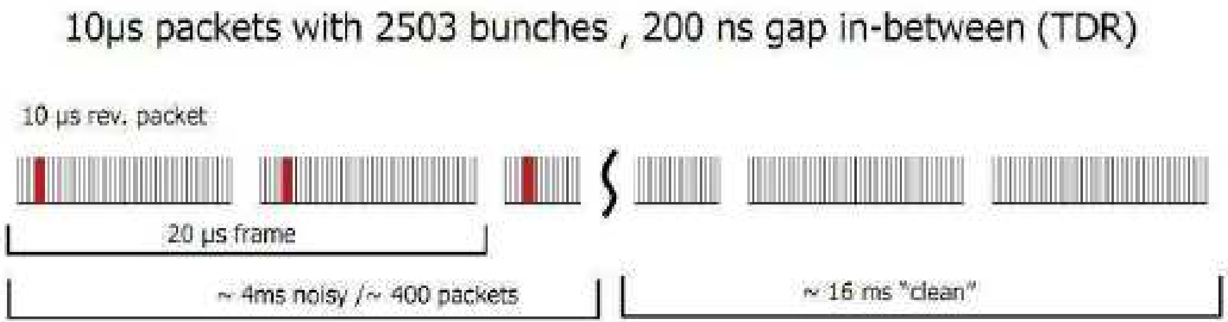
Punch through mechanism allows to bias the backside from a contact on the front side.
No electrical connections on backside needed
However, CDF observed excess noise in punch through biased strip detectors



- Punch-through biasing mechanism still in tact after high neutron fluxes
- No increase of punch-through noise after irradiation up to $1x10^{14}$ neq/cm^2 detectable (measured through various methods)

Injection Noise & Gating





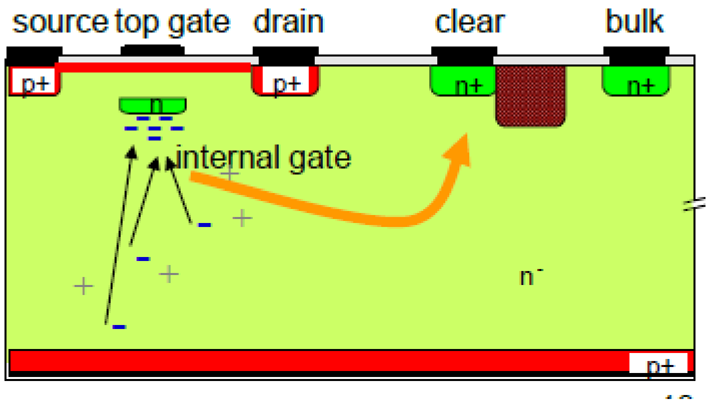
Sensor filled with hits from freshly injected bunches => ~ 20% dead time

Gating : Sensor is made blind for a short time during high background (noisy bunch)
Signals detected in the clean period before are preserved

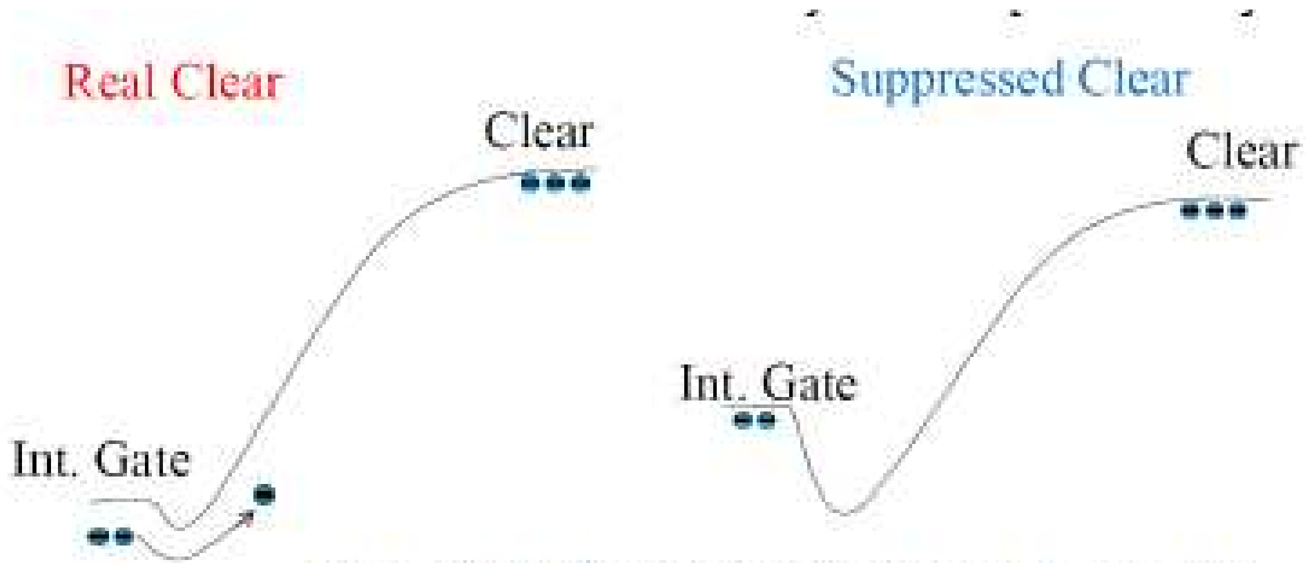
Simulations, lab tests with lasers and particle beams demonstrate feasibility of gating

Gated Operation

In normal clear operation the gate is pulsed negatively (repells electrons)
The clear is pulsed positively (attracts electrons from internal gate and bulk underneath)



In gated mode the gate is not pulsed,
Remains attractive for electrons
The clear is pulsed positively,
Attracte electrons fro, bulk underneath



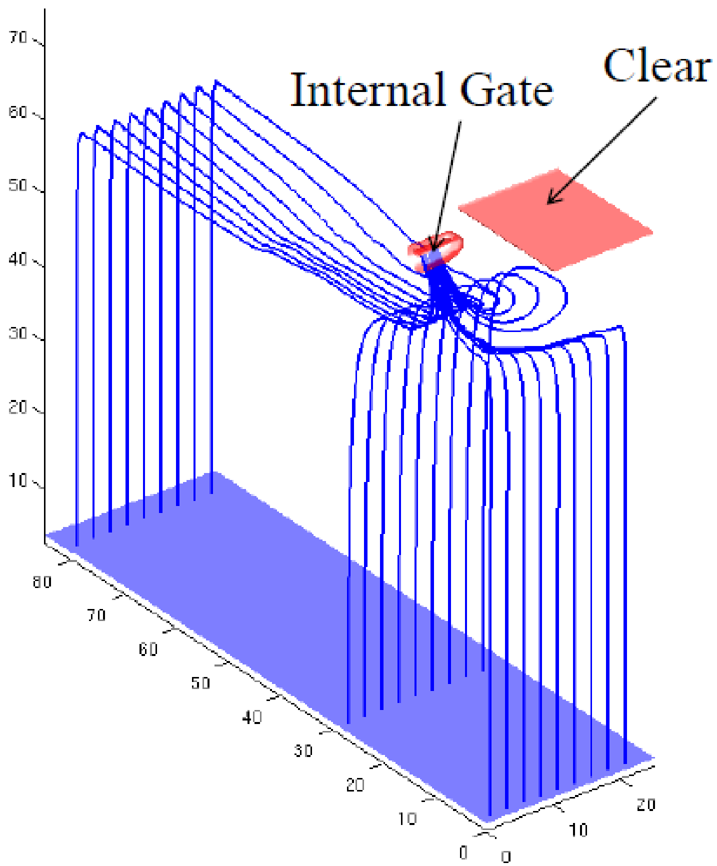
Selectivity of the Clear Process [R. Richter]

Electron drift directions

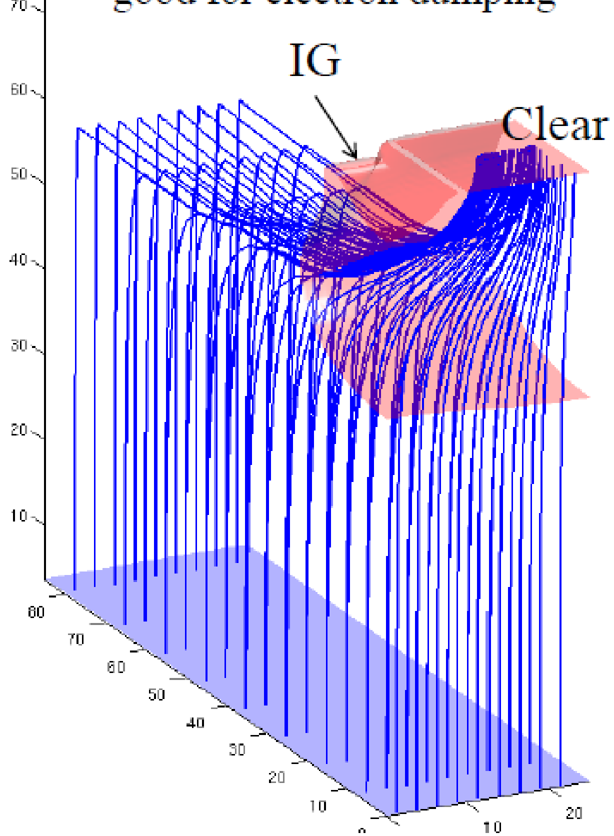
Normal operation:
Signal charge drifts into internal gate

Gated Mode
Charges from background drift directly to clear gate

Signal already stored in internal gate is protected



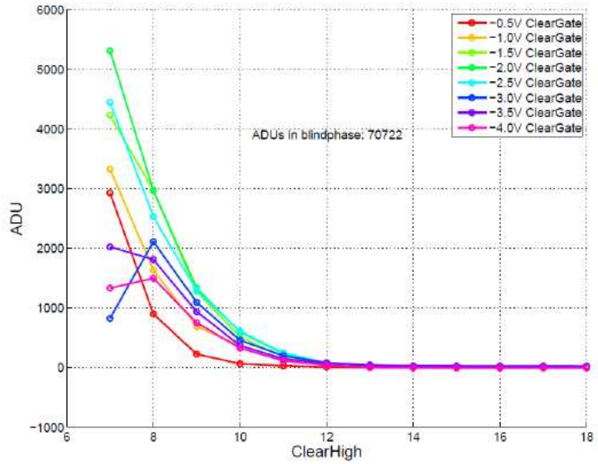
Huge clear region compared to Internal Gate
- good for electron dumping

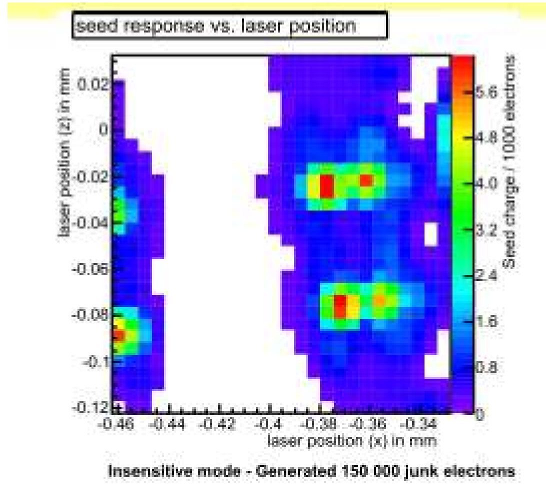


Lab test with laser

Inject (using a laser) 180k electrons
(MIP: 6k electrons)

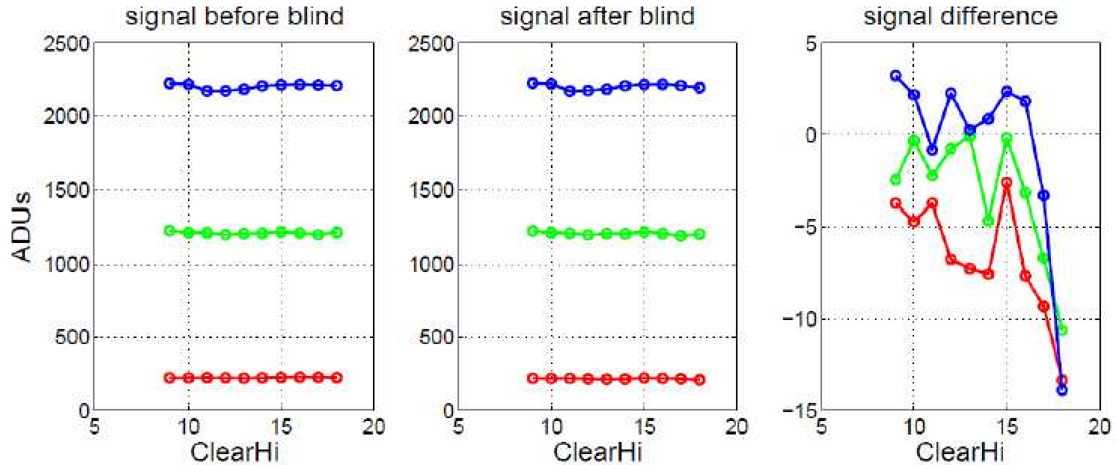
scan clear voltage
=> 12V needed for complete shield





Test storage capacity during gating
Measure injected signal before and after gate

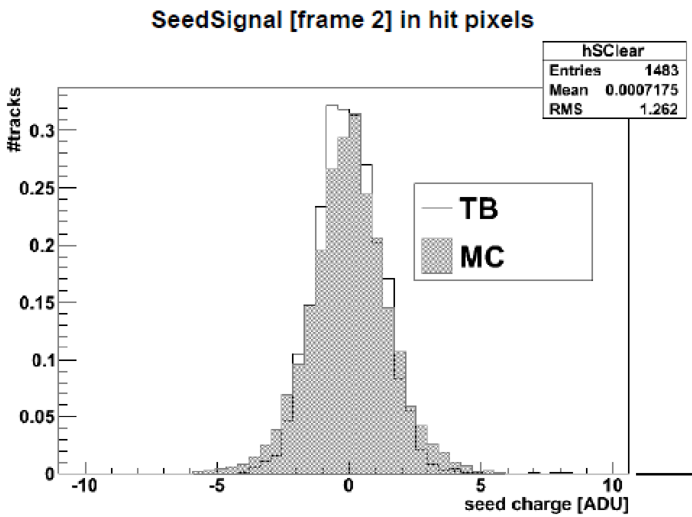
=> No losses up to 14V clear voltage



- three different amounts of electrons have been created (red, green, blue curve)
- shielding of the internal gate works for all studied ClearHi voltages

Tests with beam

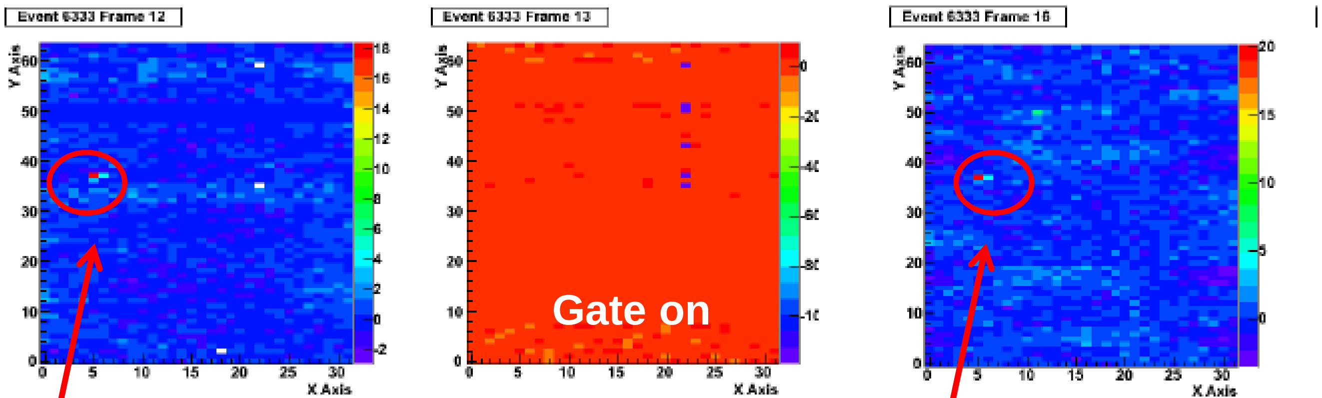
Gated mode successfully tested in the lab (laser) and test beam



TB: Signal distribution of pixels which have been hit by a track when gating was on (from track extrapolation)
MC: normal noise distribution

A real signal should be here

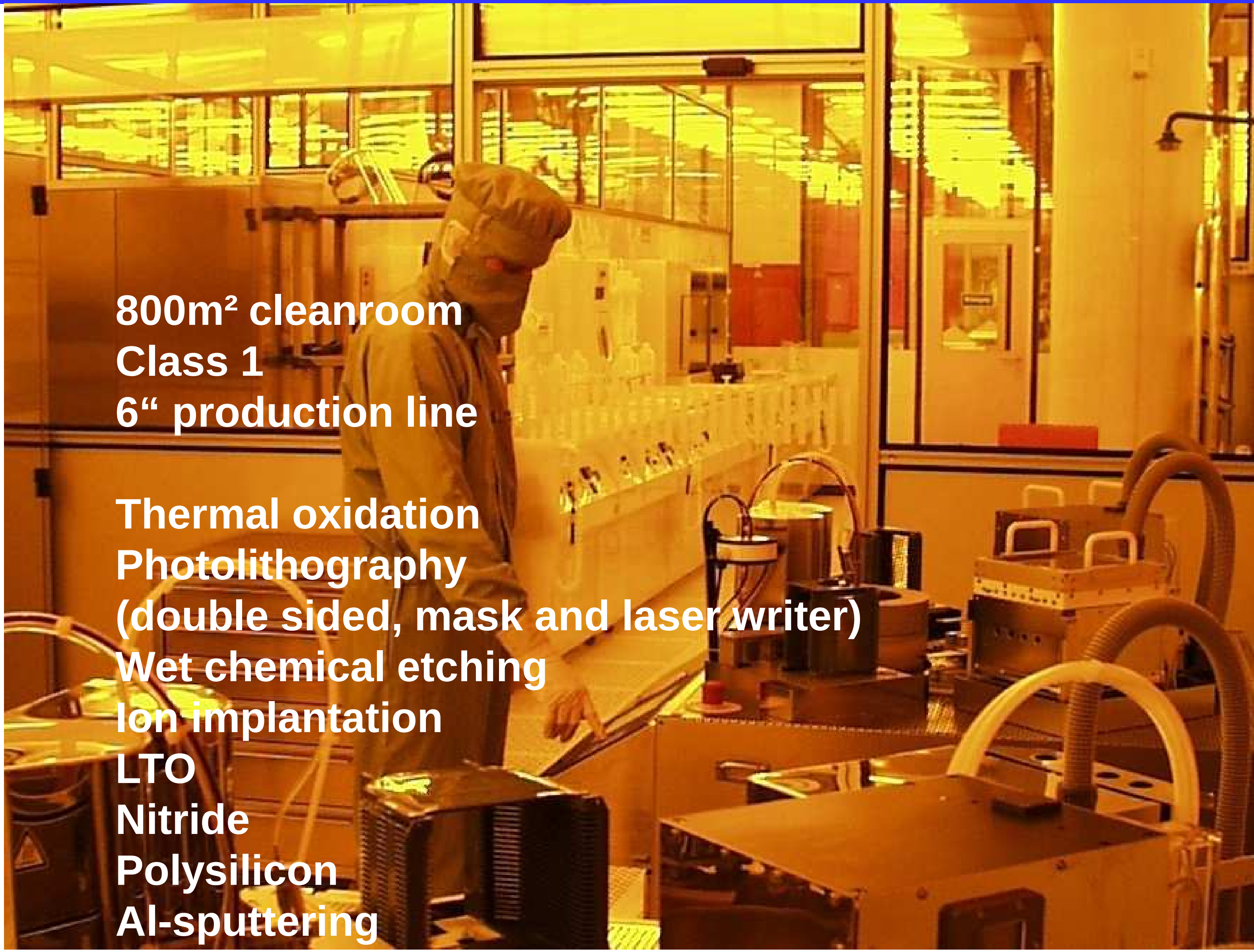
Protection: the signal of a real hit is still present after gating:



Signal before gate (not cleared)

Signal after gate

Production Facilities

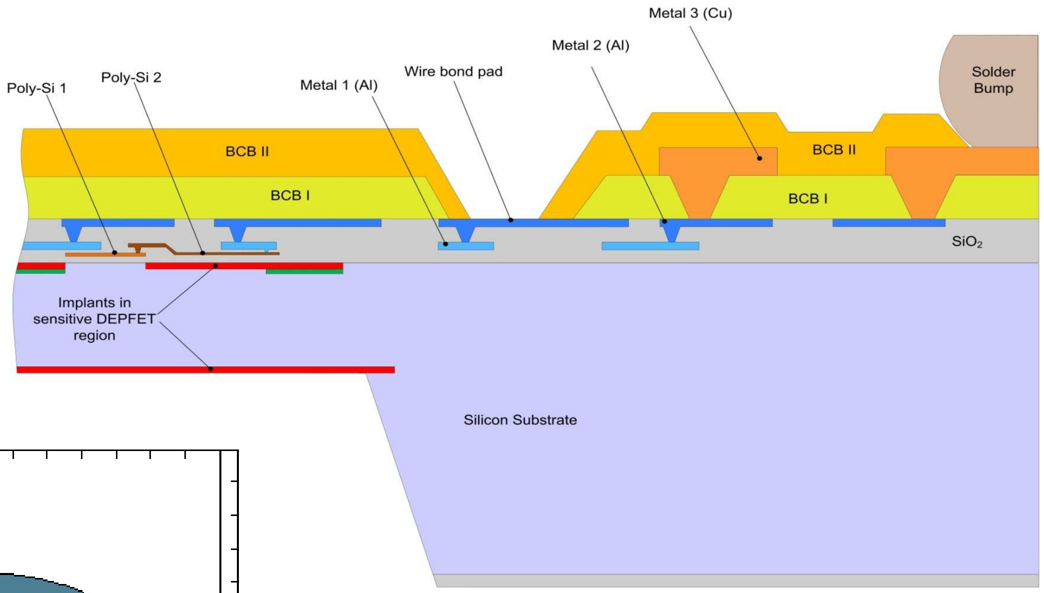


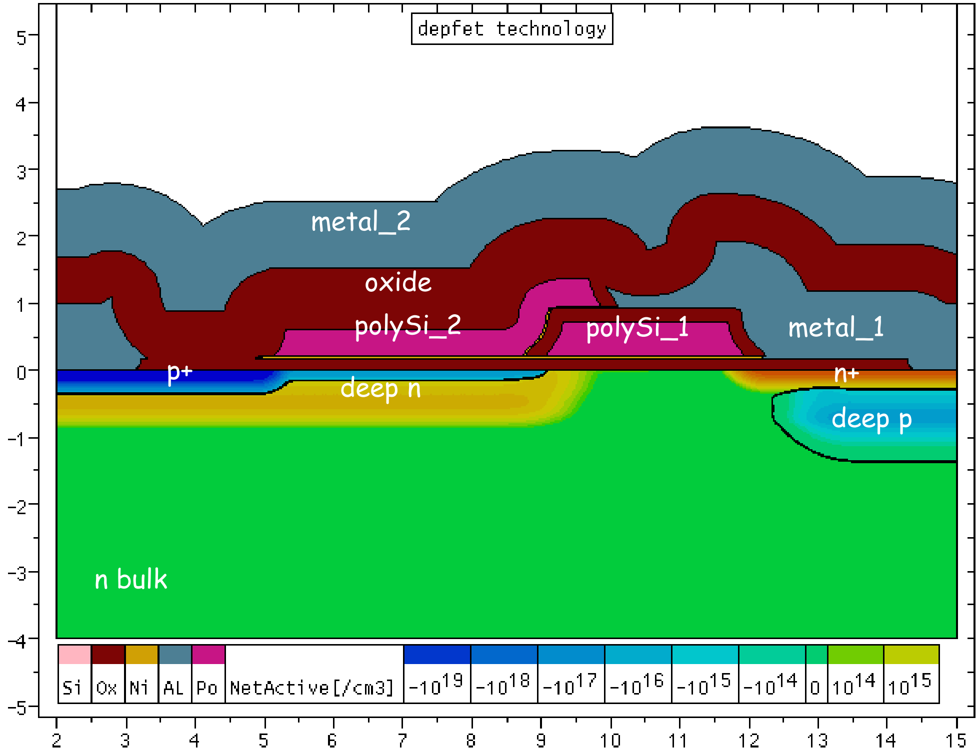
800m² cleanroom
Class 1
6“ production line

Thermal oxidation
Photolithography
(double sided, mask and laser writer)
Wet chemical etching
Ion implantation
LTO
Nitride
Polysilicon
Al-sputtering

DEPFET production

BCB passivation
Copper layer (power and UBM)
BCB insulation





Poly I (transistor gate)
Poly II (clear gate, contact)
Alu I (contacts)
Alu II (contacts)

In total: 93 processing steps
~ 2 years processing time

DEPFET Production

.

First production batch with 13 wafers started in HLL in July

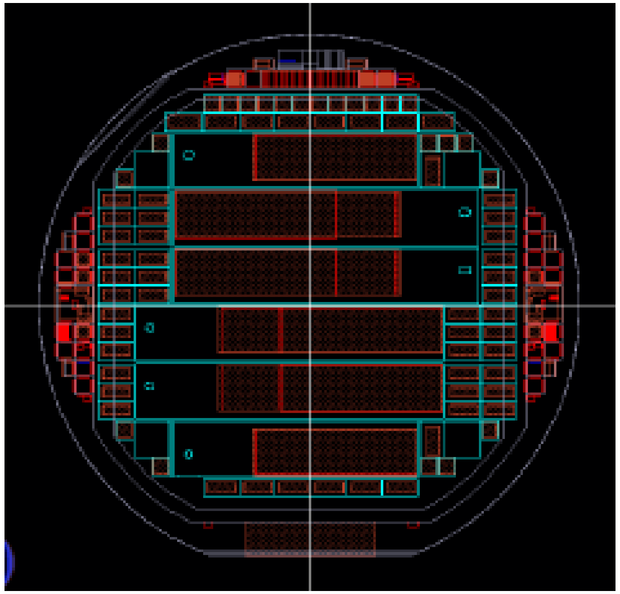
•one wafer has sensors for 1 inner and 2 outer ladders

Nominal processing time (including thinning): 2 years

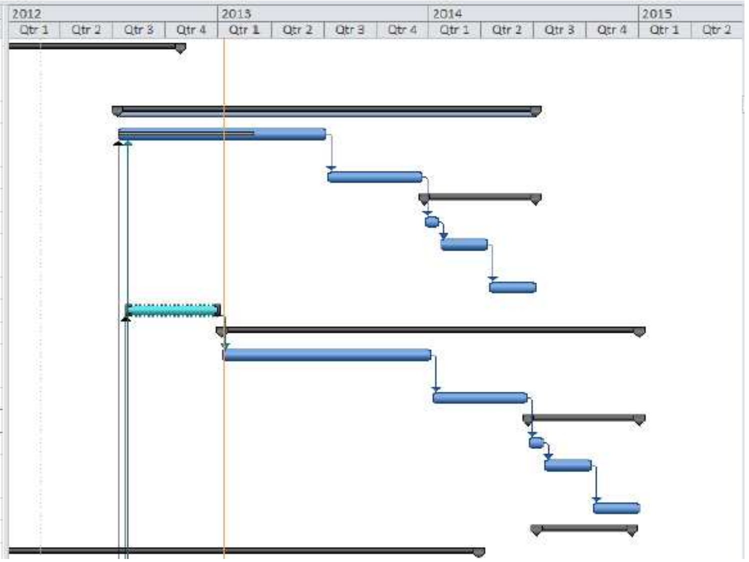
Processing runs smoothly, ahead of schedule

Second batch with 18 wafers will follow soon

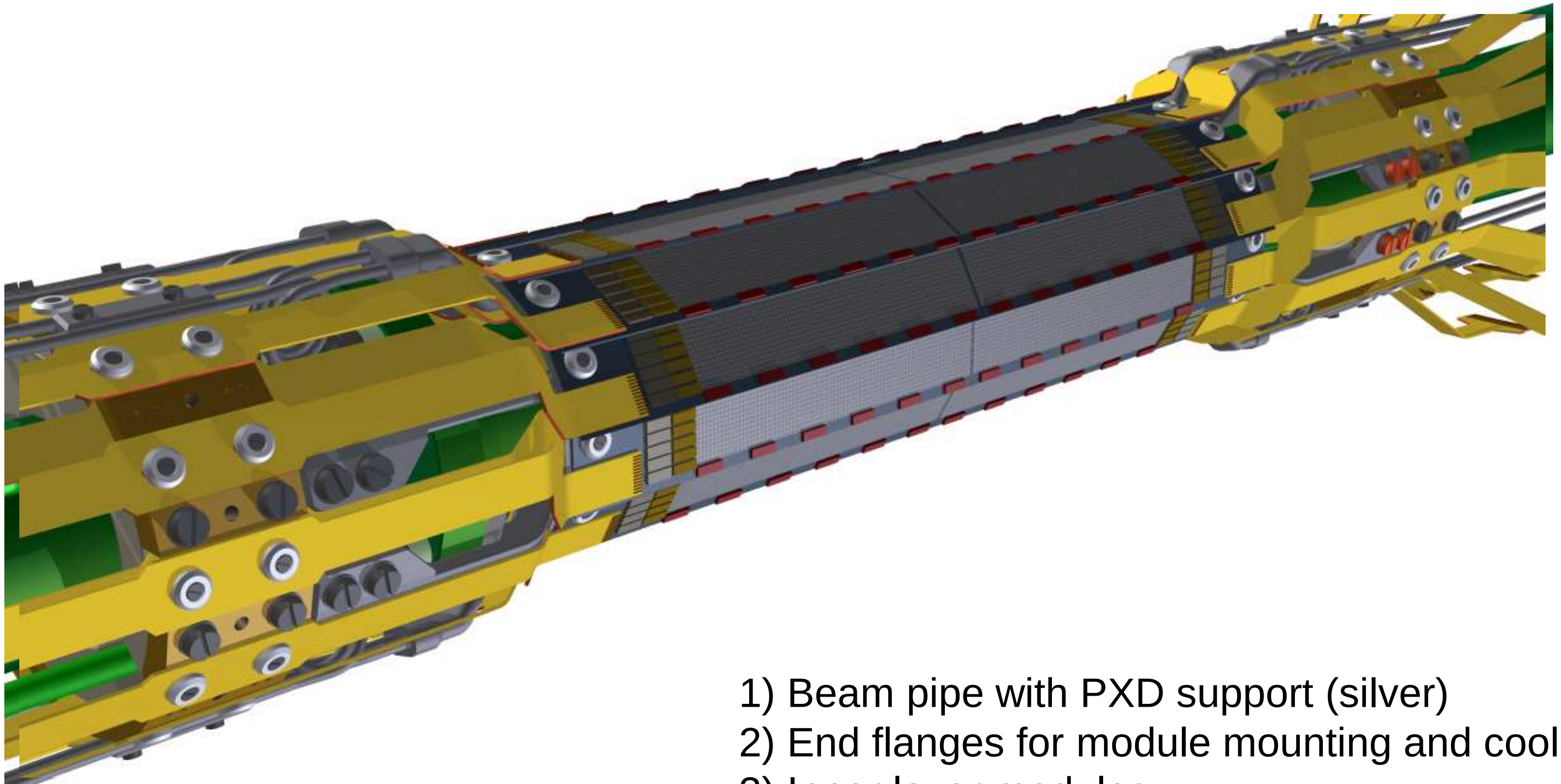
Yield requirements: 20% for outer layer
27% for inner layer



Task Name	Duration	Start	Finish
SOI preparation (for prototype and final run)	295 days	Mon 12.09.11	Fri 26.10.12
PXD9a production	520 days	Mon 09.07.12	Fri 04.07.14
frontside processing	13 mons	Mon 09.07.12	Fri 05.07.13
metal layers	6 mons	Mon 08.07.13	Fri 20.12.13
thinning	140 days	Mon 23.12.13	Fri 04.07.14
test	4 wks	Mon 23.12.13	Fri 17.01.14
Etching handle wafer	12 wks	Mon 20.01.14	Fri 11.04.14
Copper layer	12 wks	Mon 14.04.14	Fri 04.07.14
Pause	6 mons	Mon 23.07.12	Fri 04.01.13
PXD9b production	520 days	Mon 07.01.13	Fri 02.01.15
frontside processing	13 mons	Mon 07.01.13	Fri 03.01.14
metal layers	6 mons	Mon 06.01.14	Fri 20.06.14
thinning	140 days	Mon 23.06.14	Fri 02.01.15
test	4 wks	Mon 23.06.14	Fri 18.07.14
Etching handle wafer	12 wks	Mon 21.07.14	Fri 10.10.14
Copper layer	12 wks	Mon 13.10.14	Fri 02.01.15
Sensor Tests	120 days	Mon 07.07.14	Fri 19.12.14
1.3 ASIC	1404 days?	Tue 11.11.08	Fri 28.03.14



Support

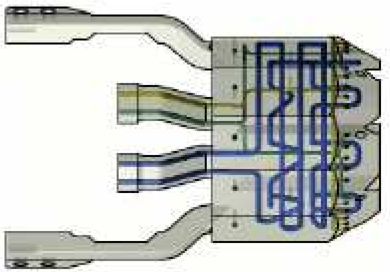


1) Beam pipe with PXD support (silver)
2) End flanges for module mounting and cooling
3) Inner layer modules
4) Outer layer modules

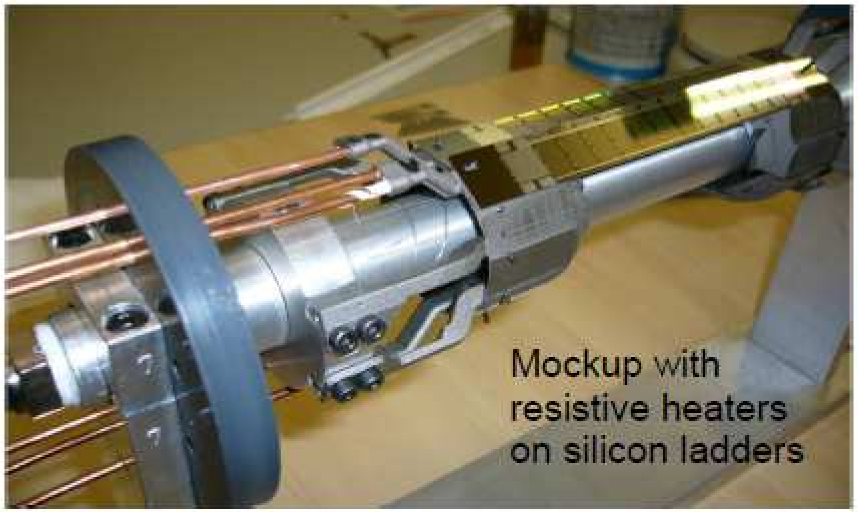
End Flange - Cooling Block

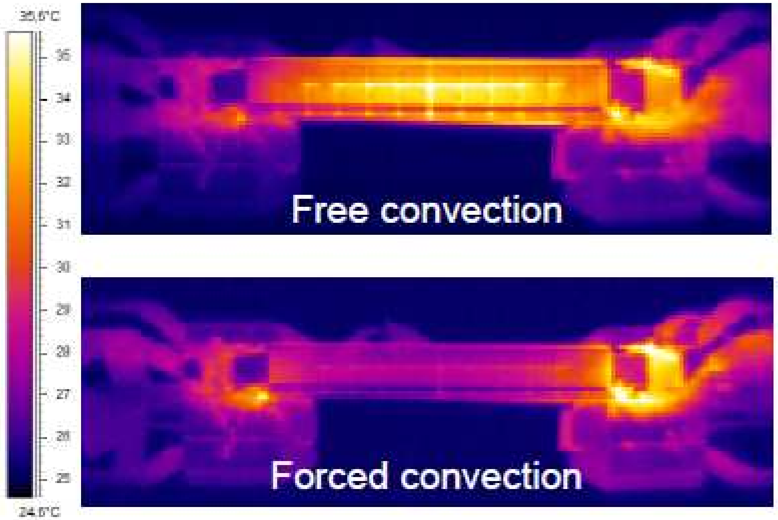
- Cooling system outside acceptance
- Closed CO_2 cooling system for readout electronics (320W)
- Cold dry air for steering chips and DEPFET pixels (40W)

150mW/cm²



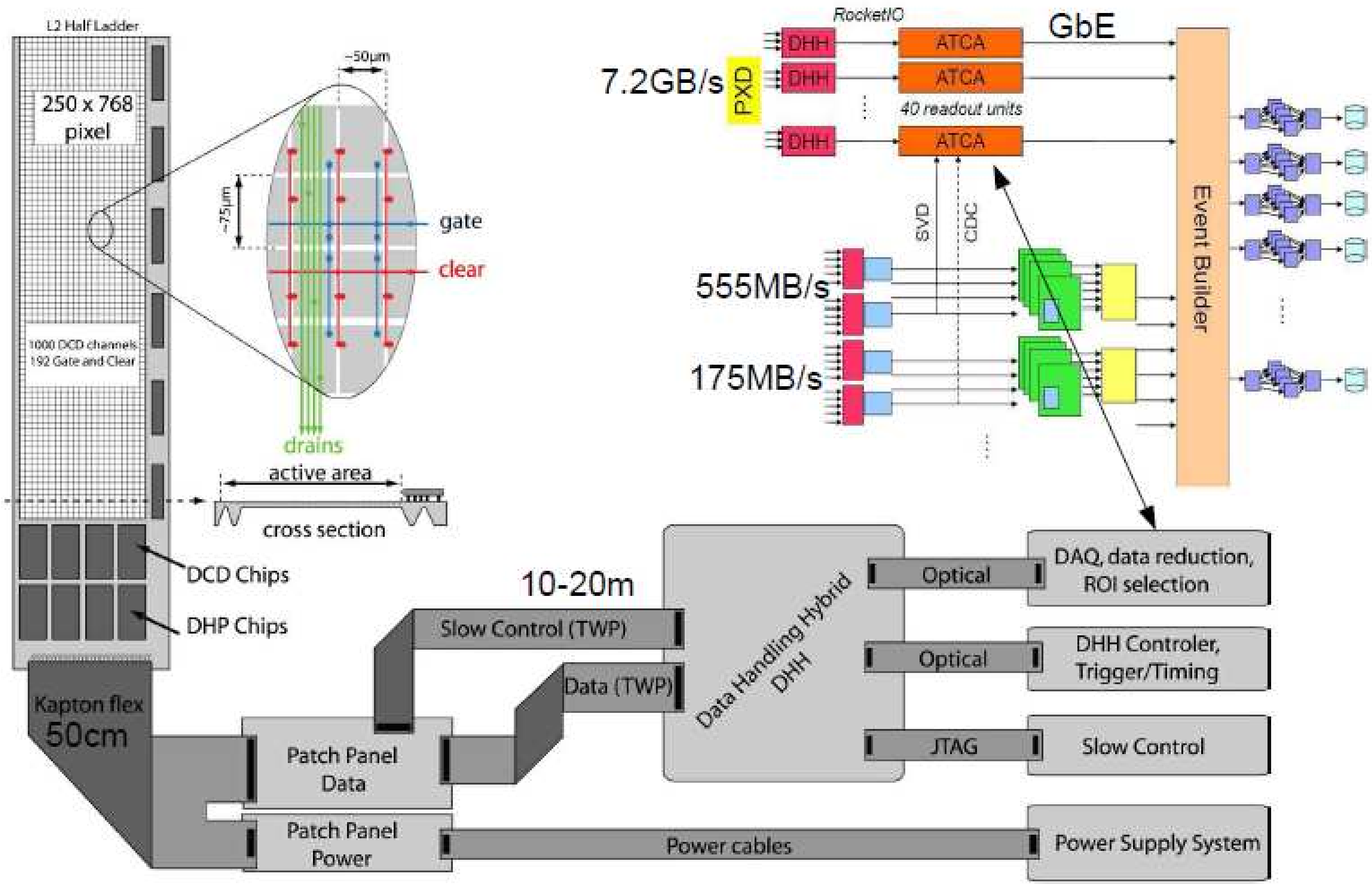
- Stainless steel
- Fast sintering
- Blue: CO_2 channels
- Yellow: Air channels





DAQ

Max data rate: 20 GB/s @ 3% occupancy (expected: 0.8%)
Date reduction (ROI selection): ~ 700 MB/s



Conclusions

SuperKEKB upgrade progressing well
-> machine commissioning starts beginning of 2015

Major upgrade of Belle II detector underway (inner detector, PID, KLM)

Pixel Detector:

- DEPFET sensors thinned to 75µm
- low mass self supporting, air cooled module: 0.21% X0
- S/N, resolution, readout speed and radiation hardness tested
- production of final sensors started
- CO_2 cooling for ASICs (and SVD)
- mounting blocks with integrated cooling channels (3D printing)

Installation of PXD/SVD: September 2015

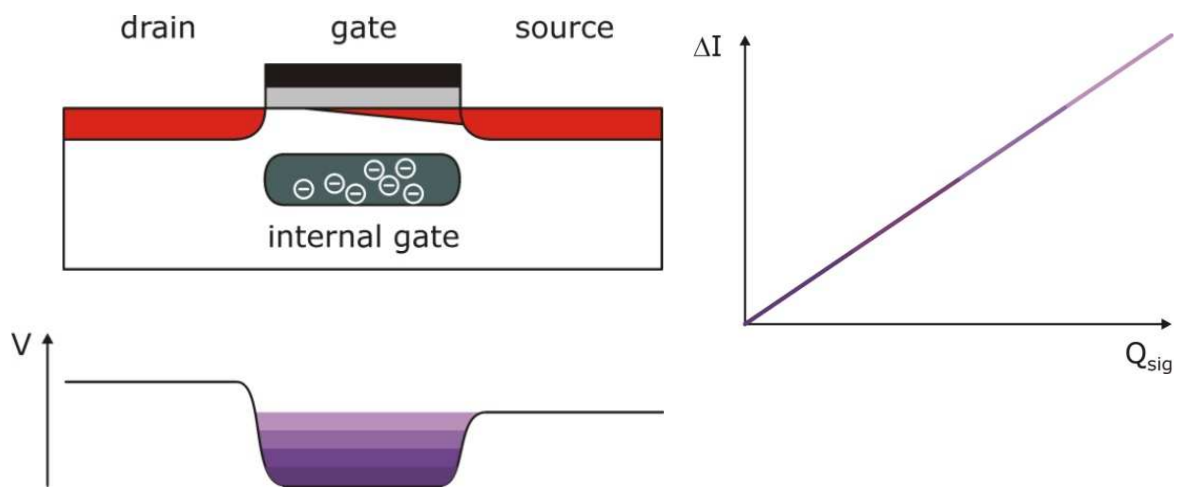
Physics start: mid 2016

DSSC DEPFET Principle

J. Kemmer and G. Lutz, “New semiconductor concept,” *NIM. A, 1987*

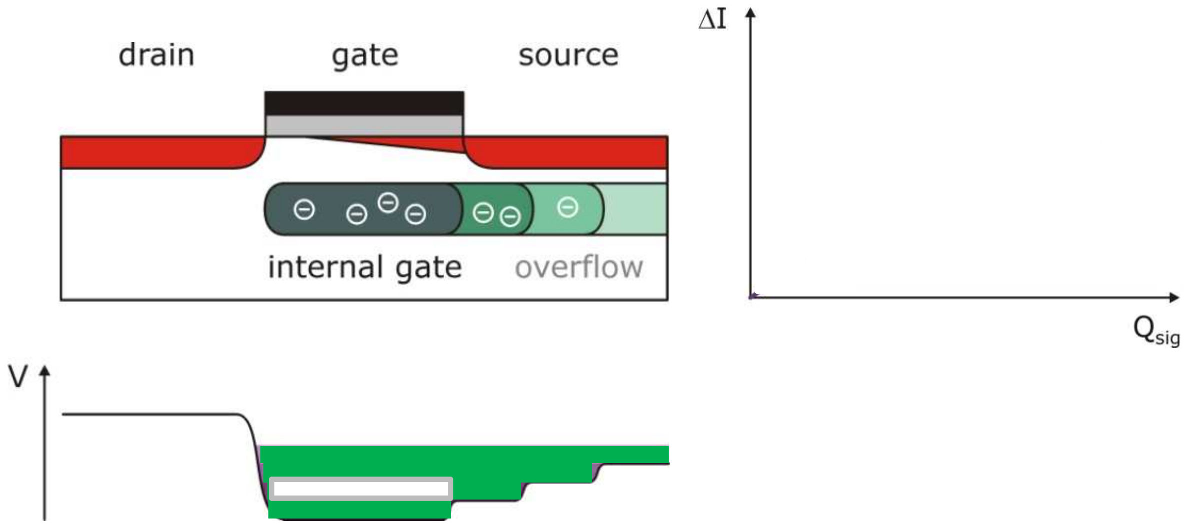
Standard DEPFET principle

- p-FET on depleted n-bulk
  - ↳ All signal charge collected in potential minimum below FET channel **"internal gate"**
  - ↳ all signal charges cause an equal effect on the FET current
  - ↳ **linear $\Delta I/Q_{sig}$ characteristics**
- reset via ClearFET
- low capacitance & noise



DSSC adaptation

- ↳ signal charges at high levels also stored under source
- ↳ less/no effect on FET current
- ↳ **non-linear $\Delta I/Q_{sig}$ characteristics**
- ↳ gain curve engineering by dose & geometry of implantations



Need O(100x) more data
→Next generation B-factories