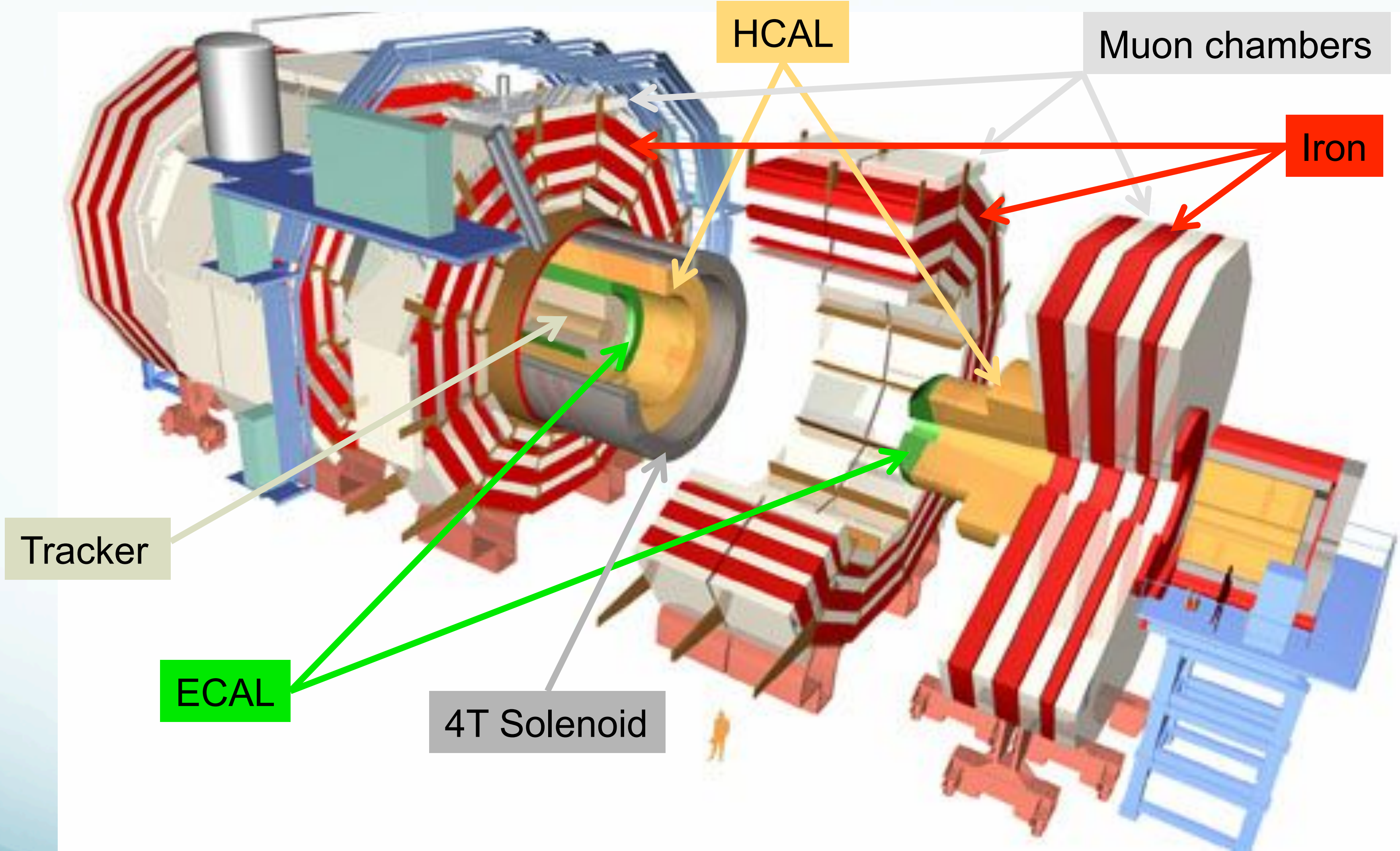
The CMS Tracker Upgrade for HL-LHC

Project overview and outlook

Outline

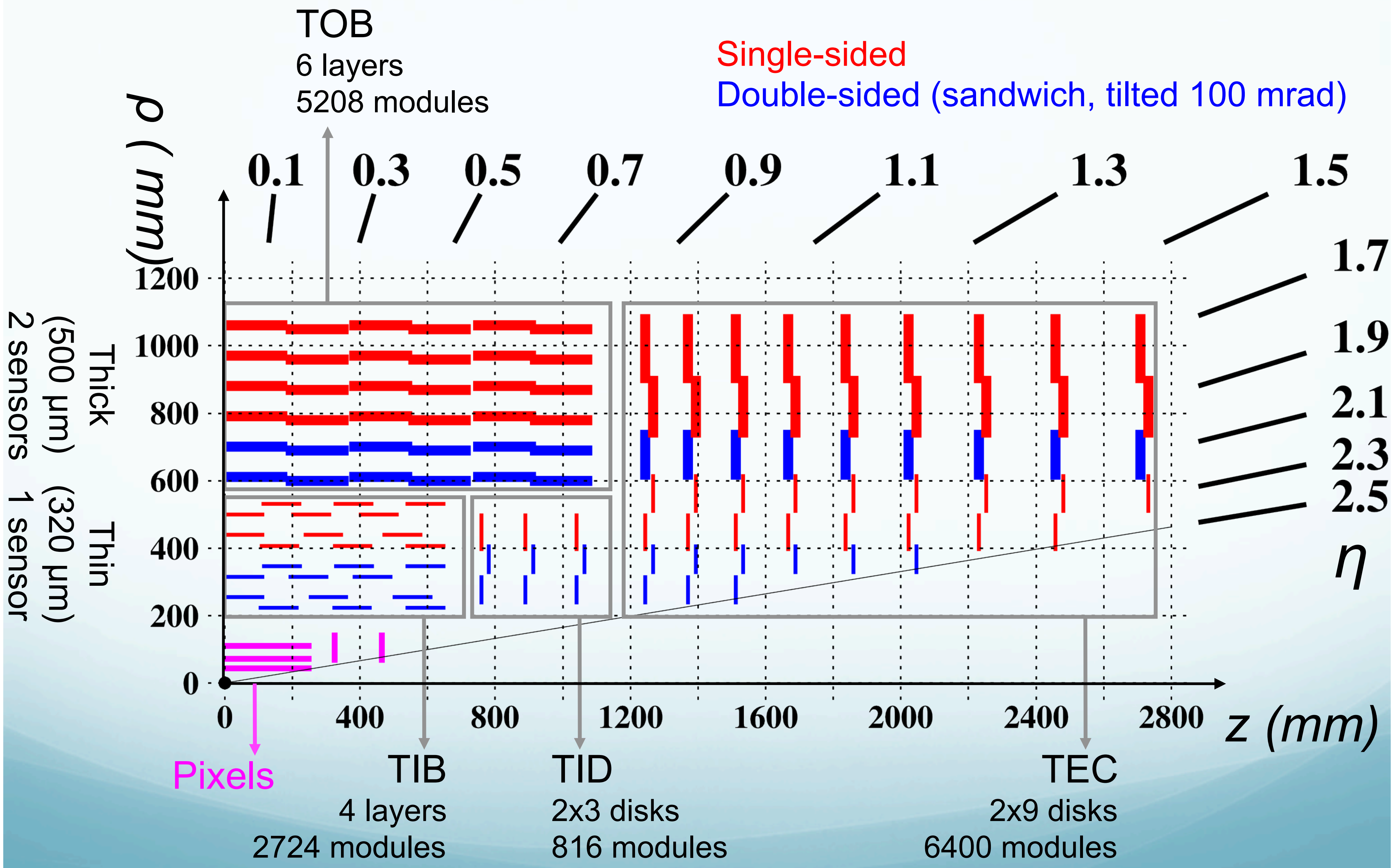
- The HL-LHC Tracker: requirements
- Overview of R&D
  - Development of "p_T modules"
- Tracker geometries
- Expected performance
- Ultimate pixel upgrade
- Summary and outlook

The Tracker in CMS

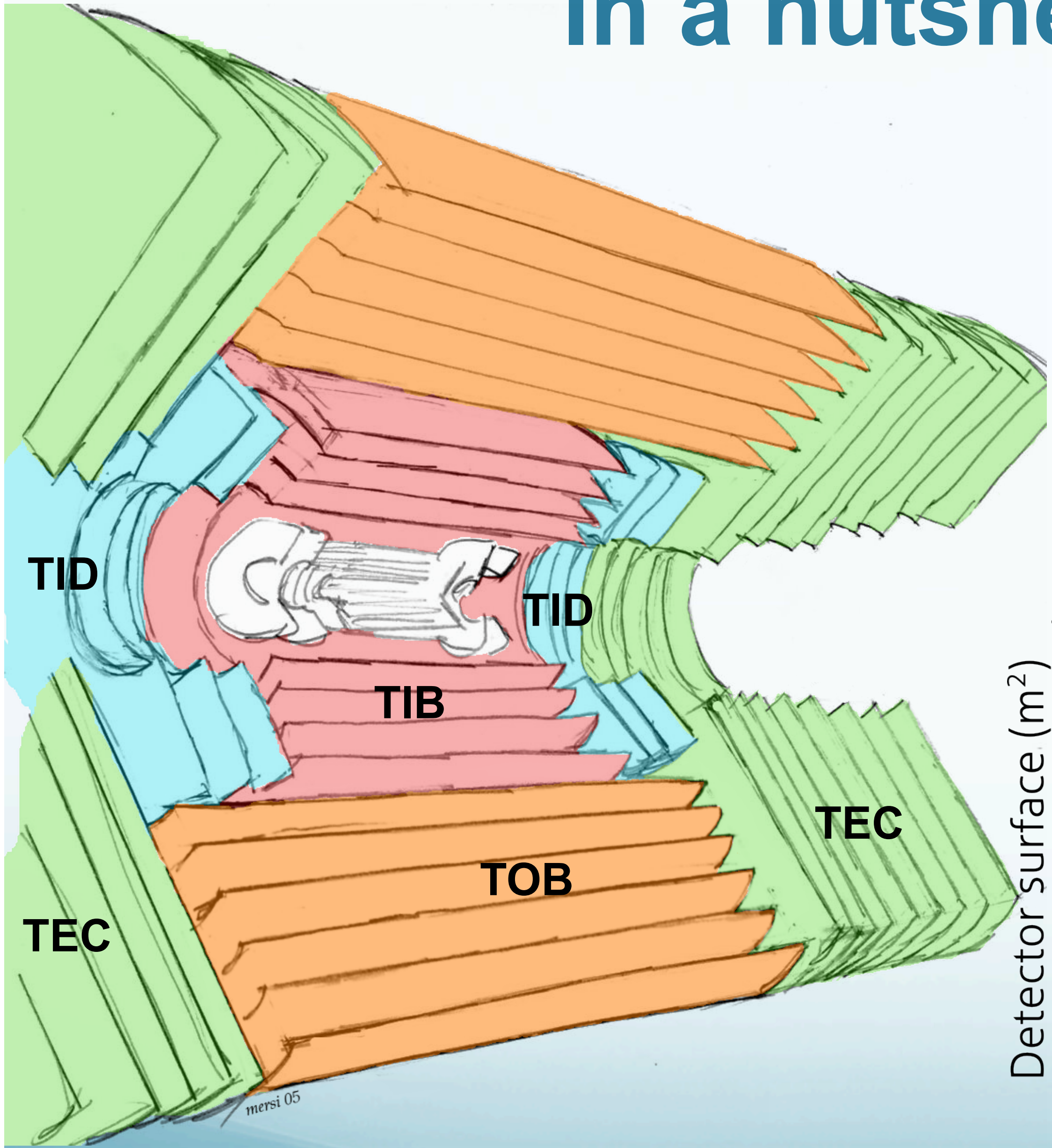


- Total weight: 12,500 t
- Overall diameter: 15 m
- Overall lenght: 21.6 m
- Magnetic field: 3.8 T

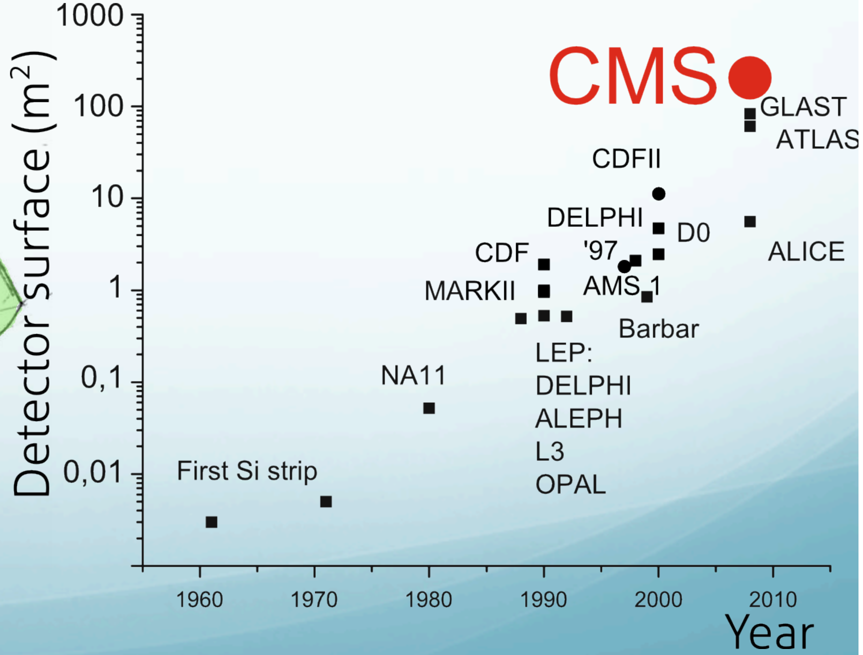
The Tracker layout



In a nutshell…

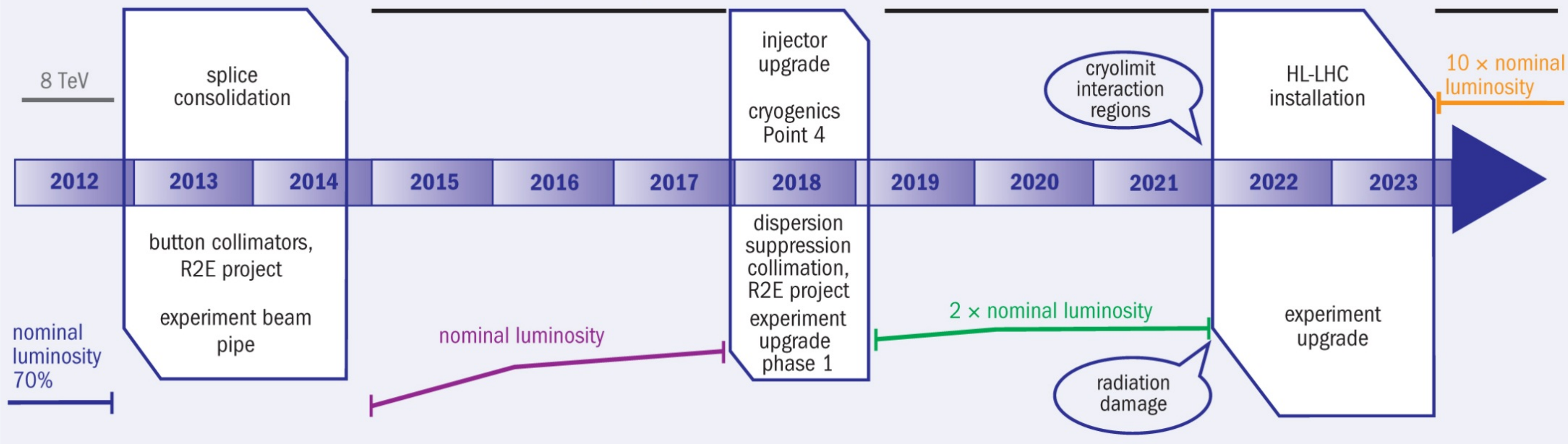


Volume	23 m^3
Active area	210 m^2
Modules	15'148
Front-end chips	72'784
Read-out channels	9'316'352
Bonds	24'000'000
Optical channels	36'392
Raw data rate:	1 Tbyte/s
Power dissipation:	30 kW
Operating T:	−10°C



The HL-LHC

A plan for the LHC in the next 10 years [L. Rossi, IPAC 2011]



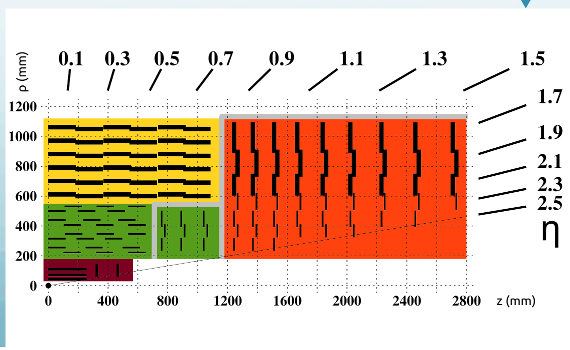
Pixel Upgrade
"phase 1"

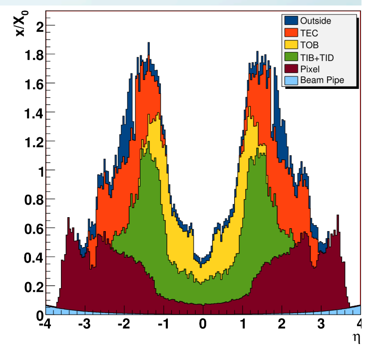
Ful Tracker Upgrade
"phase 2"

Basic requirements and guidelines - I

- **Radiation hardness**
  - Ultimate integrated luminosity considered ~ 3000 fb^{-1}
    - To be compared with original ~ 500 fb^{-1}
- **Granularity**
  - Resolve up to 200÷250 collisions per bunch crossing
    - Nominal figure of 5×10^{34} cm^{-2} s^{-1} @ 40 MHz corresponds to ≥ 100 collisions
      - Keep 20 MHz as worst-case limit
  - Maintain occupancy at the few % level
  - Requires much shorter strips!
- **Improve tracking performance**
  - Reduce material in the tracking volume
    - Improve performance @ low p_T
    - Reduce rates of nuclear interaction, γ conversions, bremsstrahlung…
  - Reduce average pitch
    - Improve performance @ high p_T

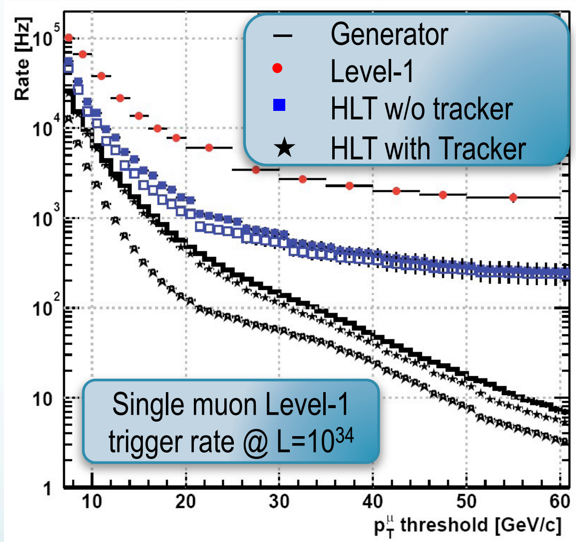
Substantially higher channel count!





Basic requirements and guidelines – II

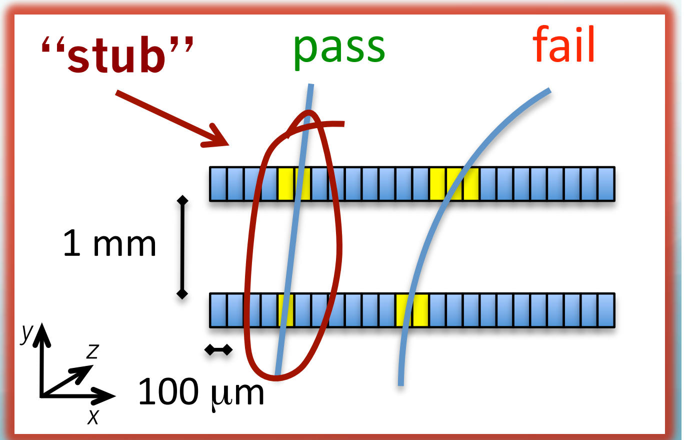
- Tracker input to Level-1 trigger
  - μ, e and jet rates would exceed 100 kHz at high luminosity
    - ★ Even considering "phase-1" trigger upgrades
  - Increasing thresholds would affect physics performance
    - ★ Performance of algorithms degrades with increasing pile-up
      - Muons: increased background rates from accidental coincidences
      - Electrons/photons: reduced QCD rejection at fixed efficiency from isolation
  - Even HLT without tracking seems marginal
  - Add tracking information at Level-1
    - ★ Move part of HLT reconstruction into Level-1!



- Full-scope objectives:
  - Reconstruct "all" tracks above 2 ÷ 2.5 GeV
  - Identify the origin along the beam axis with ~ 1 mm precision

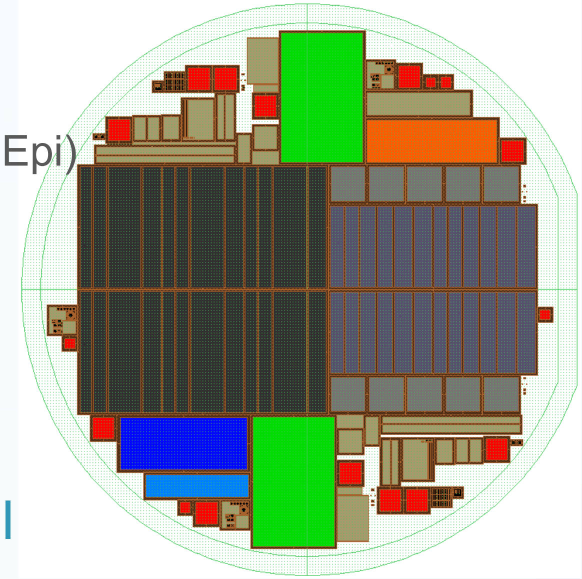
General concept

- Silicon modules provide at the same time “Level-1 data” (@ 40 MHZ), and “readout data” (@ 100 kHz, upon Level-1 trigger)
  - The whole tracker sends out data at each BX: “push path”
- Level-1 data require local rejection of low-p_T tracks
  - To reduce the data volume, and simplify track finding @ Level-1
    - ★ Threshold of ~ 1÷2 GeV ⇒ data reduction of one order of magnitude or more
- Design modules with p_T discrimination (“p_T modules”)
  - Correlate signals in two closely-spaced sensors
    - ★ Exploit the strong magnetic field of CMS
- Level-1 “stubs” are processed in the back-end
  - Form Level-1 tracks, p_T above 2÷2.5 GeV
    - ★ To be used to improve different trigger channels



Sensors R&D - I

- HPK project
  - Different materials
    - Float-zone (FZ), Magnetic Czochralski (MCz), Epitaxial (Epi)
  - Different thicknesses and technologies
    - n-bulk, p-bulk with p-spray and p-stop isolation
    - Wafers with 2nd metal layer
  - Several strip and pixel geometries
  - ~ 6 wafers of each material; >150 wafers in total
  - Exhaustive program of proton and neutron irradiations
  - Lab tests complemented by device simulations

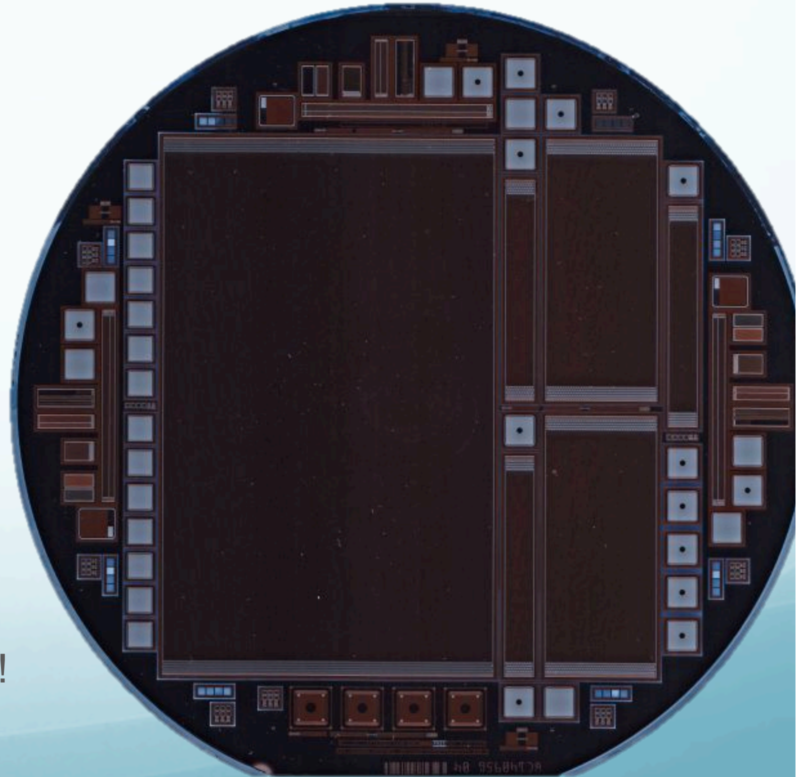


- Gaining excellent understanding of materials
  - Doping profiles and process details
  - Almost reverse engineering!

Sensors R&D - II

- HPK project main goals
  - Choose material and technology for outer Tracker Upgrade
    - ★ Target: early 2013, then move on to sensor prototyping
      - ❖ Current activities likely beyond the scope of the immediate CMS needs!
  - Provide a solid baseline in planar technology for pixel phase-2 upgrade
    - ★ To be compared with more “exotic” technologies
      - ❖ Ongoing R&D on diamonds and 3d silicon

- Qualification run @ Infineon
  - 25 wafers produced
    - ★ p-on-n 300 μm thickness as in present TK
  - Basic tests done, irradiations planned
    - ★ Nearly perfect quality out of the box!
      - ❖ E.g. 0.5% faulty strips, likely to improve in the future
  - Potential to explore different options
    - ★ P-type bulk, thinner sensors, and even 8” wafers!
  - Very promising for the future!



Electronics system

Concept well-advanced, based on ongoing developments

- Data links: Low-Power GigaBit Transceiver (LP-GBT)
  - Further evolution of GBT (under development)
  - 65 nm technology, simplified to minimize power and footprint size
  - Same bandwidth (5 Gb/s total, 3.2 Gb/s for data)
  - To be integrated *at module level,* with lightweight opto-coupler
    - Good match to expected bandwidth ***including L1 data, readout data and controls!***
- Power: DC-DC converters
  - Pursue ongoing developments
    - Will be used already in the Pixel Upgrade
  - Key development to reduce material in the tracking volume
    - Bring in current @ 10÷12 V: gain one order of magnitude in conductor cross-section
    - Dominant contribution to material in present Tracker
  - Also integrated *at module level*
    - Reasonable match with expected power consumption
- Fully integrated modules: the module is the system!

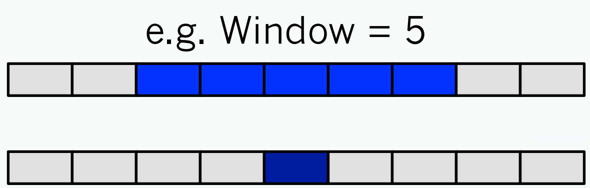
Cooling and mechanics

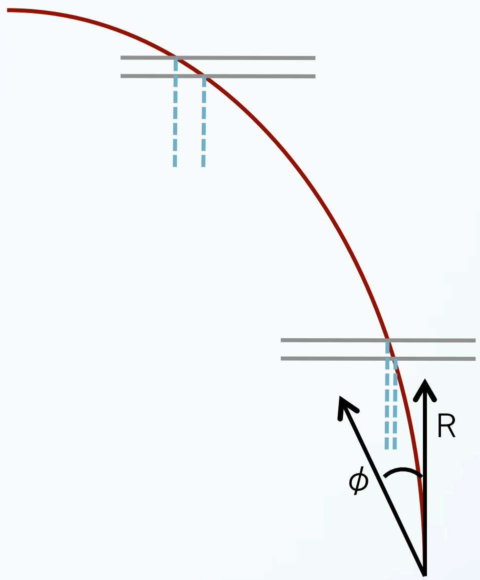
- Cooling: two-phase CO_2 is the baseline
  - Evaporative system + excellent thermodynamic properties of CO_2 can provide low-mass, high-efficiency cooling
  - Experience being gained with phase-1 pixel system
    - By far the largest system ever built in HEP!
  - No dedicated phase-2 R&D yet

- Mechanics
  - Studies of possible endcap geometries ongoing (Lyon)
    - Two-phase cooling prefers simple pipe geometries
    - Adopt rectangular modules as in barrel
      - To avoid too many module flavours
    - Several options under study
  - Mechanics for barrel "double-stack" geometry under development (FNAL)
    - Layers closely-spaced in pairs (more details later) ⇒ common supporting mechanics
  - Prototyping of 2S modules to start this year
    - Preparation work ongoing

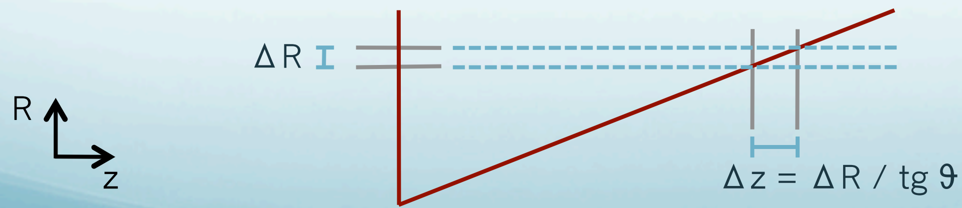
More on p_T modules working principle

- Sensitivity to p_T from measurement of $\Delta(R\varphi)$ over a given ΔR
- For a given p_T, $\Delta(R\varphi)$ increases with R
  - A same geometrical cut, corresponds to harder p_T cuts at large radii
  - At low radii, rejection power limited by pitch
  - Optimize selection window and/or sensors spacing
    - ★ To obtain, ideally, consistent p_T selection through the tracking volume



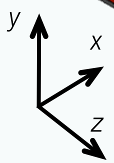


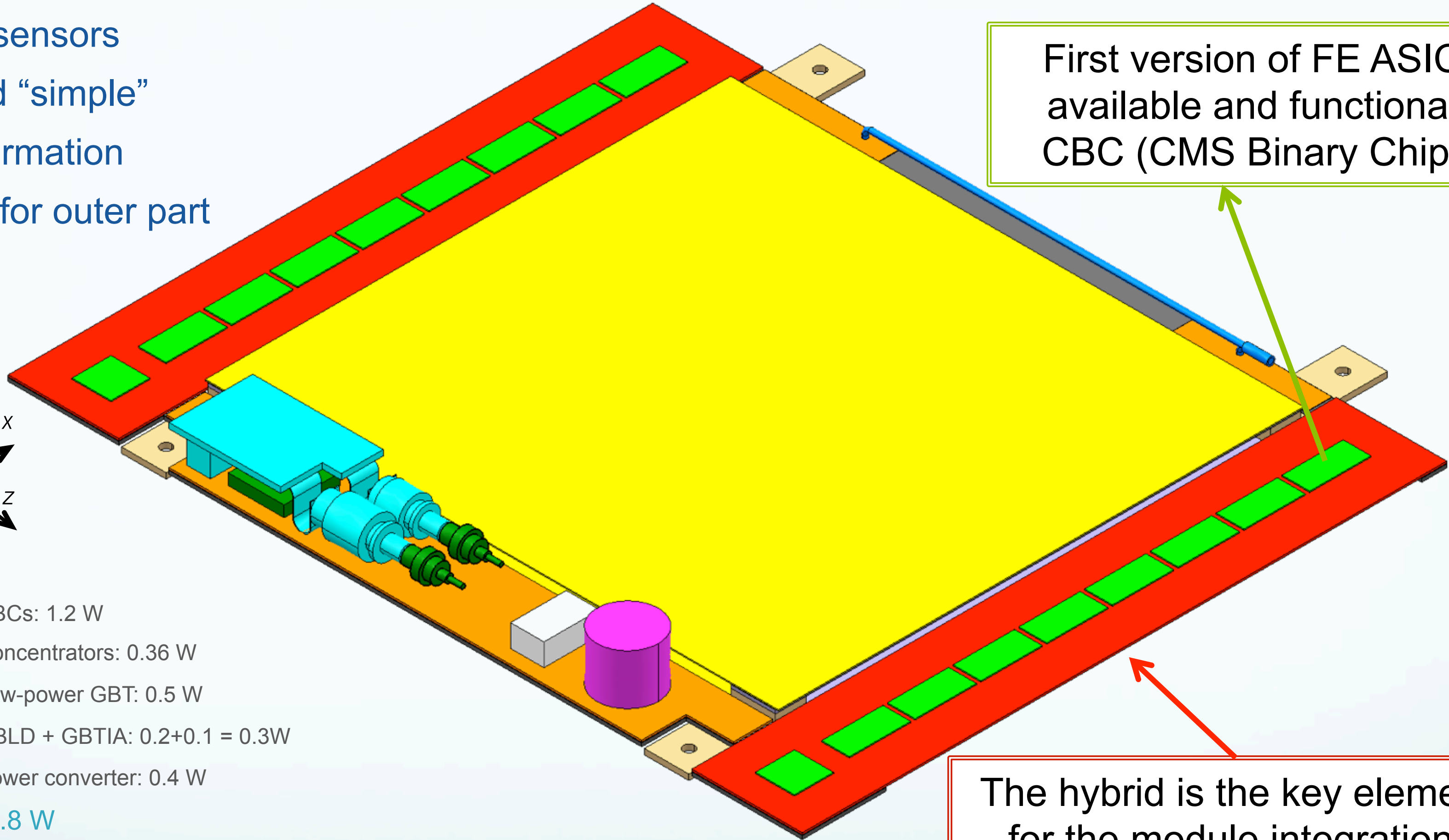
- In the barrel, ΔR is given directly by the sensors spacing
- In the end-cap, it depends on the location of the detector
  - End-cap configuration typically requires wider spacing



p_T modules types: “2S Module”

- 2x Strip sensors
- Light and “simple”
- No z information
- Suitable for outer part



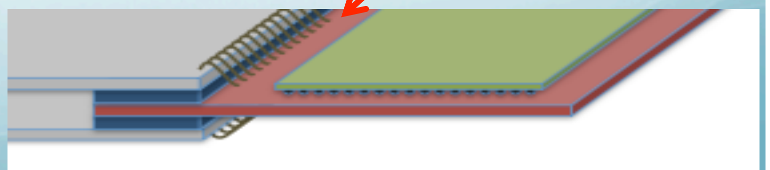


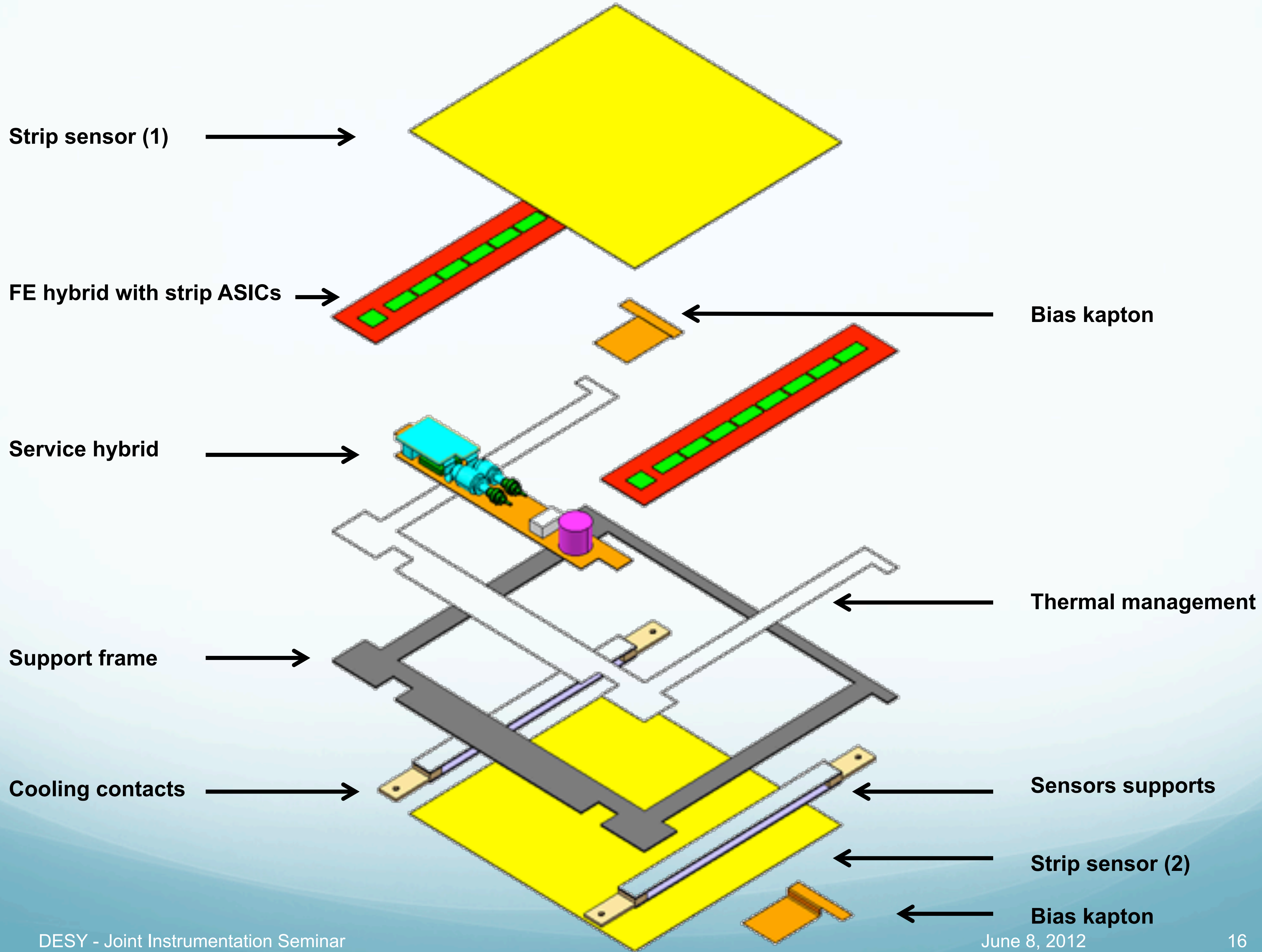
First version of FE ASIC available and functional CBC (CMS Binary Chip)

- Power
  - ★ CBCs: 1.2 W
  - ★ Concentrators: 0.36 W
  - ★ Low-power GBT: 0.5 W
  - ★ GBLD + GBTIA: 0.2+0.1 = 0.3W
  - ★ Power converter: 0.4 W
  - ⦿ Total 2.8 W

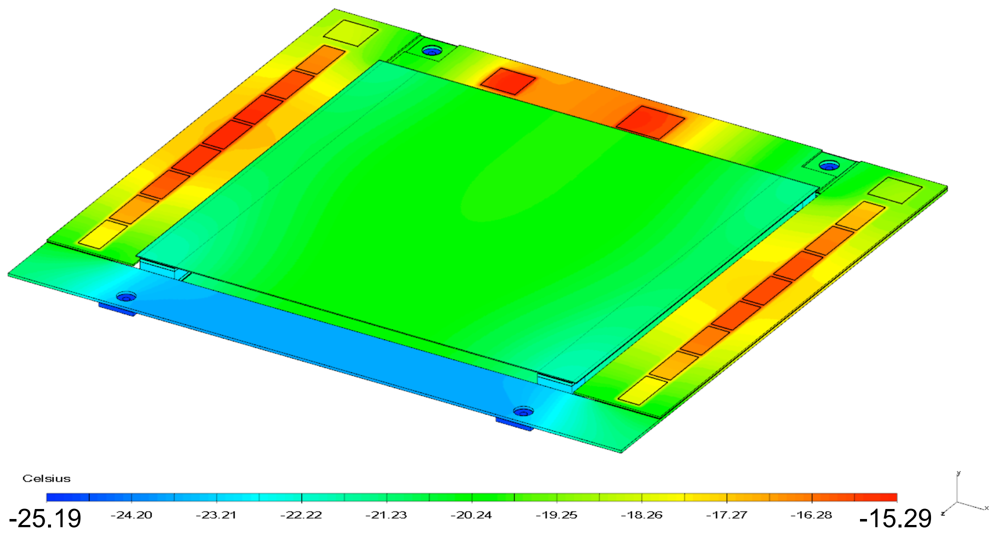
The hybrid is the key element for the module integration!

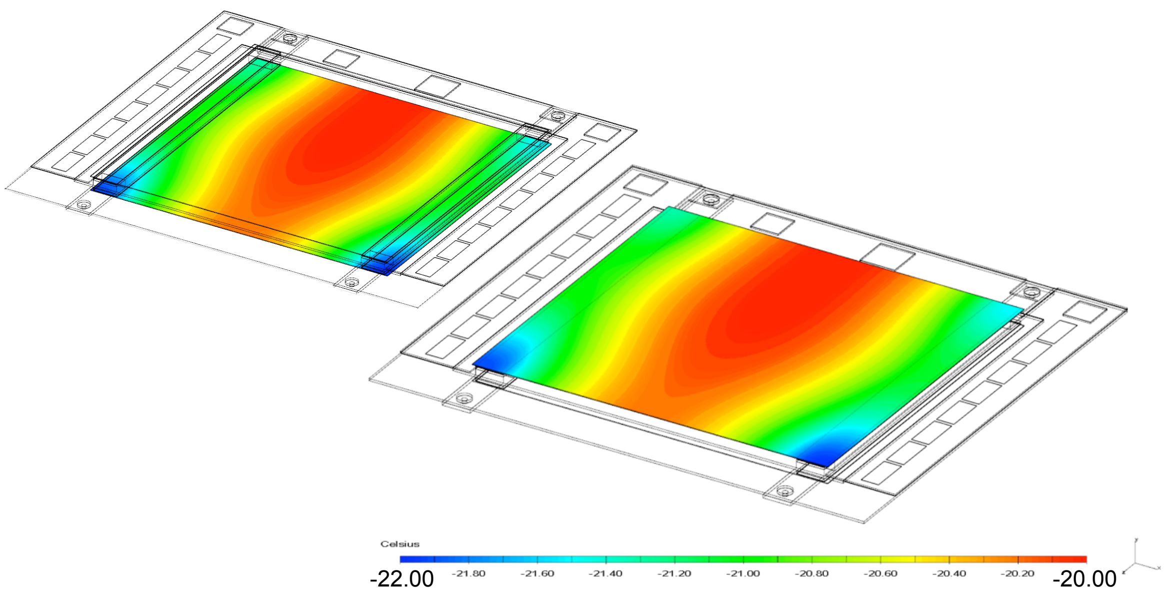
- ≈ 5 cm long strips, ≈ 90 μm pitch, ≈ 10x10 cm^2 overall sensor size
- Wirebonds from the sensors to the hybrid **on the two sides**
  - ⦿ 2048 channels on each hybrid
- Chips bump-bonded onto the hybrid
- **Prototyping to start during 2012!**




Strip sensor (1)
FE hybrid with strip ASICs
Bias kapton
Service hybrid
Thermal management
Support frame
Cooling contacts
Sensors supports
Strip sensor (2)
Bias kapton

Thermal modelling





- FEA results encouraging
  - ΔT from contacts to hottest point on sensor ~ 5°C
  - Same temperature on both sensors
  - Gradient across sensor ~ 2°C

Module design development

- Several new challenges
  - Inherent to electronics
    - Bump bonding
    - Novel technologies for hybrids
      - Yield, reliability, cost…
    - …
  - Related to the overall assembly
    - Two sensors with one hybrid!
      - Precision
      - Support for wirebonding
      - Stiffness of the assembly
      - …
    - New hybrid technologies, lower mass target
      - New materials
      - Surface treatment/gluing
      - ....

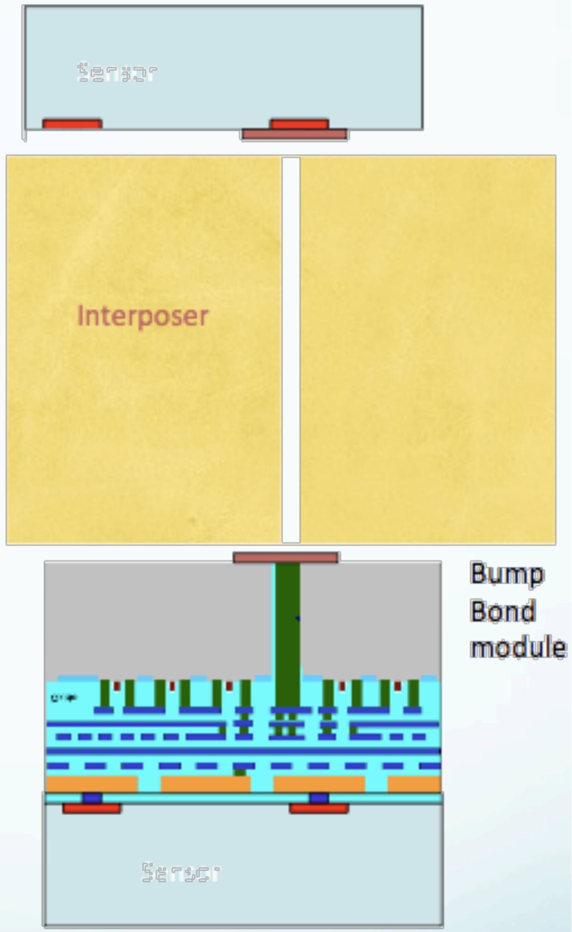
- Strategy: build simplified prototypes
  - Design and procure circuits implementing:
    - Bond pads
    - Resistors for power dissipation
    - Lines for connectivity tests
  - Qualify assemblies under all aspects
    - Ahead of / in parallel with development of functional components

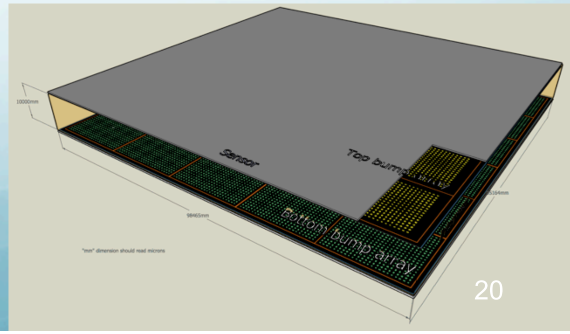
Prototyping

- WP1: gluing techniques
  - Choice of glues, treatment of surfaces, size and location of glue joints.
  - Cold tests, irradiation tests
- WP2: choice of materials
  - Choice and thickness of CF
  - Research on new C-based materials
    - Test gluing, irradiation, cold
- WP3: wirebonding tests
  - Optimize design of sensor support in the frame (sensors-FEH)
  - Optimize module support for bonding
    - Feedback to design of hybrid and HV kapton
- WP4: thermal tests
  - Measure heat transfer efficiency
- WP5: Deformation tests
  - Measure deformations in cold in a lab setup
- WP6: Vibration tests
  - Test module under realistic vibrations that can be expected during transport
- WP7: Module assembly
  - Develop high-precision automatized and reproducible assembly procedure
  - Feedback to module design
- WP8: FEA
  - Thermal and deformation calculations.
  - Guide module design and compare with WP4 and WP5
- WP9: 3d modelling
  - Repository of drawings.

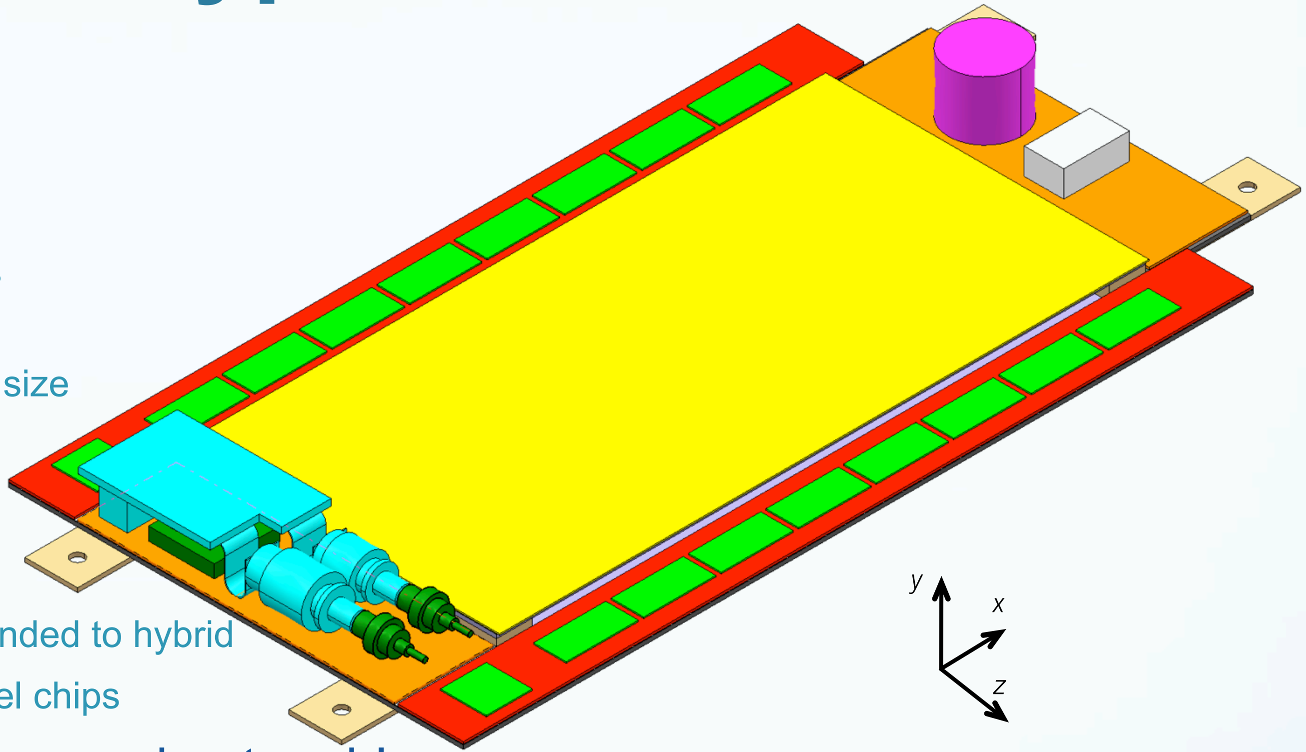
p_T modules types: “VPS Module”

- Strip / Pixel module with vertical interconnections
- Single chip connected to top and bottom sensors
- Analogue paths through interposer from top sensor, segmented in ~ cm long strips
- Bottom sensor gives z info (~ mm long pixels)
- Electronics and connectivity (interposer) are technological challenges (yield, robustness, mass, large–size module)
- Several developments ongoing in parallel
  - 2D demonstrator chip functional
  - TSVs functional, 3D assembly difficult
  - Technology for interposer still an open problem
  - Data processing simulation started
  - Option to use active edge sensors

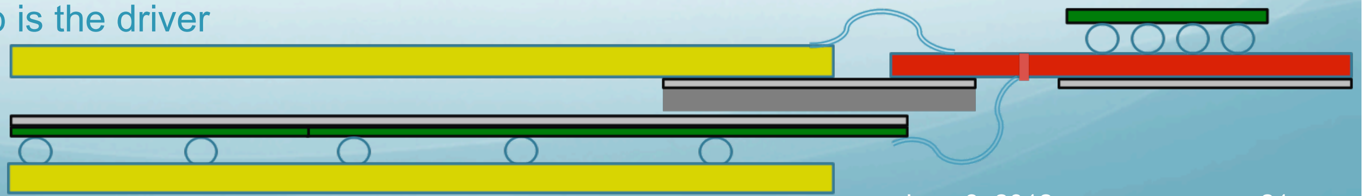


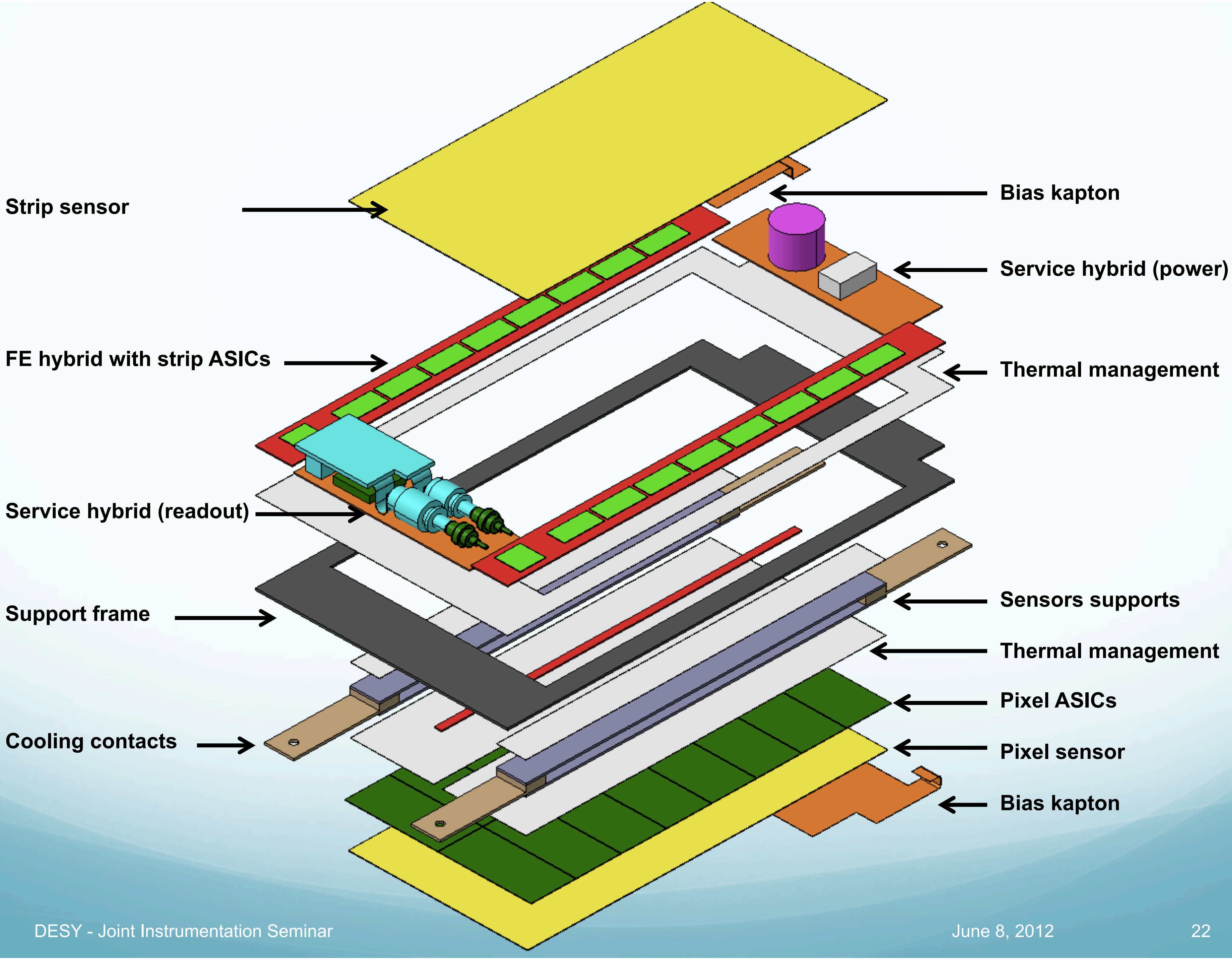


p_T modules types: “PS Module”



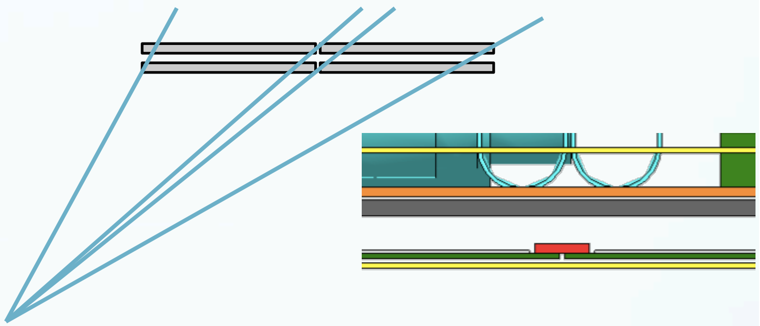
- Sensors:
  - Top sensor: strips
    - 2×25 mm, 100 µm pitch
  - Bottom sensor: long pixels
    - 100 µm × 1500 µm
  - ≈ 5x10 cm^2 overall sensor size
- Readout:
  - Top: wirebonds to “hybrid”
  - Bottom: pixel chips wirebonded to hybrid
  - Correlation logic in the pixel chips
- No interposer, sensors spacing tunable
- Power estimates
    - Pixels + Strips + Logic ~ 2.62 + 0.51 + 0.38 W = 3.51 W
    - Low-power GBT + GBLD + GBTIA ~ 0.5 + 0.2 + 0.1 = 0.8 W
    - Power converter ~0.75 W
  - Total ~ 5.1 W, pixel chip is the driver




Strip sensor
Bias kapton
Service hybrid (power)
FE hybrid with strip ASICs
Thermal management
Service hybrid (readout)
Support frame
Sensors supports
Thermal management
Pixel ASICs
Cooling contacts
Pixel sensor
Bias kapton

Summary of PS module features

- "Horizontal" transmission
  - Path for data longer, but not relevant in power budget, driven by pixel chip
  - No interposer. Potentially lighter.
  - Sensors spacing is tunable with nearly no drawback up to ~ 4 mm.
    - Can be used at low radii (down to R ≳ 20 cm – but not lower!)
      - Helps for z_0 resolution.
    - Can be used also in endcap.



- Two halves of the module independent
  - Inefficiency for stub finding in the middle.
  - But can be solved with TSVs
    - R&D ongoing, very encouraging results
- Size limited to ~10×5 cm^2 is part of the concept (… for the time being…)
- Optimized design for large production / large detector
  - Makes best use of advanced technologies for high-density substrates
  - Relies on commercial technologies
    - But do they work for our "product"? R&D needed!
  - Self-contained building block
- Further improvement: reduce pitch on strip sensor to 50 μm
  - Additional ~500 mW power, wirebonding pitch 50 μm on both sides
  - Better resolution on Δ(Rφ): from 41 μm to 32μm (25% improvement)
  - Improve p_T discrimination and tracking resolution with ~ no impact on module design and mass

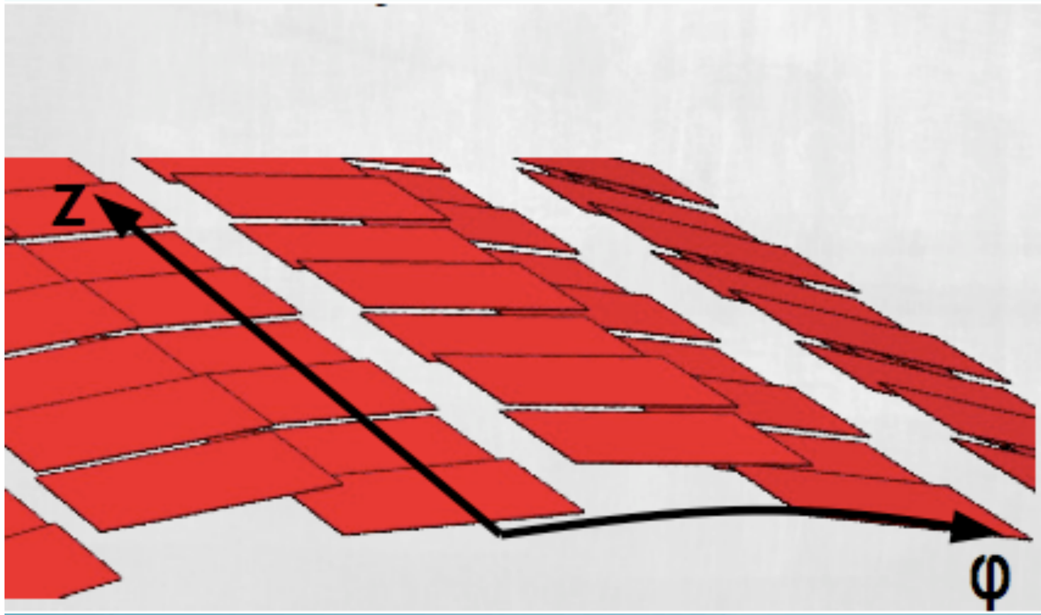
PS module: status and outlook

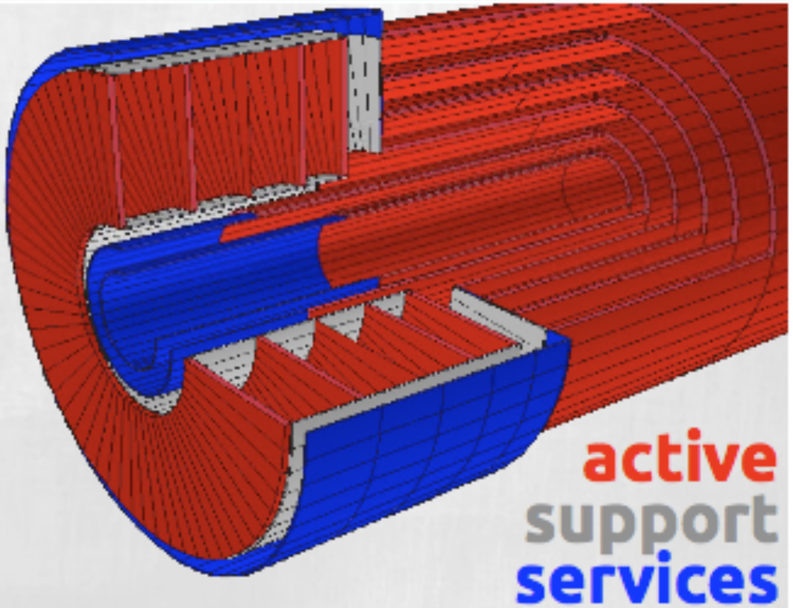
- Electronics substantially less developed compared to 2S module
- Finite Element Analysis performed using present power estimates
  - Cooling the pixel sensor is a challenge
  - Novel materials will hopefully provide a low-mass solution
- Overall power budget exceeds capability of present DC-DC converter
  - Further developments needed. A second converter would be highly undesirable.
- Expect that the development of this module will follow the 2S module with ~1 year delay
  - Adopt wherever possible common or similar technical solutions, as well as coherent concepts and procedures to validate the design

Evaluation of different tracker geometries and options: layout modelling

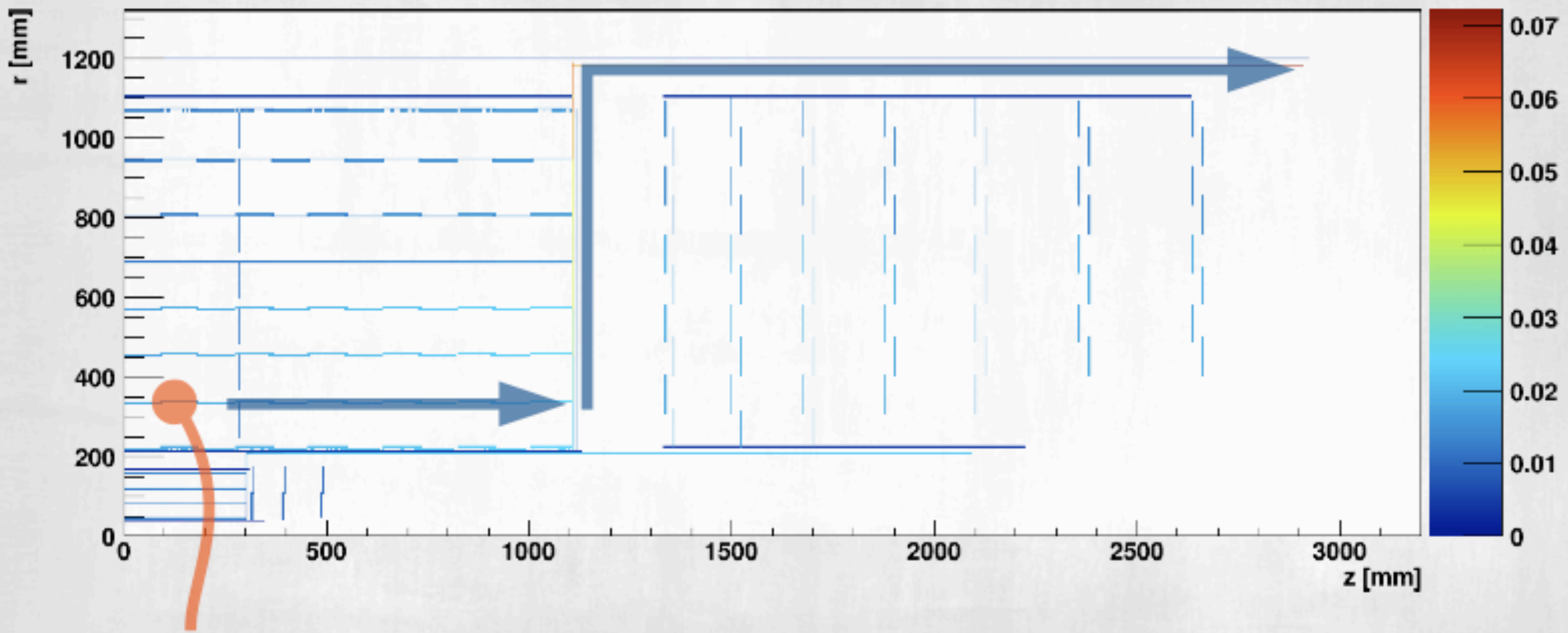
- Dedicated standalone software package©
  - © N. De Maio, S. Mersi, G. Bianchi
    - Based also on work from V. Karimaki and G. Hall

- Allows to place in space active and passive volumes
  - Starting from a small sets of simple parameters



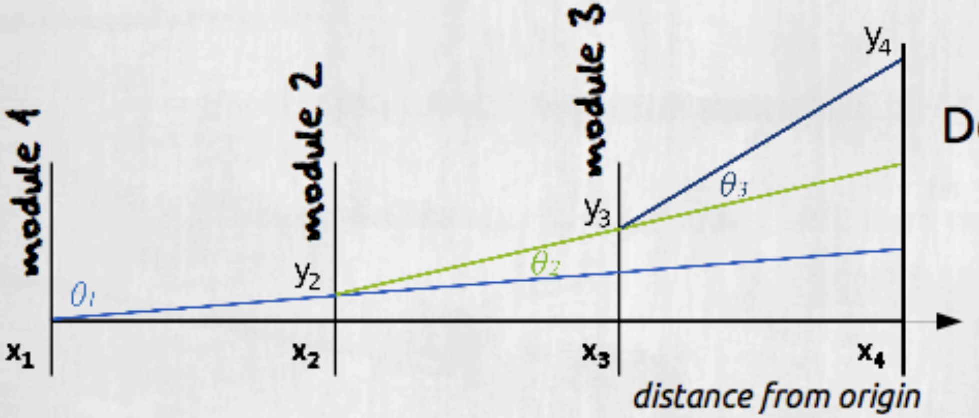


➢ Simple (semi-automatic) modelling of services



Material on active elements + Material for services automatically routed

- Implements estimates of tracking performance
  - Use measurement errors to estimate the errors in track fit parameters
  - **Multiple scattering** treated as (correlated) a measurement error



Deviation due to scattering:

$$y_n = \sum_{i=1}^{n-1} (x_n - x_i)\, \theta_i$$

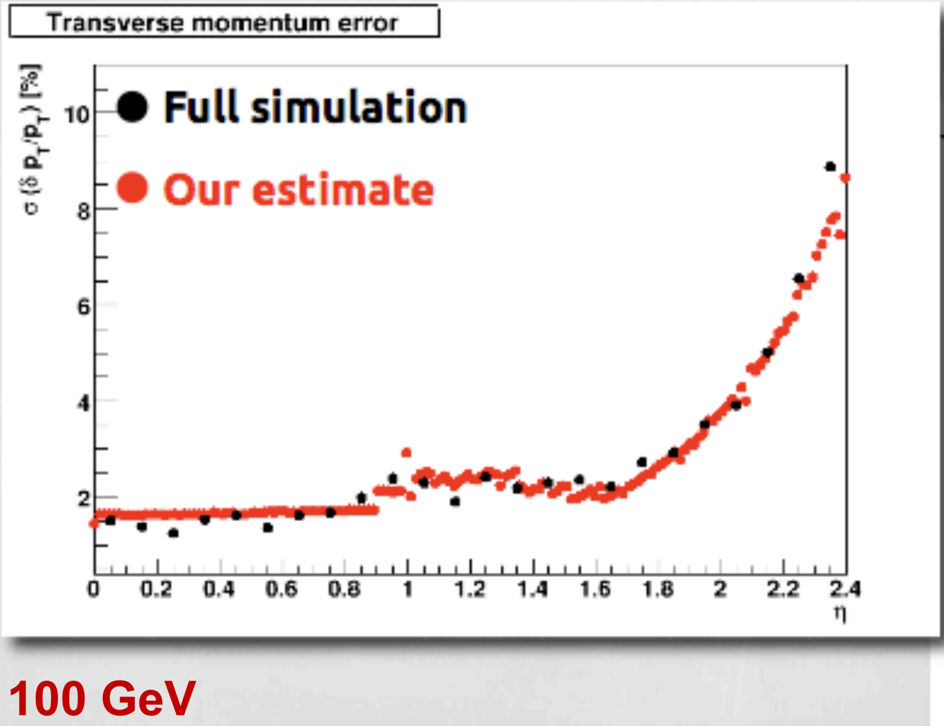
Error correlation matrix:

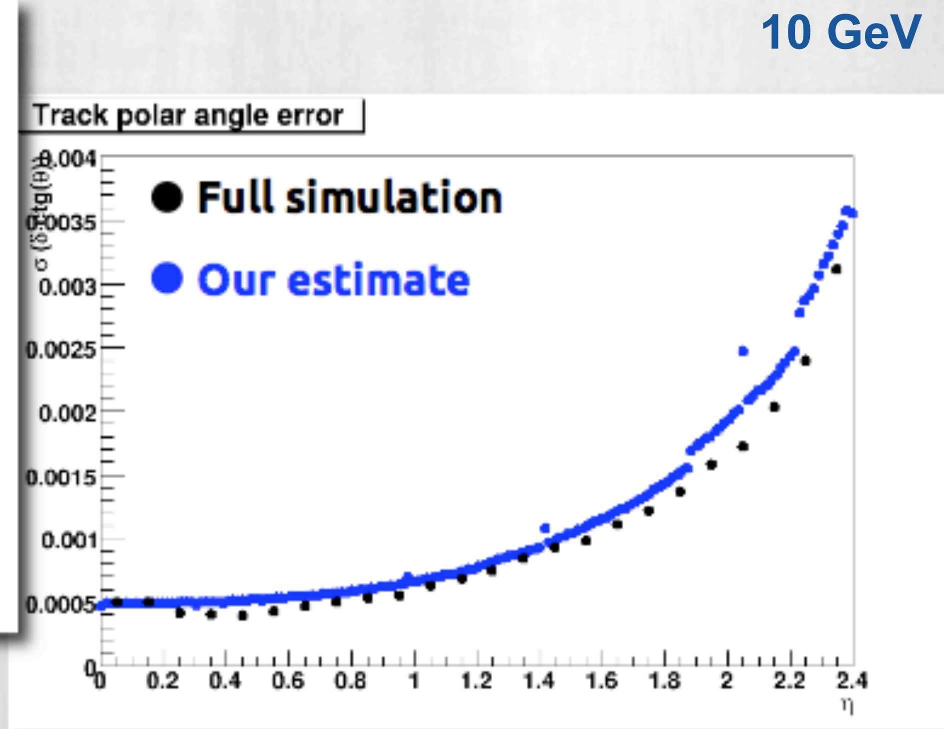
$$\sigma_{n,m} = \langle y_n y_m \rangle = \sum_{i=1}^{n-1} (x_m - x_i)(x_n - x_i) \langle \theta_i^2 \rangle$$

$$\sigma_n^2 = \frac{p^2}{12}$$

- As well as fraction of interacting particles
- Can be used in the same way to evaluate trigger performance potential

➢ Validated by modelling the present tracker

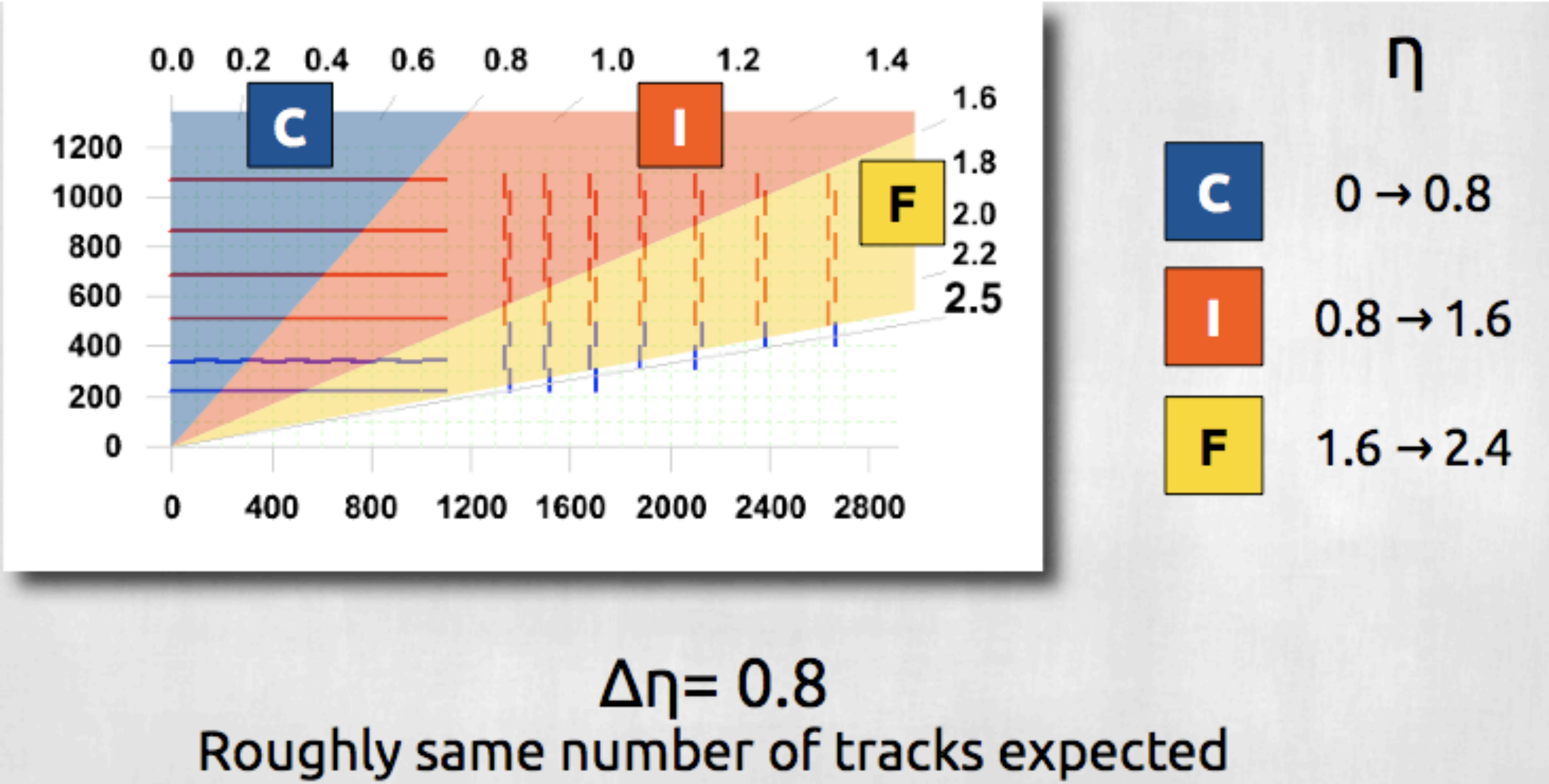




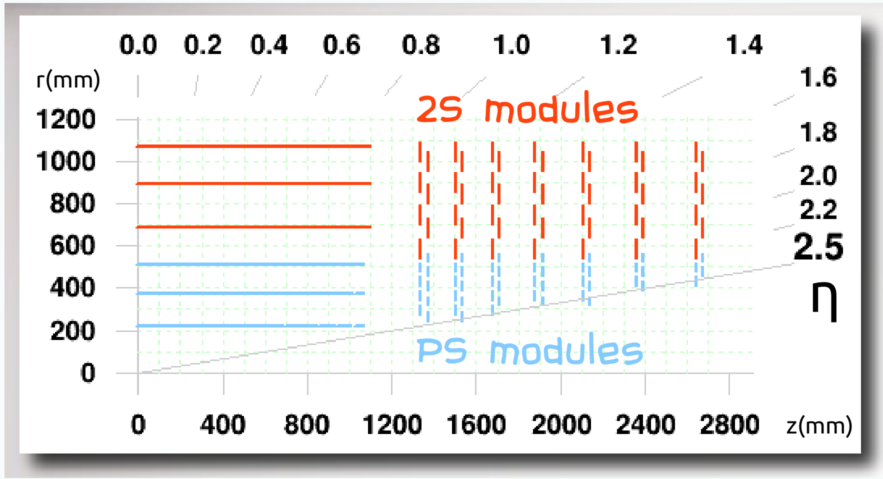
➢ Excellent accuracy out of the box!

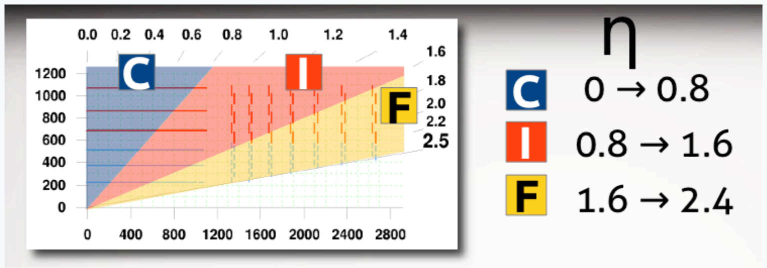
Only a glimpse of some functionalities…

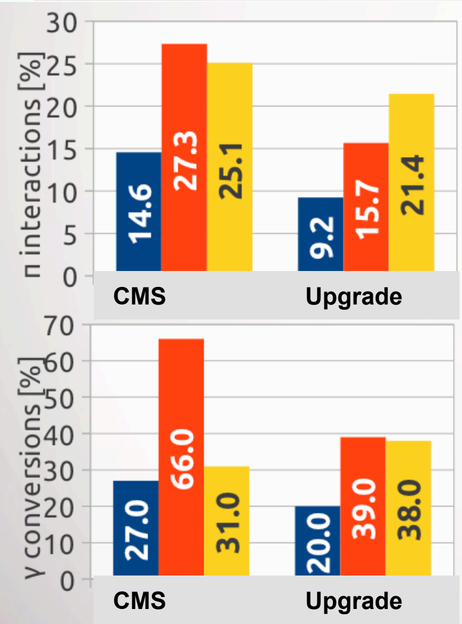
- Summarize results in three rapidity regions



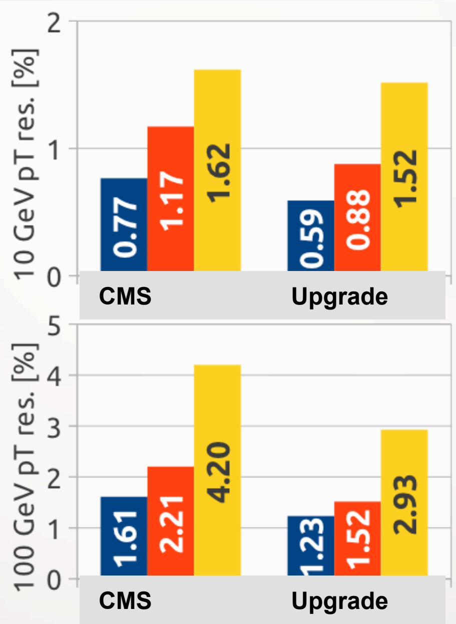
Example of layout



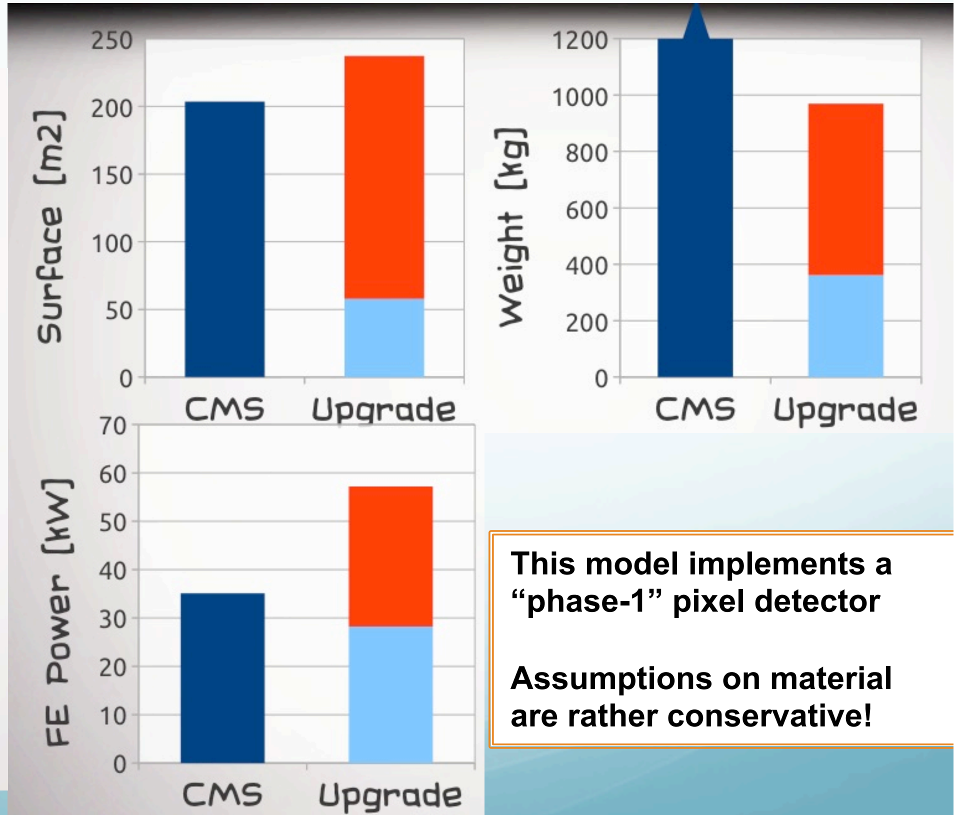




Particle interactions



Tracking resolution

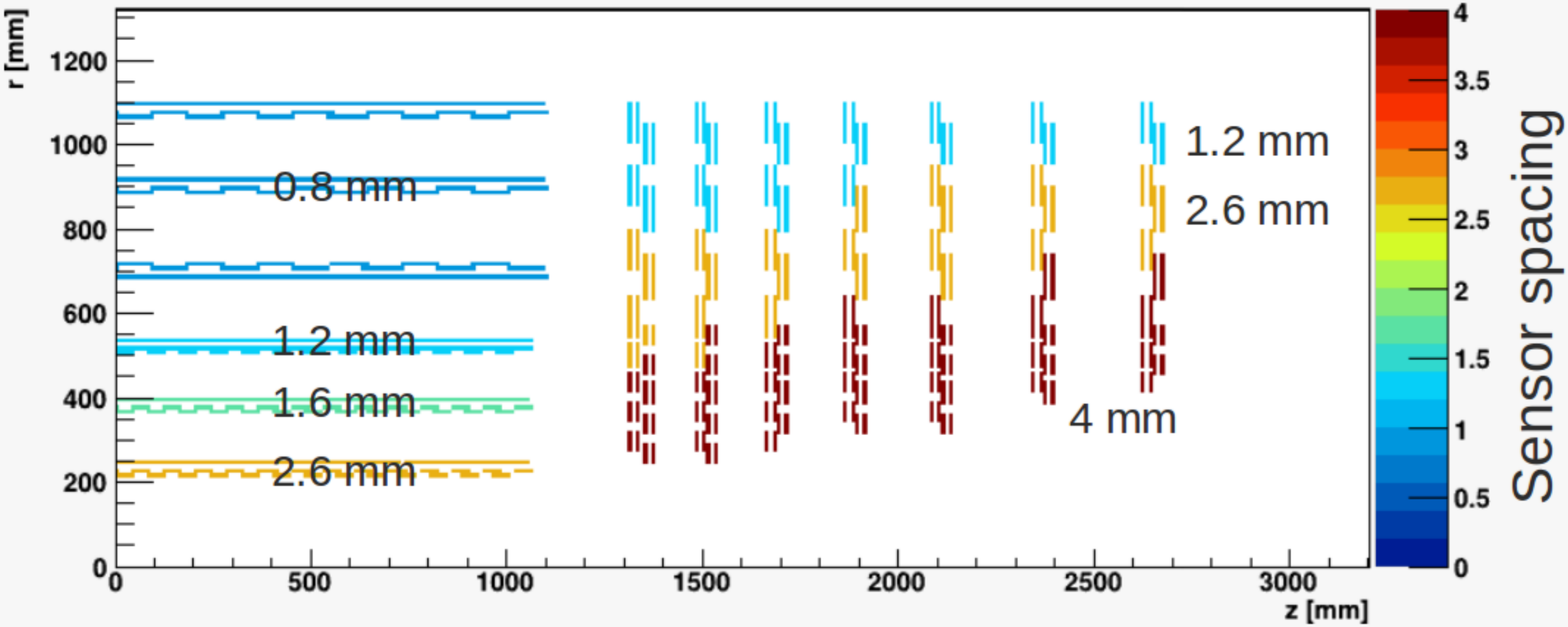


This model implements a "phase-1" pixel detector

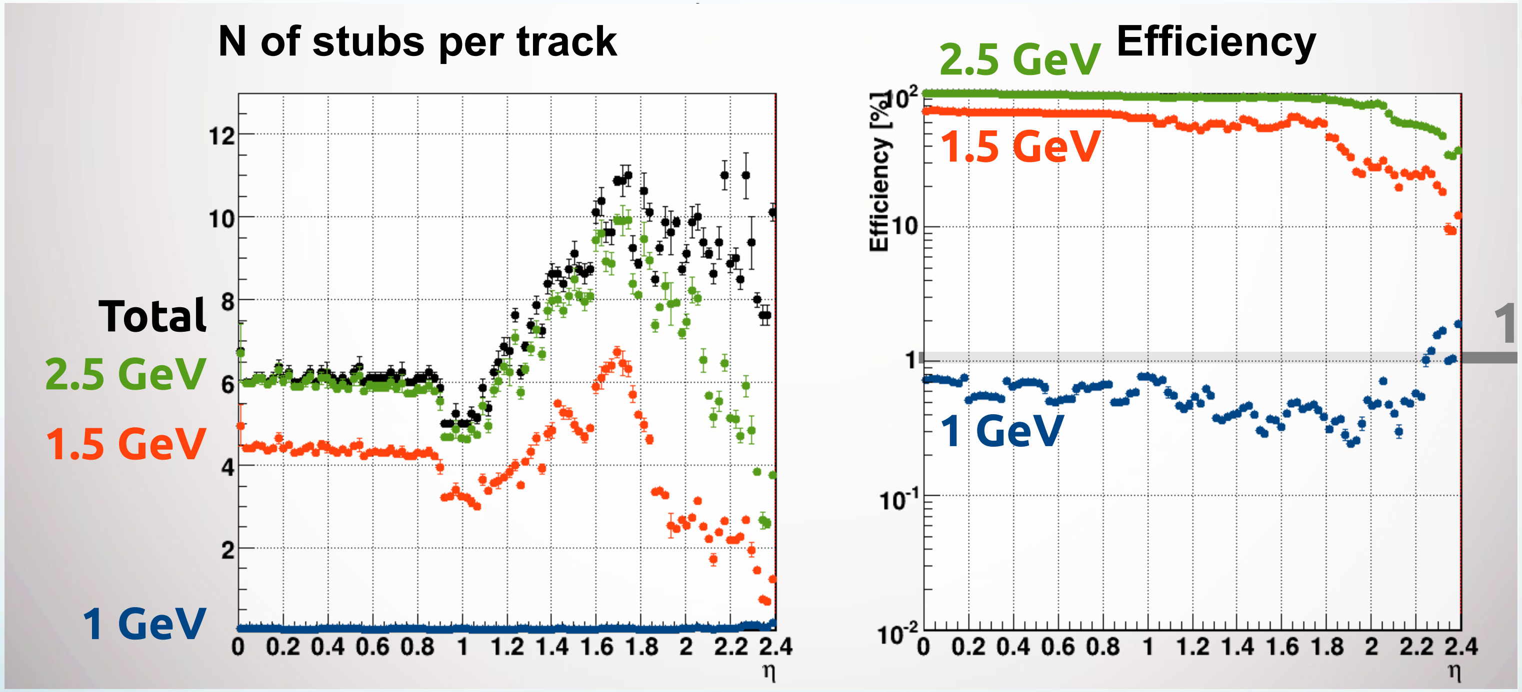
Assumptions on material are rather conservative!

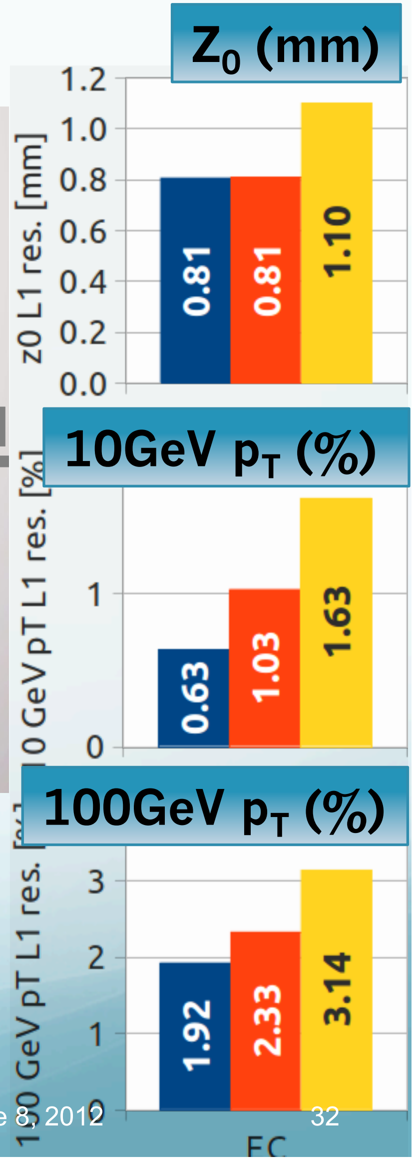
Optimization of module parameters

- Keep as ideal targets:
  - <1% efficiency @ p_T = 1GeV
  - maximize efficiency @ p_T = 2 GeV
- Limit choice of spacing to "a few" different values
- Optimize width of acceptance window at the same time
  - between 3 and 9 strips for the example below



Stub finding and L1 tracking potential (calculated)



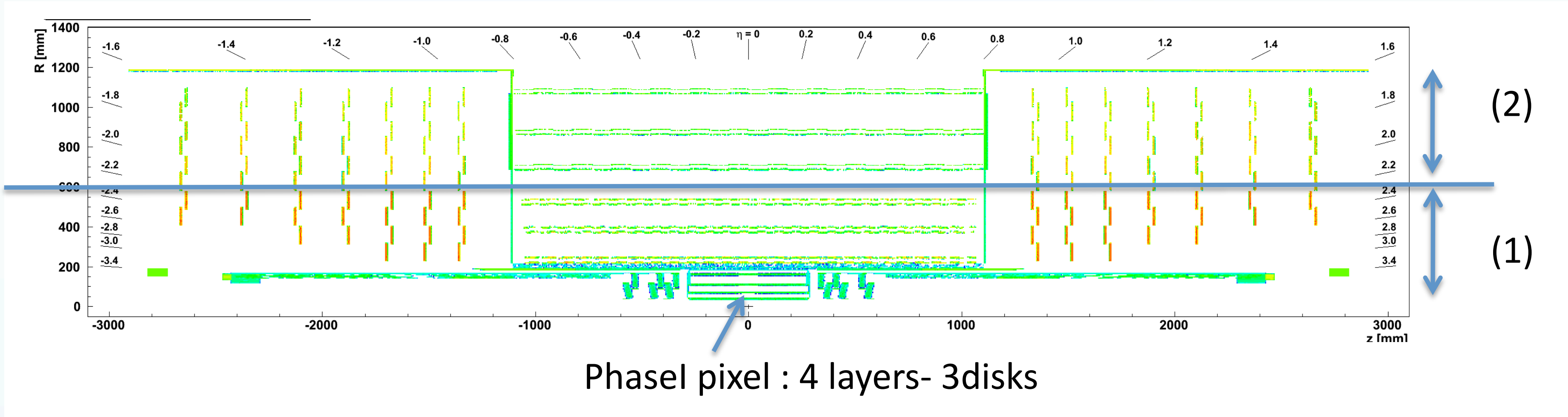


From layout modelling to CMS simulation

- The software produces also geometry files for CMS simulation and reconstruction software
  - Including material modelling
    - Some “features” still to be fixed
- CMS software needs then to be “adapted” to work with the new geometry
  - Full automatization for any possible geometry not really feasible….
- Will be used to keep geometry and material up-to-date once the overall layout is chosen

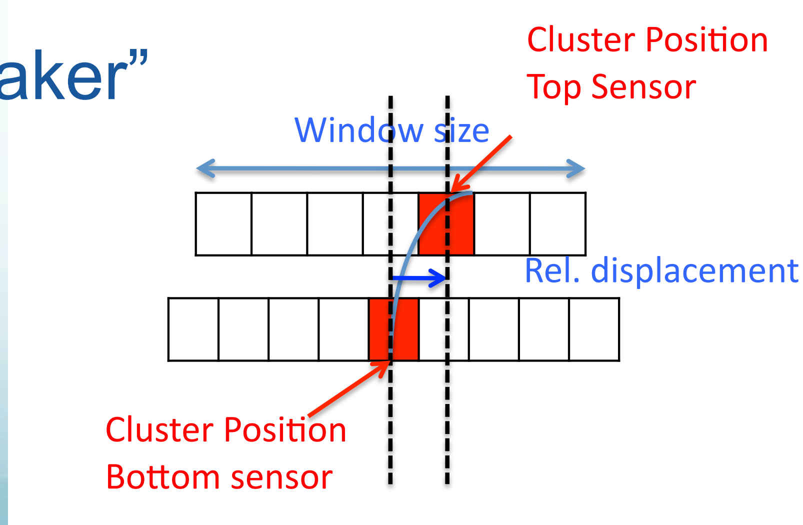
Stub finding in simulation

➢ Previous layout in CMS simulation



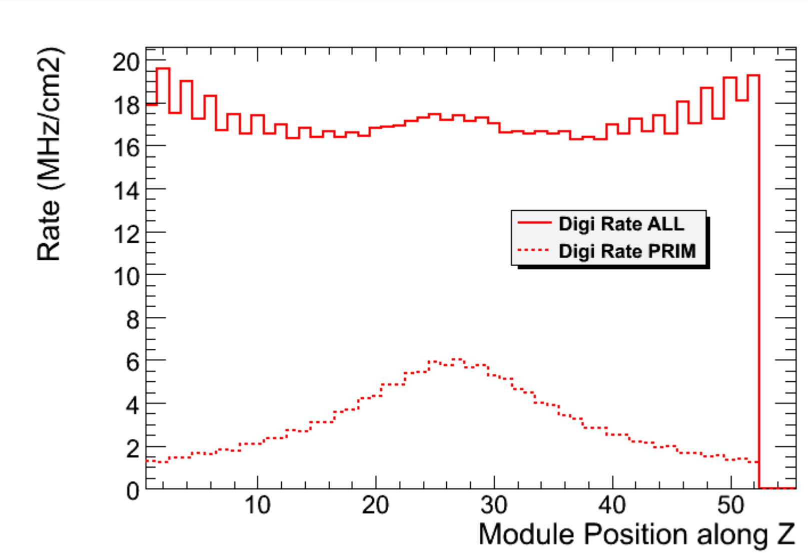
➢ Digitizer, clusterizer, "stub maker"

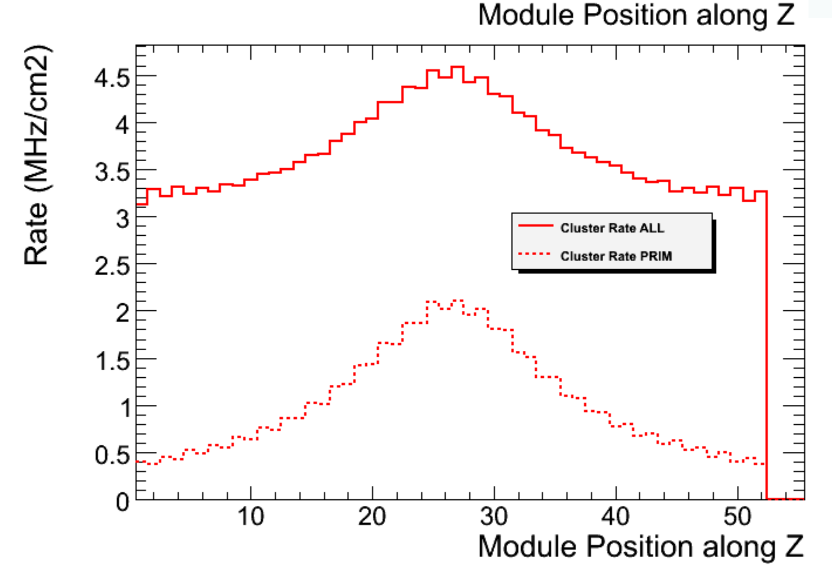
- Meant to be realistic
  - ★ To be reviewed
  - ★ All results "fresh and preliminary"

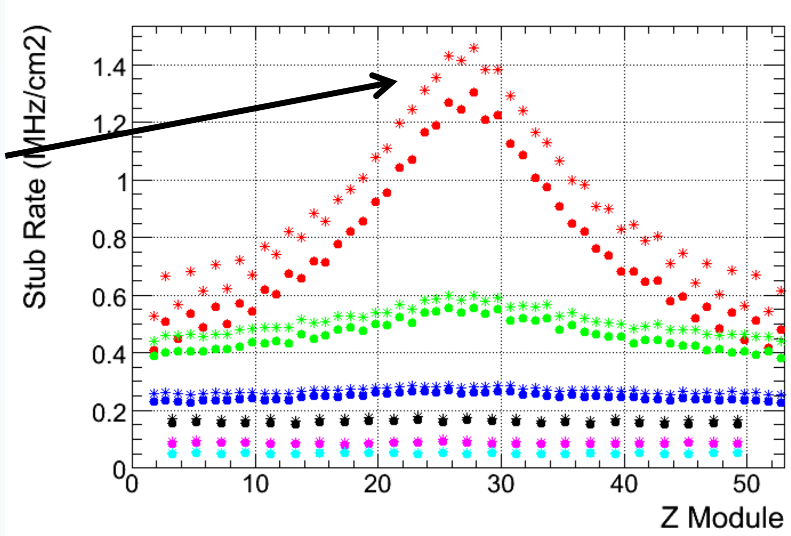


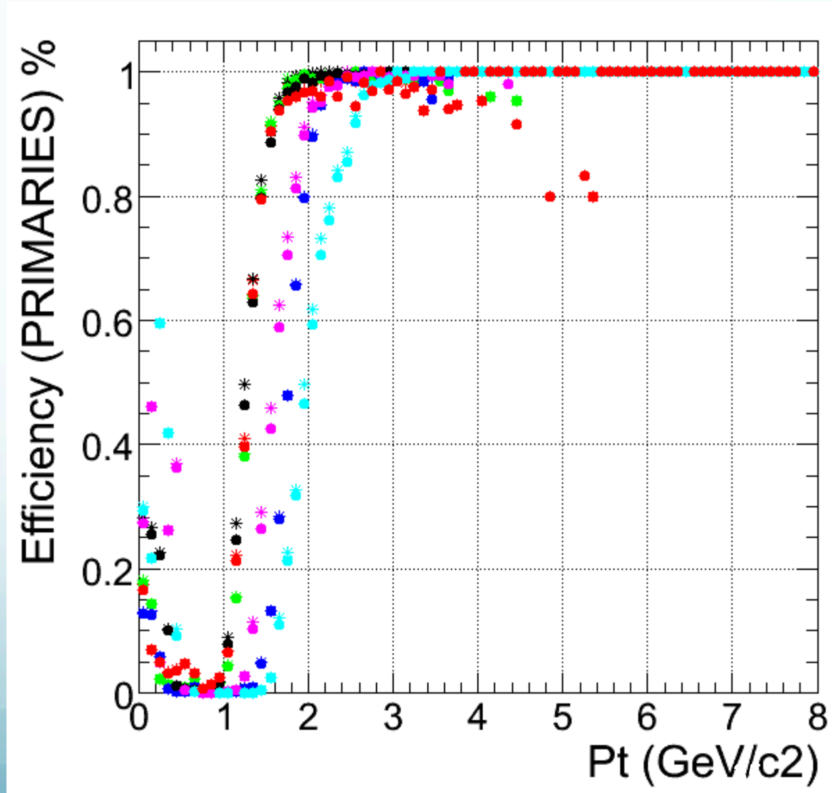
Stub finding

- Barrel layer 1 @ 23 cm, sensor spacing 2.6 mm









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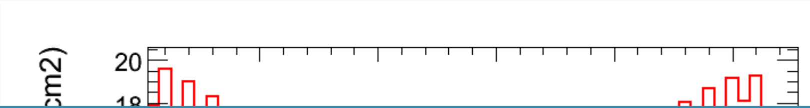
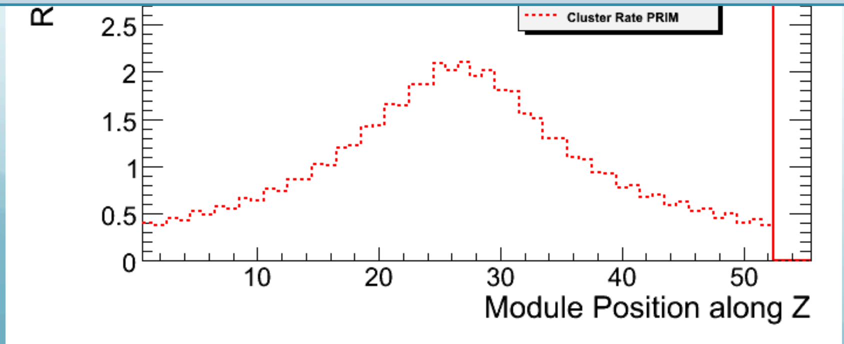
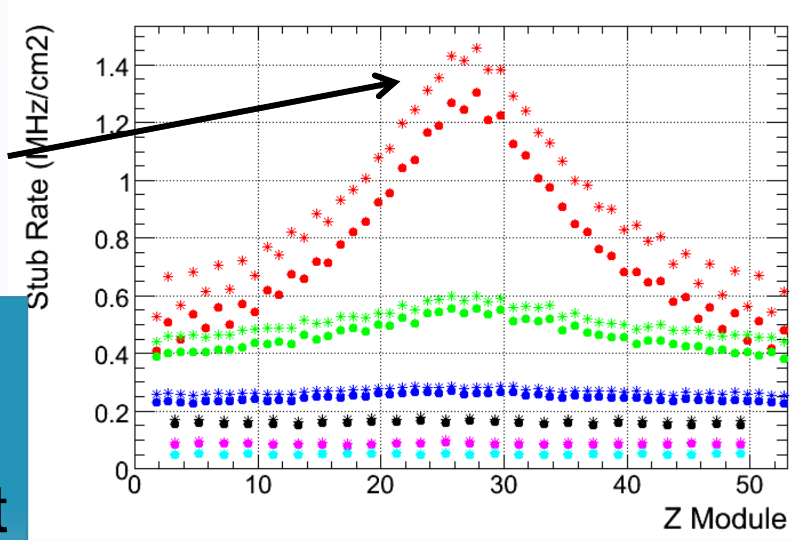
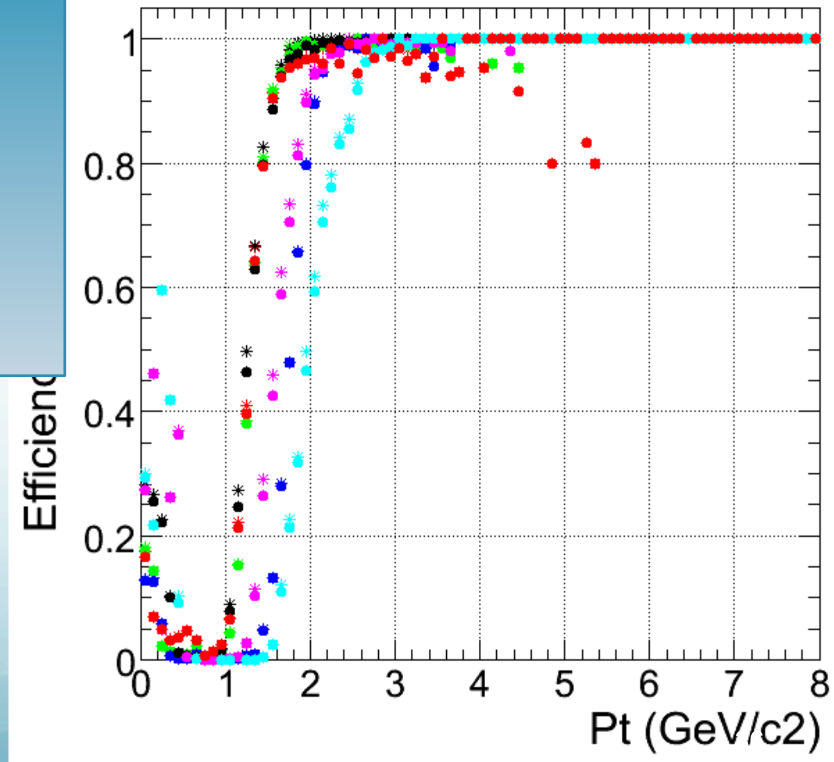


- Good performance for p_T > 2 GeV
  - This was the target
- Estimated average stub rate in worst case ~ 1.5 / module / 25 ns
  - Cfr peak:
    - 6 / chip
    - 7 / module
  - Average:
    - 3 / module
  - Margin for further improvements!





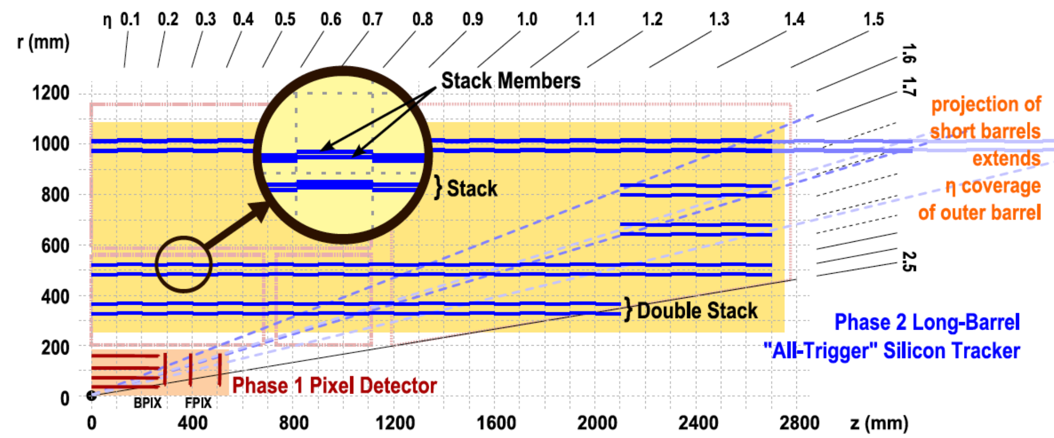


Status and outlook

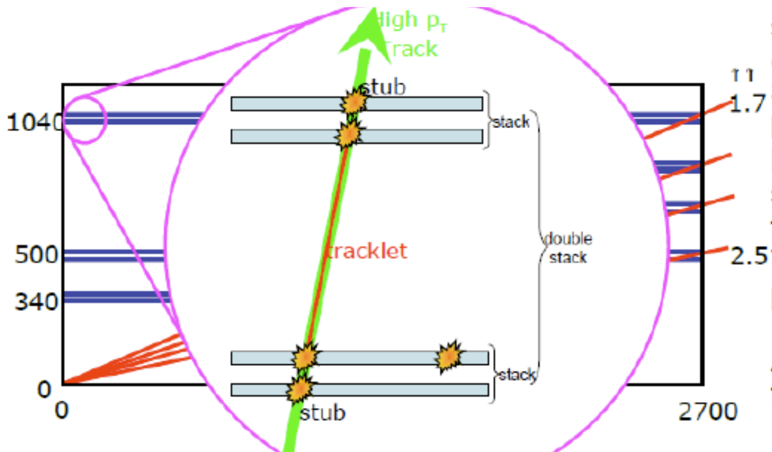
- Indications that data reduction and stub finding work rather well even in the worst-case location
- p_T modules can be used down to $\gtrsim$ 20 cm, with relatively large sensor spacing
- Tuning from layout modelling validated
  - End cap still to be checked
- N.B. Stub rates are a crucial input for the design of the electronics system!
  - Studies to be pursued. Digitizer, clusterizer and front-end logic to be developed coherently with electronics (and sensors) R&D
- No concept, so far, to go from stubs to L1 tracks with this layout
  - But work is now ongoing…

Optimized layout of L1 track finding

➢ The "long-barrel" double-stack layout

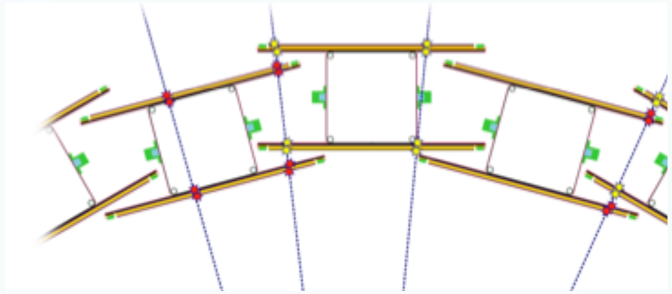


6 long layers = 3 Super layers



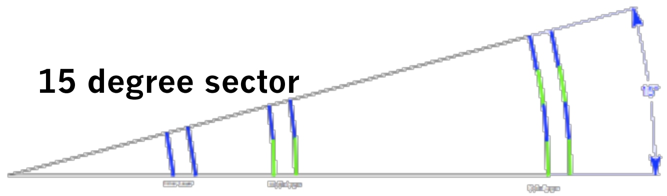
Pairs of stubs are combined to form "tracklets"

ϕ arrangement within double-stack layer



Common supporting mechanics

Self-contained ϕ sectors.
Each sector needs to be combined with the two neighbouring sectors (left and right) to "contain" ~2.5 GeV tracks.

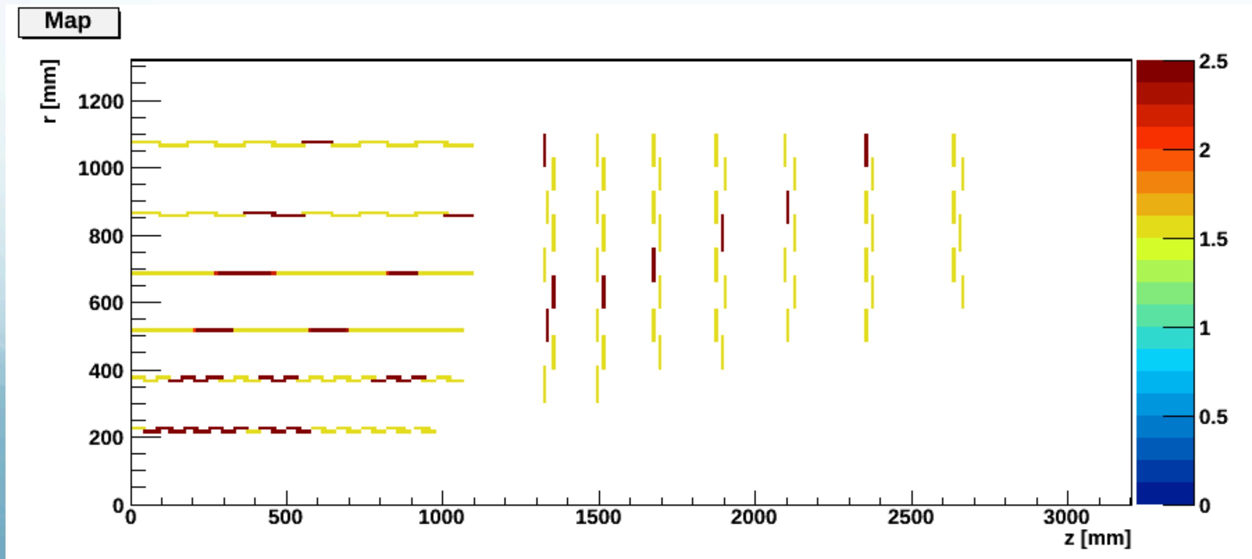


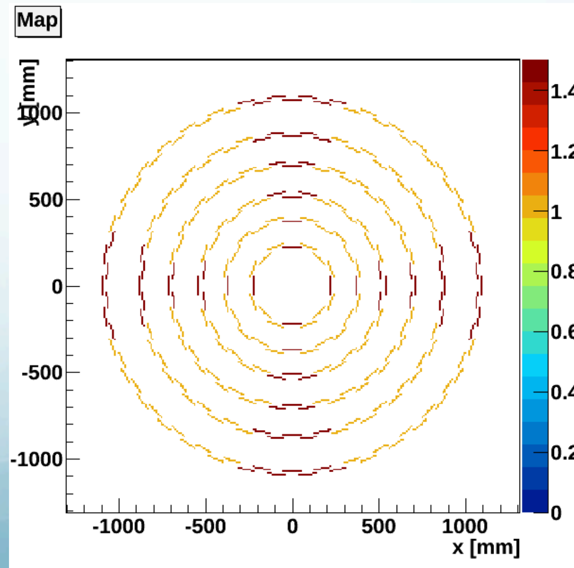
Stubs, Tracklets, L1 Tracks

- Hierarchical logic to find L1 tracks
  - Within double-stack, each lower module is combined with two upper modules to form Tracklets
    - Geometry helps to keep problem “local”
  - Tracklets in each layer are extrapolated to the other two layers
    - Possible to find a track if there is at least one tracklet
      - N.B. in this layout also the outermost layer is pixellated!
        - Impact on power and cost!
  - Remove duplicates
- Concept appears to be feasible
- Only defined strategy to deliver L1 tracks so far
- Data reduction, stub and tracklet rates verified in CMS simulation and reconstruction

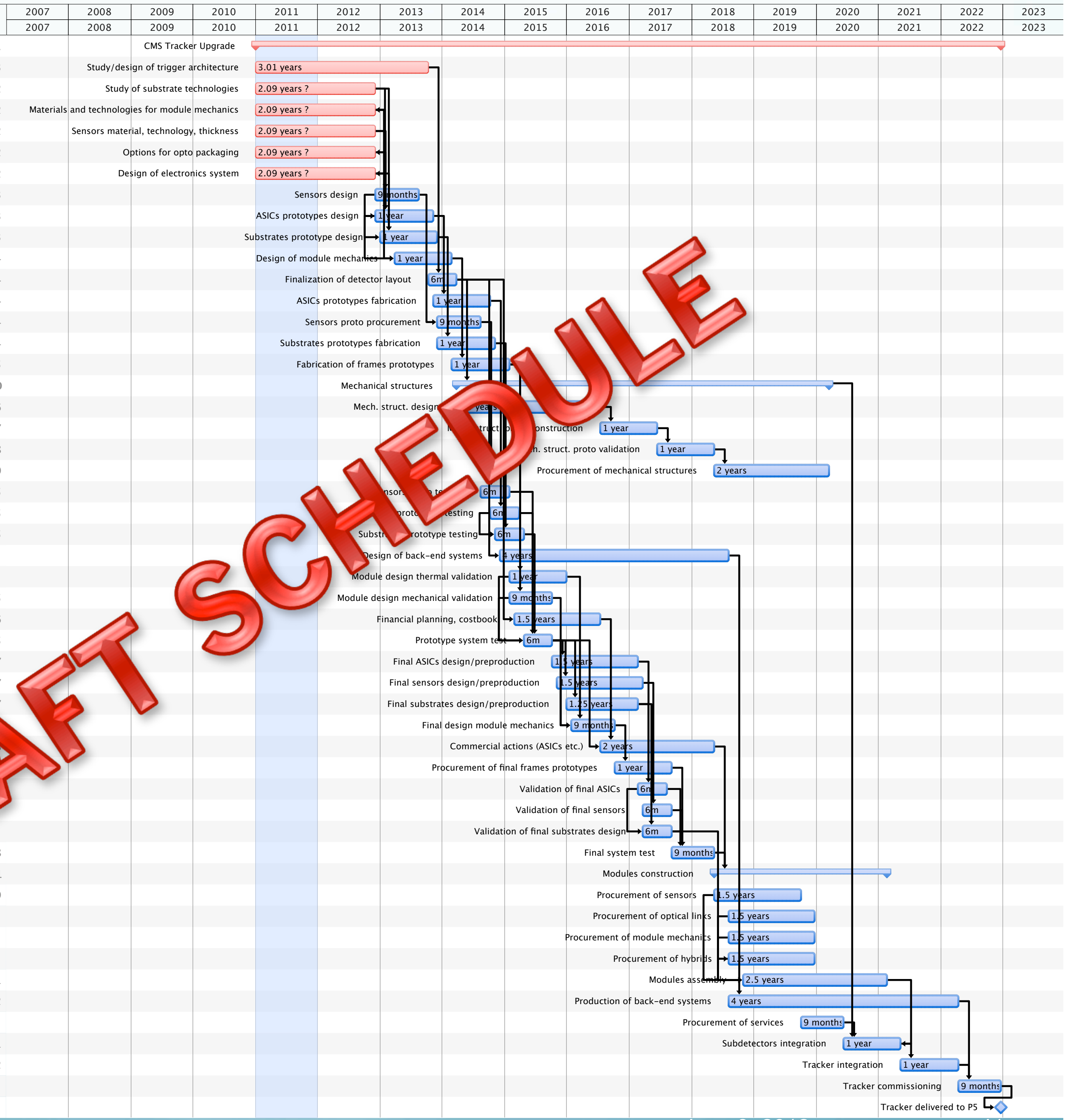
Alternative approach to L1 tracks

- Pattern matching in a generic layout
  - Associative Memories successfully used in CDF
  - Will be used for the ATLAS FTK
    - ★ At Level-2!
  - Applicable to our case?
- Work started, a few groups interested
- Started looking also into "data formatting"
  - I.e. How you get the all the needed data in a given back-end crate of processors





#	Info	Title	Flag Status	# Predecessors	Expected Start	Expected End
0		**CMS Tracker Upgrade**			1/1/11	12/21...
2		Study/design of trigger architecture			1/1/11	10/9/13
32		Study of substrate technologies			1/3/11	12/4/12
38		Materials and technologies for module...		32FF	1/3/11	12/4/12
34		Sensors material, technology, thickness			1/3/11	12/4/12
33		Options for opto packaging		38FF	1/3/11	12/4/12
37		Design of electronics system		38FF	1/3/11	12/4/12
35		Sensors design		34	12/5/12	8/13/13
40		ASICs prototypes design		33; 3...	12/5/12	11/5/13
16		Substrates prototype design		32; 3...	1/2/13	12/3/13
39		Design of module mechanics		38; 4...	3/27/13	2/25/14
3		Finalization of detector layout		2	10/9/13	3/25/14
45		ASICs prototypes fabrication		40	11/6/13	10/7/14
36		Sensors proto procurement		35	12/4/13	8/12/14
17		Substrates prototypes fabrication		16	12/4/13	11/4/14
41		Fabrication of frames prototypes		39	2/26/14	1/27/15
27		**Mechanical structures**		3	3/26/14	3/17/20
29		Mech. struct. design			3/26/14	7/12/16
30		Mech. struct. proto construction		29	7/13/16	6/13/17
31		Mech. struct. proto validation		30	6/14/17	5/15/18
28		Procurement of mechanical structures		31	5/16/18	3/17/20
18		Sensors proto testing		36	8/13/14	1/27/15
42		ASICs prototypes testing		45	10/8/14	3/24/15
10		Substrates prototype testing		17; 4...	11/5/14	4/21/15
25		Design of back-end systems		3	12/3/14	8/7/18
43		Module design thermal validation		41	1/28/15	12/29...
44		Module design mechanical validation		41	1/28/15	10/6/15
11		Financial planning, costbook		3	2/25/15	7/12/16
13		Prototype system test		10; 1...	4/22/15	10/6/15
8		Final ASICs design/preproduction		13	10/7/15	2/21/17
14		Final sensors design/preproduction		13	11/4/15	3/21/17
5		Final substrates design/preproduction		13	12/30/15	2/21/17
6		Final design module mechanics		13; 4...	1/27/16	[illegible]
12		Commercial actions (ASICs etc.)		11; 13	7/13/16	[illegible]
7		Procurement of final frames prototypes		6	[illegible]	[illegible]
9		Validation of final ASICs		5; 8	[illegible]	[illegible]
15		Validation of final sensors			[illegible]	[illegible]
1		Validation of final substrates design		5; 9SS...	[illegible]	9/5/17
4		Final system test		[illegible]	[illegible]	5/15/18
19		**Modules construction**			[illegible]	2/16/21
23		Procurement of sensors			5/16/18	10/1/19
22		Procurement of optical links			8/8/18	12/24...
21		Procurement of module mechanics			8/8/18	12/24...
20		Procurement of hybrids		1	8/8/18	12/24...
24		Modules assembly		20SS...	10/31/18	2/16/21
26		Production of back-end systems		25	8/8/18	4/12/22
46		Procurement of services			10/2/19	6/9/20
48		Subdetectors integration		24FF...	6/10/20	5/11/21
50		Tracker integration		48FS+0	5/12/21	4/12/22
47		Tracker commissioning		26; 5...	4/13/22	12/20...
49		Tracker delivered to P5		47	12/21/22	12/21...



Simplified excel version

R&D and concepts for front-end systems
Study of substrate technologies
Materials and technologies for module mechanics
Sensors material, technology, thickness
Options for opto packaging
Definition of electronics system

ASICs, Sensors, Substrates, Frames
Design and fabrication of prototypes
Prototype test/qualification
System test
Final design / preproduction
Qualification
Final system test

Study/design of trigger architecture

Finalization of detector layout

Financial planning, costbook
Commercial actions (ASICs etc..)

Mechanical structures
Design
Prototype construction
Prototype validation
Procurement

Modules construction

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Production

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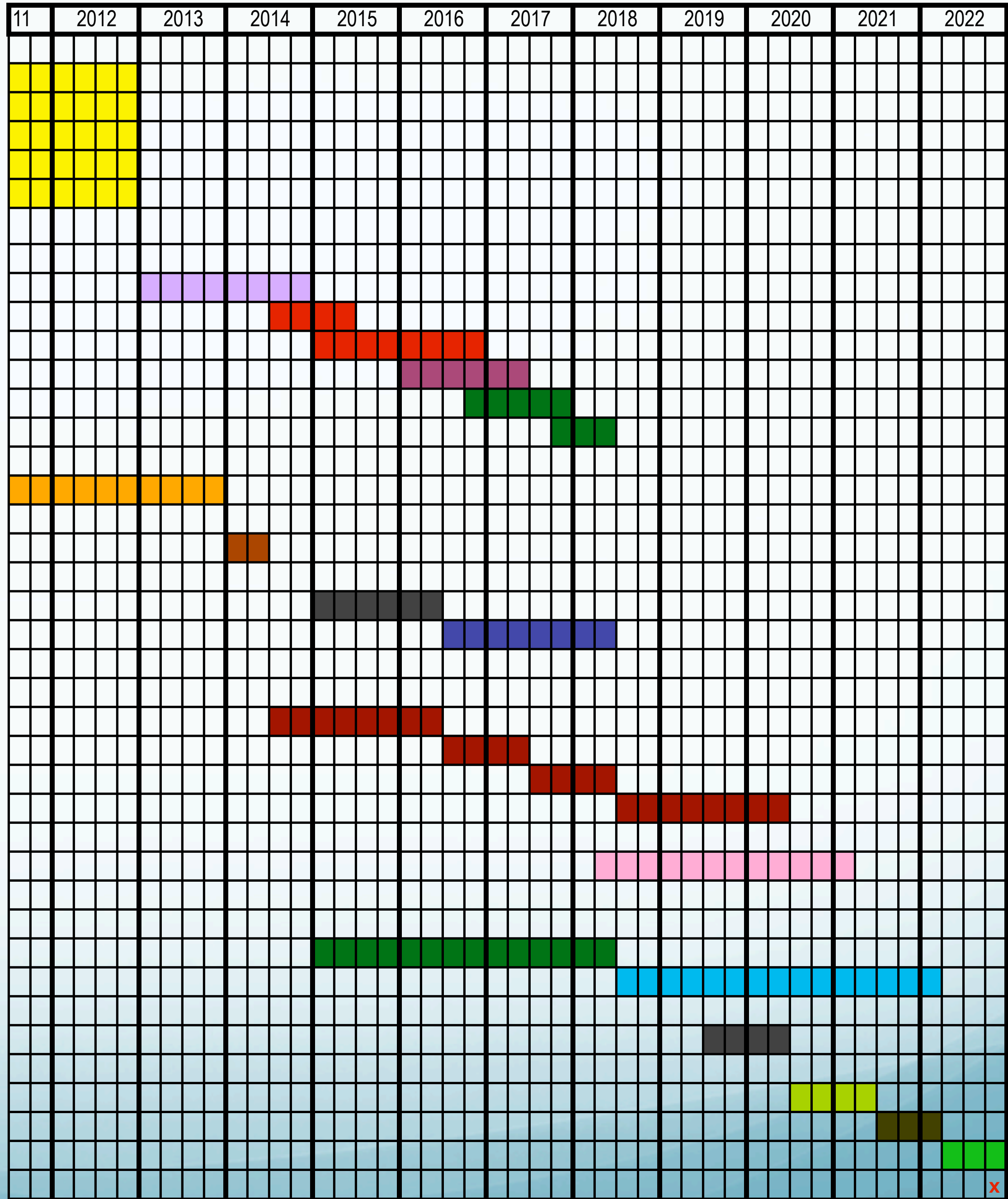

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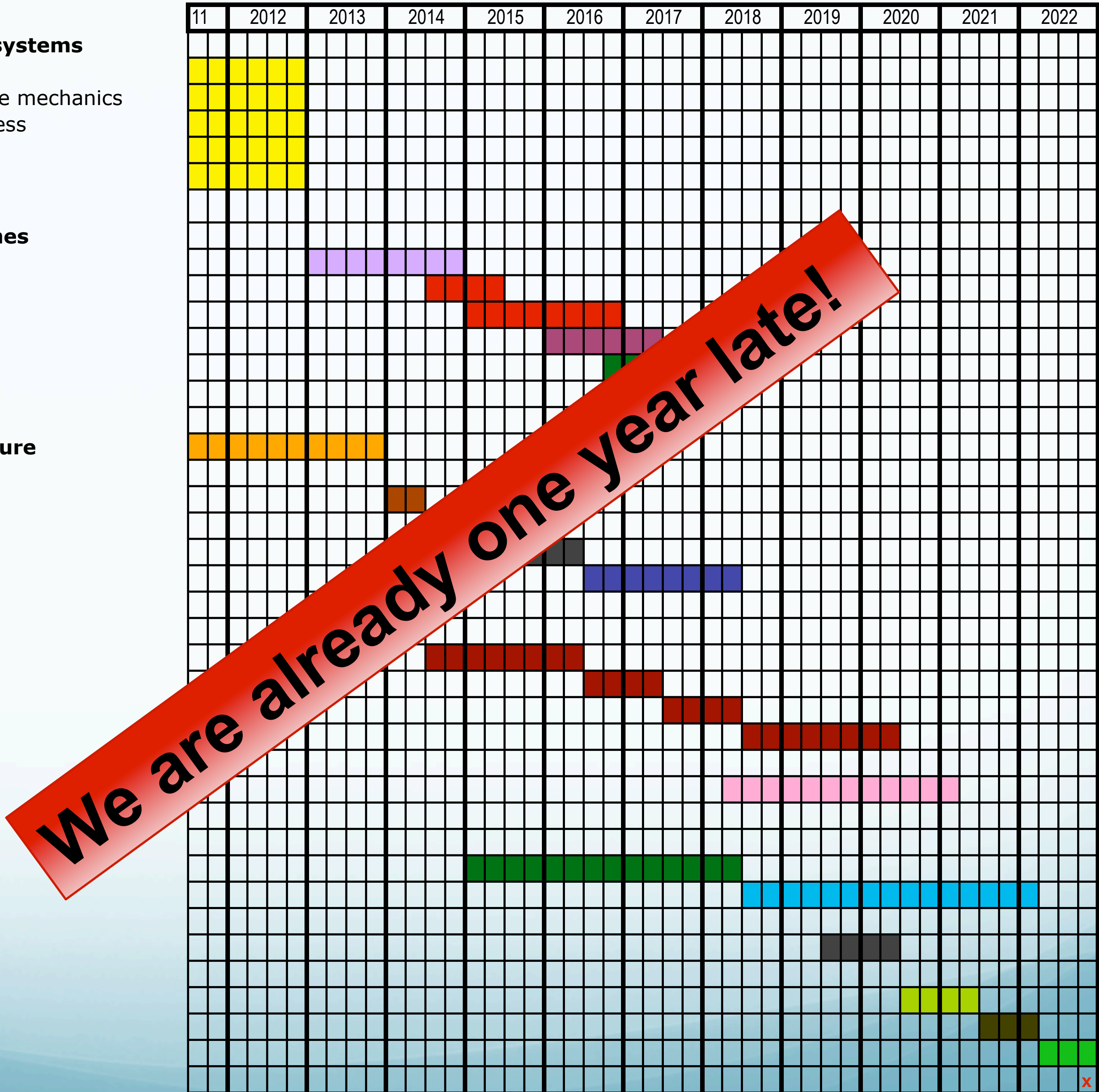

Phase 2 pixel

- The phase-1 pixel detector is not the CMS ultimate pixel
- Construction time is shorter, ~ 2 more years to converge on a design compared to the outer tracker
- Discussions started; convergence on some basic concepts
  - Aiming at a significantly smaller pixel size. Possibly as small as 30×100 μm^2?
  - 65 nm seems to be a good technology choice
    - Strong technology node, likely to be available for very long
    - Can squeeze 4× digital logic in same area wrt 130 nm
  - Thin planar sensors with small pixels could be a robust baseline
  - 3d silicon very appealing option with potentially excellent performance
  - Diamonds the ultimate radiation hardness? Production and cost still an issue
    - In any case low signal requires a chip with low threshold
  - Several important system issues need to be addressed
    - Synergies with Outer Tracker are necessary, but differences are relevant
- Sketch of a 5-year development plan defined
  - Should yield choice of sensor technology, and design of readout chip
  - Interested groups gathering together

Phase 2 pixel

- A major question is, again, the trigger
  - Local data reduction is not viable below 20 cm
  - Regional readout is probably the way to go, if needed

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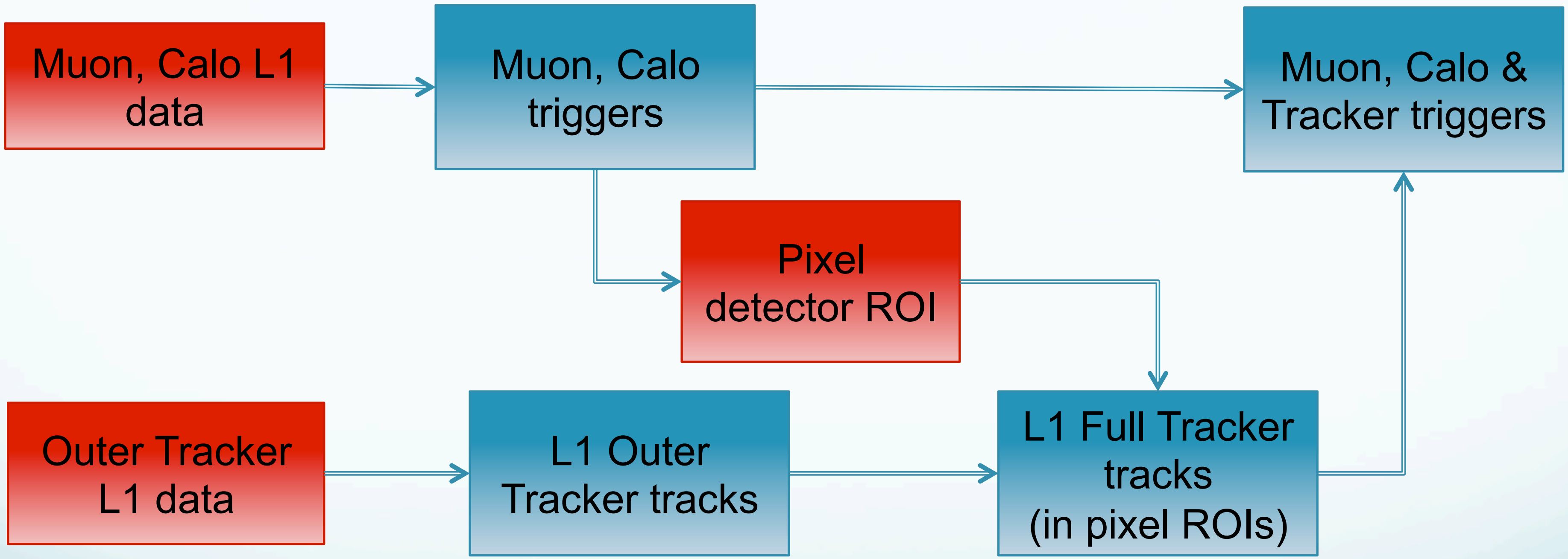

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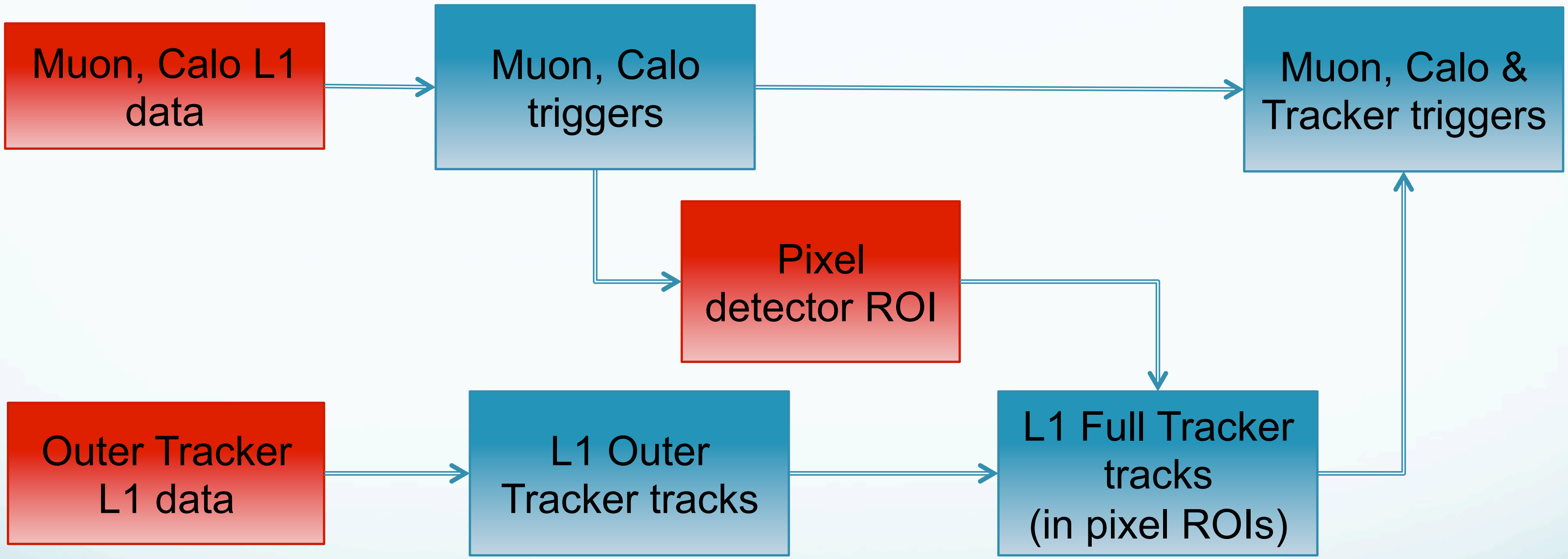


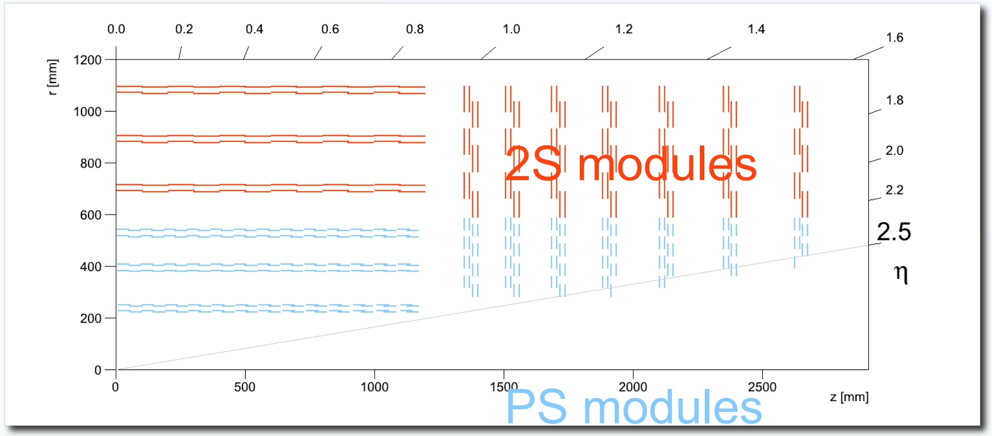
- Would provide precise PV determination @ Level-1
  - From < 1 mm with outer tracker to < 100 μm with pixels
  - But it's just a cartoon for the time being…!
    - ★ Is the latency enough?!?

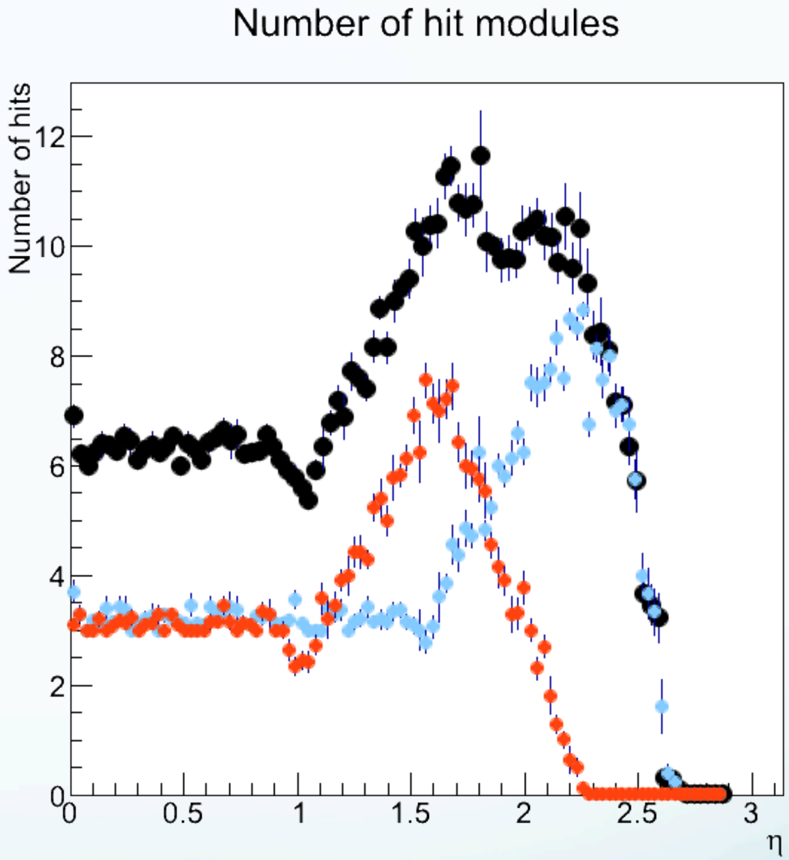
Summary and outlook

- Designing an Outer Tracker with:
  - Higher granularity
  - Enhanced radiation hardness
  - Improved tracking performance (i.e. lighter!)
  - L1 Track finding capability
    - Reconstruct tracks above ~ 2.5 GeV
    - With ~ 1mm z_0 resolution
- All the necessary R&D activities are ongoing
- Still far from a fully defined concept
  - But a lot of progress has been made already
  - Encouraging indications that the goals could be met
  - Need to converge on an optimal design in the next ~ 2 years
- Draft schedule developed for delivery in LS3
- Phase 2 pixel project on the starting blocks
  - Development plan for the next 5 years being defined
- A lot of interesting and creative work: newcomers most welcome!

Backup

Layout properties



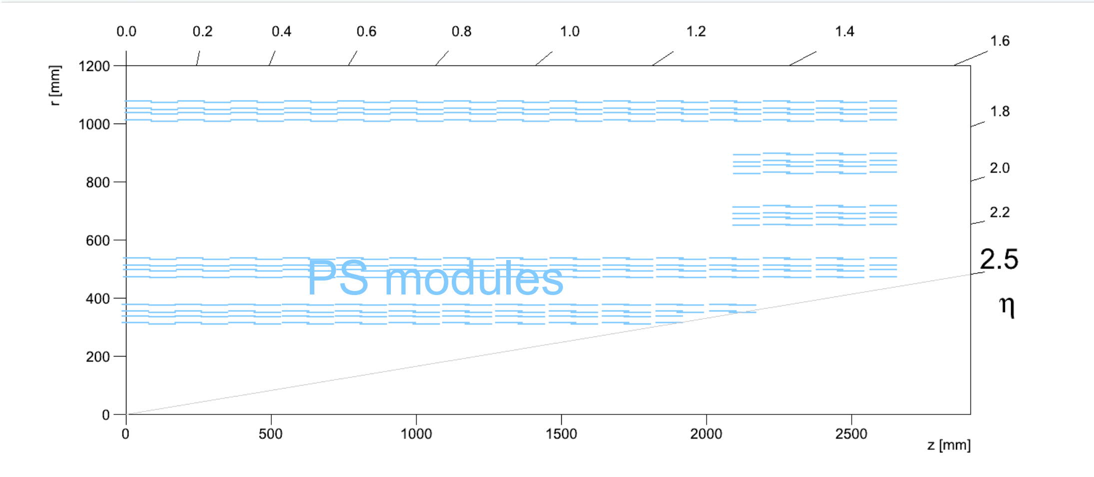


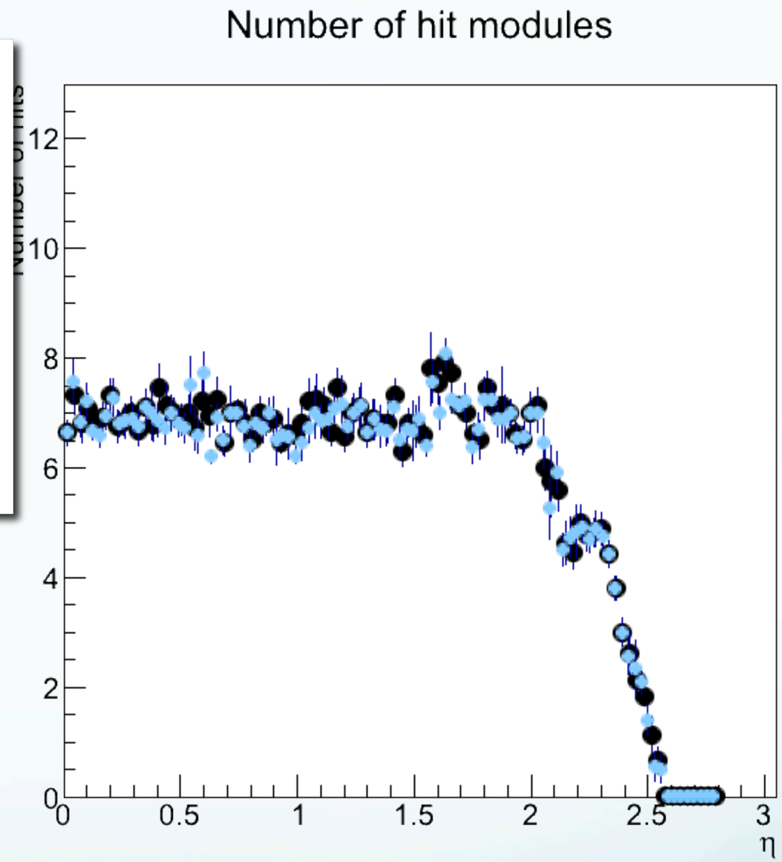
	CMS	A
Barrel layers	10	6
Endcap layers	9	7
Number of fibers	~ 41 k	~ 34 k

Geometry optimized for tracking: end-cap modules, no double-stacks, ...

Less layers to reduce material (improves p_T resolution at low p)

Layout properties

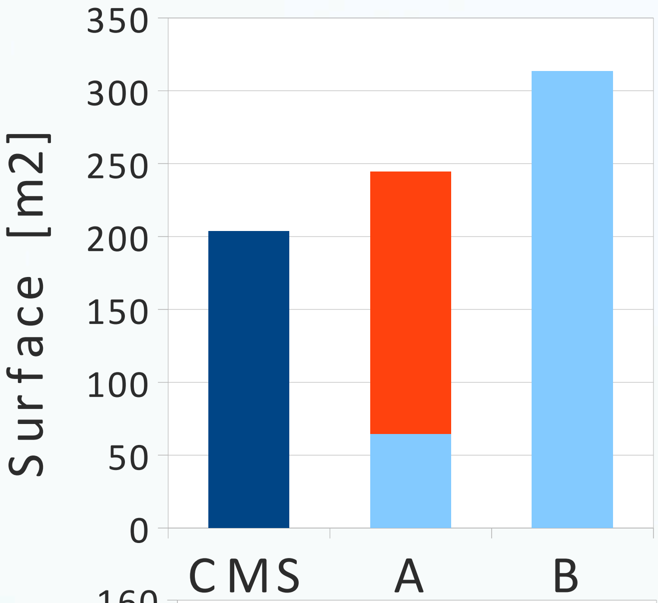


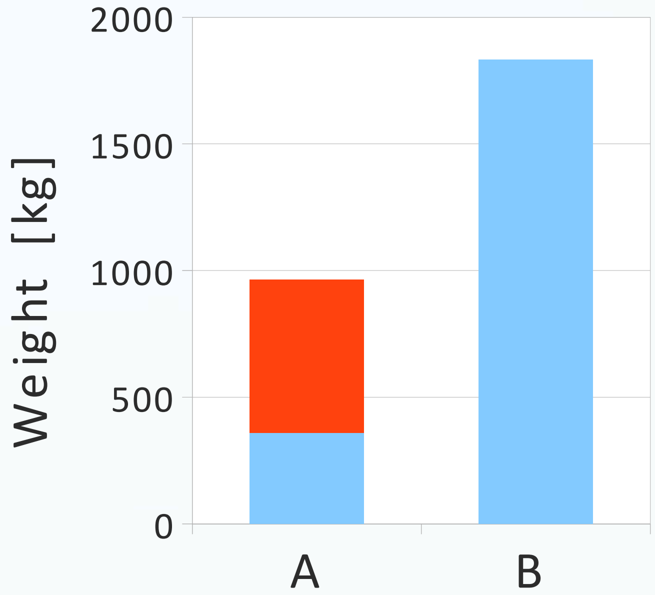


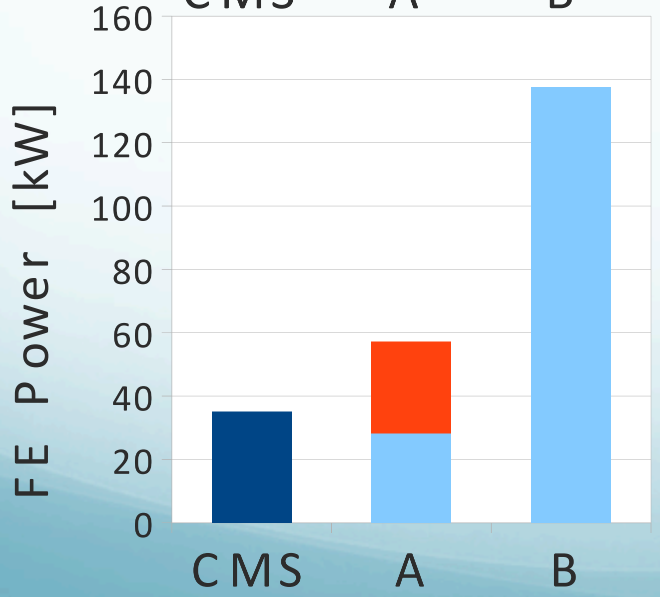
	CMS	B
Barrel layers	10	6
Endcap layers	9	N/A
Number of fibers	~ 41 k	~ 35 k*

Geometry optimized for track-trigger: long barrel, double-stacks, ...
All pixellated modules (modelled as twice a PS module)
* Assuming one GBT/module of 10x10 in the first layers

Surface, power, weight, ...



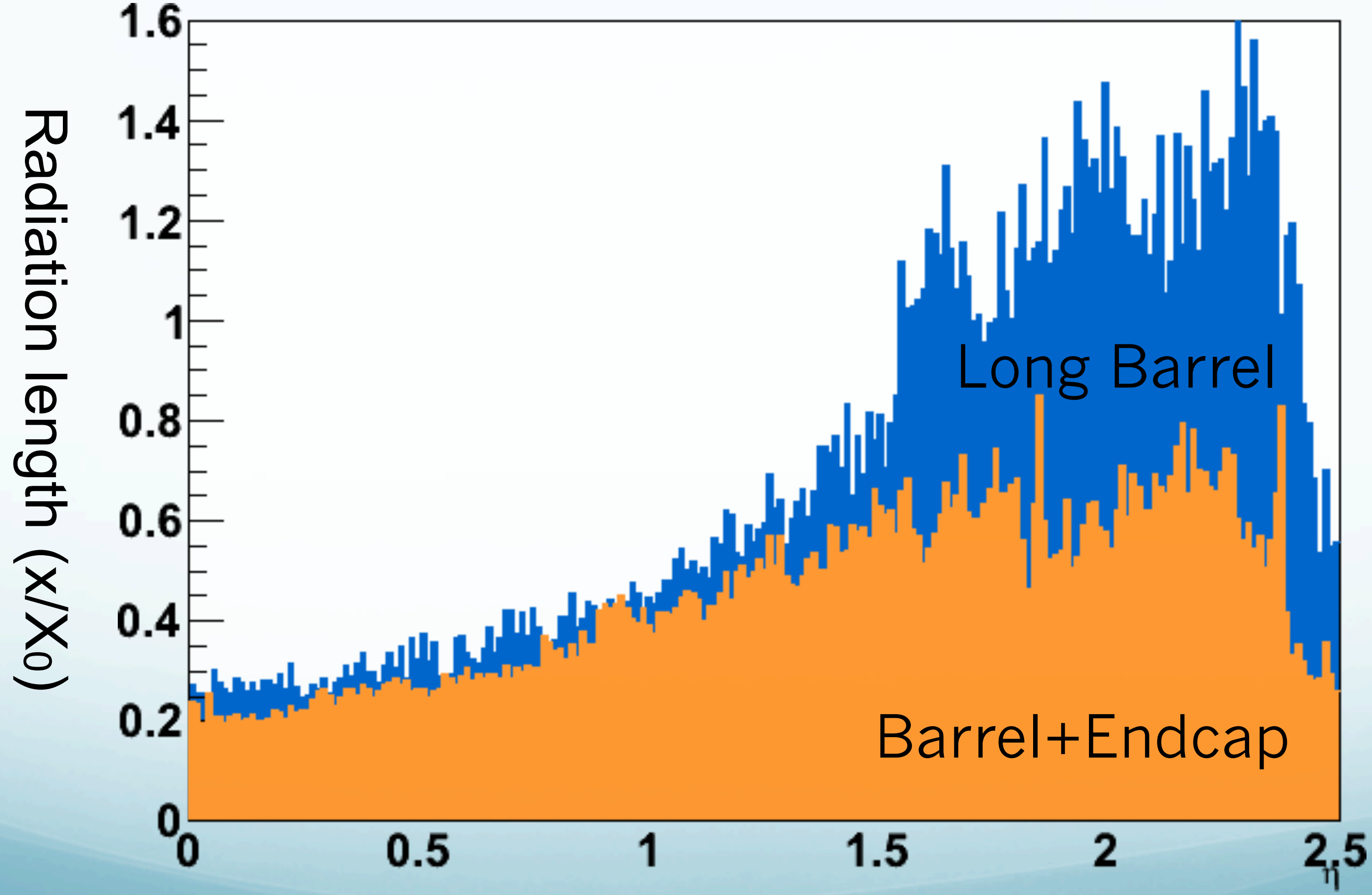




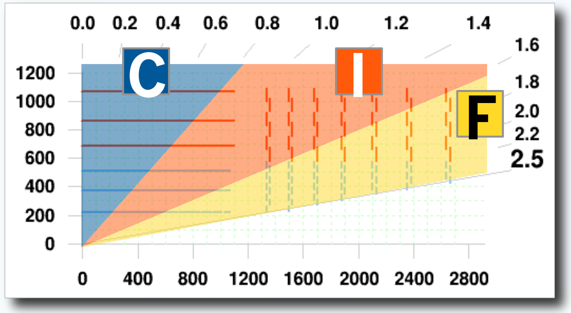
A: 1 front-end + 1 DC/DC
+ 1 correlator + 1 GBT
10 x 5 cm^2 1.5 mm long pixels

B: 2 front-end + 2 DC/DC
+ 1 correlator + 1 GBT
10 x 10 cm^2 1 mm long pixels

Material budget comparison



Performance comparison

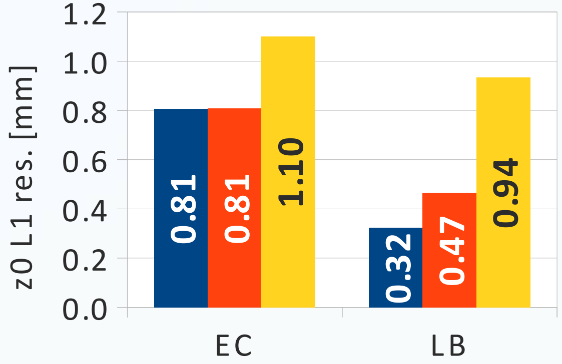


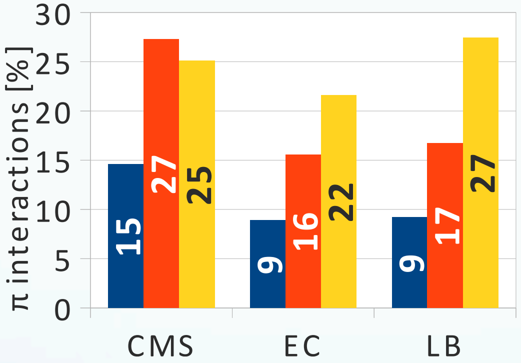
η

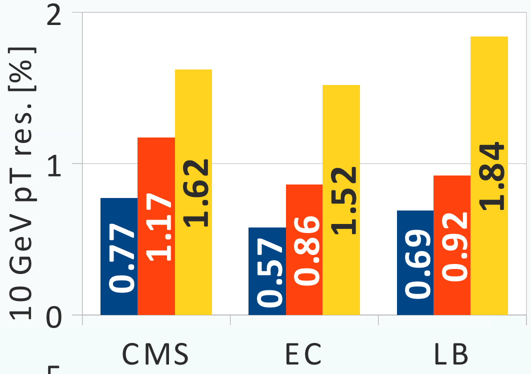
C $0 \rightarrow 0.8$

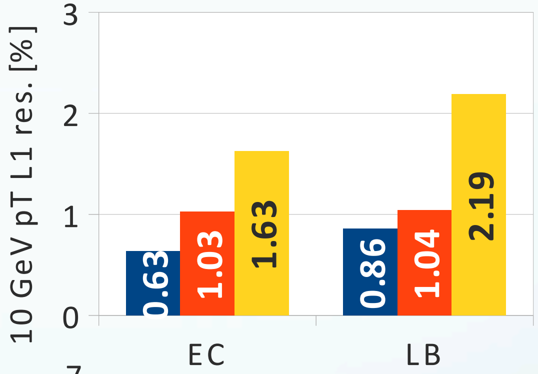
I $0.8 \rightarrow 1.6$

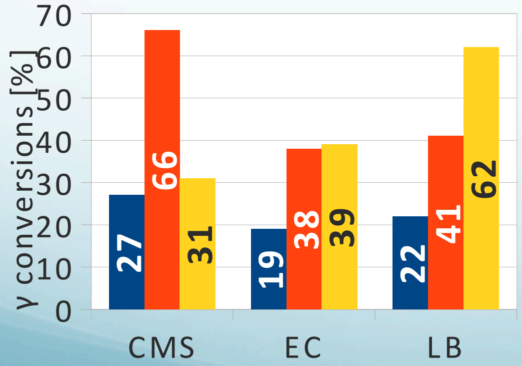
F $1.6 \rightarrow 2.4$

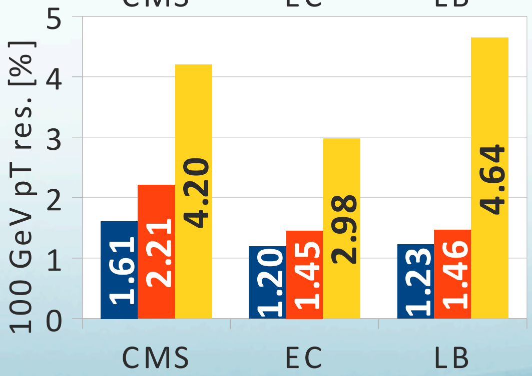


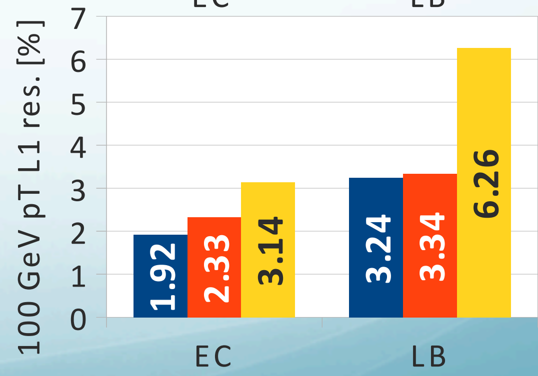












Particle interactions

Tracking resolution

Trigger resolution