Development of ASICs for forward calorimetry in future linear collider

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Outline

- Introduction to forward detectors in ILC/CLIC
- Front-end electronics signal processing
  - Noise, Preamplifier, Shaper, S/N and ENC, ADC
- Core ASICs and signal processing for LumiCal Detector
  - Preamplifier-Shaper ASIC
  - Pipeline ADC ASIC
  - Readout with deconvolution
- Integration of Complex Readout System for LumiCal
  - Peripheral blocks for multichannel system
  - Multichannel Digitizer ASIC
  - Prototype multichannel readout system
- Developments in progress...
**LumiCal Detector in ILD**

- **Aim:** Precise measurement of integrated luminosity (based on counting BhaBha events)
- **Construction:** sampling calorimeter
  - 30 (ILC) / 40 (CLIC) layers Si/W

*H. Abramowicz et al., "Forward Instrumentation for ILC Detectors" JINST 5:P12002, 2010*
### LumiCal baseline design

<table>
<thead>
<tr>
<th>Parameter</th>
<th>ILC</th>
<th>CLIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Absorber material</td>
<td>Tungsten</td>
<td>Tungsten</td>
</tr>
<tr>
<td>Absorber thickness[mm]</td>
<td>3.5</td>
<td>3.5</td>
</tr>
<tr>
<td>Sensor [µm]</td>
<td>Si 300</td>
<td>Si 300</td>
</tr>
<tr>
<td>R inner [mm]</td>
<td>80</td>
<td>100</td>
</tr>
<tr>
<td>R outer [mm]</td>
<td>195.2</td>
<td>290</td>
</tr>
<tr>
<td>Θ inner [mrad]</td>
<td>31</td>
<td>37</td>
</tr>
<tr>
<td>Θ outer [mrad]</td>
<td>78</td>
<td>110</td>
</tr>
<tr>
<td>Z pos [mm]</td>
<td>2500</td>
<td>2654</td>
</tr>
<tr>
<td>Layers</td>
<td>30</td>
<td>40</td>
</tr>
<tr>
<td>Mass [kg]</td>
<td>210</td>
<td>660</td>
</tr>
</tbody>
</table>
## Linear Collider Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>ILC</th>
<th>CLIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Centre-of-mass energy (GeV)</td>
<td>500</td>
<td>500</td>
</tr>
<tr>
<td>Total (Peak 1%) luminosity ($10^{34}$)</td>
<td>2.0(1.5)</td>
<td>2.3(1.4)</td>
</tr>
<tr>
<td>Total site length (km)</td>
<td>31</td>
<td>13.0</td>
</tr>
<tr>
<td>Loaded accel. gradient (MV/m)</td>
<td>31.5</td>
<td>80</td>
</tr>
<tr>
<td>Main linac RF frequency (GHz)</td>
<td>1.3 (Super Cond.)</td>
<td>12 (Normal Conducting)</td>
</tr>
<tr>
<td>Beam power/beam (MW)</td>
<td>20</td>
<td>4.9</td>
</tr>
<tr>
<td>Bunch charge ($10^9$ e+/−)</td>
<td>20</td>
<td>6.8</td>
</tr>
<tr>
<td>Bunch separation (ns)</td>
<td>330</td>
<td></td>
</tr>
<tr>
<td>Beam pulse duration (ns)</td>
<td>1000000</td>
<td>177</td>
</tr>
<tr>
<td>Repetition rate (Hz)</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>Total power consumption (MW)</td>
<td>216</td>
<td>129.4</td>
</tr>
</tbody>
</table>

Readout requirements for ILC and CLIC different:
- Synchronous with beam measurement of signal feasible at ILC
- Asynchronous amplitude and time measurement needed for CLIC
- Power pulsing feasible for ILC and CLIC
“Future” readout architecture for amplitude and time measurement

Is it possible to proceed with similar developments for ILC and CLIC?
Readout electronics requirements

- Low cost
- Low material
- Low power
- High speed
- Low noise
- High reliability
- High dynamic range
- Radiation hardness

We would like all of it, but...

Technology limitations - compromise needed!
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Readout electronics processes signals from sensors to measure:
- energy released by radiation ► spectroscopy measurements
- time of signal occurrence ► timing measurements
- position where the radiation hits the sensor ► tracking, imaging

Front-end electronics noise performance is usually expressed by the Signal to Noise (S/N) ratio (typically S/N>10 required), or even better by the Equivalent Noise Charge (ENC), e.g. charge for which S/N=1

Signal usually current, its charge in fC-pC range
Sensor usually capacitive in 0.1-100 pF range
The most often used charge sensitive preamplifier configuration integrates sensor current giving the output proportional to the charge released in the sensor and so to the deposited energy (in silicon \( \sim 3.6 \) eV per electron-hole pair).

- Preamplifier amplifies sensor signal enough so that the noise sources in following stages do not deteriorate S/N.
- Preamplifier should contribute minimum possible noise.

\[
\begin{align*}
\begin{split}
    u_{\text{out}}(t) &= \frac{Q_{\text{in}}}{C_f \left(1 + \frac{1}{A} \frac{C_f + C_{\text{in}}}{C_f}\right)} \cdot 1(t) \\
    &\quad \text{if } A \to \infty \\
    u_{\text{out}}(t) &= \frac{Q_{\text{in}}}{C_f} \cdot 1(t)
\end{split}
\end{align*}
\]

Problems: No DC bias at input, No discharge of \( C_f \).

Typical gain: \( C_f = 0.2 \) pF \( \to \) 20 mV/fC.
Charge Preamplifier

pulsed reset - continuous reset

- Reset switch allows the removal of charge from feedback capacitance $C_f$
- Charge may be removed periodically
- Drawbacks of this solution are: dead time, switch noise, leakage current

This solution is rarely used

\[ u_{\text{out}}(s) \approx \frac{Q_{\text{in}}}{C_f} \frac{1}{(s+1/\tau_f)} \]

Unwanted pole

- Resistor $R_f$ continuously discharges the feedback capacitance $C_f$ after the pulse and takes away leakage current
- Time constant $\tau_f = R_f C_f$ is much longer than the front-end shaping time, typically $10^1$-$10^3$ $\mu$s
- Drawbacks are: additional thermal noise, spurious long tail appearing at the shaper output after the pulse (baseline change) – may be solved with pole-zero cancellation
Noise in CMOS – main components

- Thermal noise (Johnson, Nyquist)
- Shot noise (Schottky)
- 1/f or flicker noise

\[
S(f) = \frac{d\langle v^2 \rangle}{df} = 4kTR
\]

\[
S(f) = \frac{d\langle i^2 \rangle}{df} = 2qI
\]

\[
S(f) = \frac{d\langle v^2 \rangle}{df} = \frac{K_f}{f}
\]

White noise

1/f noise

Corner frequency

Log (f)
**Front-end electronics noise**

It is assumed that only the sensor and preamplifier contribute to output noise. It is justified since the signal after the preamplifier is already amplified. The equivalent noise diagram of sensor-preamplifier:

- **Shot noise related to sensor leakage current**

\[ i_d^2 \equiv \frac{d \langle i_d^2 \rangle}{df} = 2qI_d \]

- **Equivalent input voltage and current noise sources of preamplifier**

\[ v_{eq}^2 \equiv \frac{d \langle v_{eq}^2 \rangle}{df} = v_e^2 + \frac{K_f}{f} \]

\[ i_{eq}^2 \equiv \frac{d \langle i_{eq}^2 \rangle}{df} = i_e^2 \]

\[ v_{pre}^2 \equiv \frac{d \langle v_0^2 \rangle}{df} = \left| \frac{C_{in} + C_f}{C_f} \right|^2 \left( v_e^2 + \frac{K_f}{f} \right) + \left| \frac{1}{2j\pi f C_f} \right|^2 \left( i_e^2 + i_d^2 + i_{R_f}^2 \right) \]

- **Thermal noise of feedback resistance**

\[ v_{R_f}^2 \equiv \frac{d \langle v_{R_f}^2 \rangle}{df} = 4kT R_f \]
Shaper aim is to:

- Filter the signal spectrum to improve the S/N ratio. This is done by restricting the bandwidth
- Amplify the signal to the requested amplitude
- Set the signal length to permit operation with the expected rates

Low-pass filter reduces voltage noise
High-pass filter reduces current noise

\[
S_v \sim f^2
\]

Noise spectrum at preamplifier output
Shaper architectures

- Time invariant shapers – filter parameters do not change in time – most of applications!
  - simple implementation,
  - S/N performance close to optimum filter,
  - in particular the CR-RC\textsuperscript{n} filter - the most frequently used
- Time variant shapers – filter parameters change during processing of individual pulses
  - e.g. Correlated Double Sampling CDS
CR-RC\textsuperscript{n} shaper \((\tau = \tau_i = \tau_d)\) called pseudo-gaussian or semi-gaussian shaper gives a polynomial approximation of a gaussian signal shape. Number of integrators gives the order of pseudo-gaussian shaping:

\[
H(s) = \frac{u_{out}(s)}{u_{in}(s)} = \frac{s \tau}{(s+1/\tau)} \cdot \frac{1}{(s+1/\tau)^n}
\]

\[
u_{out}(t) \approx Q_{in} \cdot \left(\frac{t}{\tau}\right)^n \exp\left(-\frac{t}{\tau}\right)
\]

In most cases CR-RC or CR-RC\textsuperscript{2} are used!
ENC for pulse shapers

\[ \text{ENC} = \sqrt{\frac{F_v C_{\text{in}}^2 v_e^2}{\tau} + F_i i_e^2 \tau + F_f K_f C_{\text{in}}^2} \]

- **Voltage noise**
  \[ \propto \frac{1}{\tau} \]
  \[ \propto C_{\text{in}}^2 \]

- **Current noise**
  \[ \propto \tau \]
  independent of \( \tau \)

- **1/f noise**
  \[ \propto C_{\text{in}}^2 \]
  independent of \( C_{\text{in}} \)

- **\( F_v, F_i, F_f \)** – specific shape factors
- **\( v_e^2, i_e^2 \)** – voltage, current white noise densities \( v_e^2 \sim 1/g_m \)
- **\( K_f \)** – “1/f” noise constant
- **\( C_{\text{in}} \)** – total input capacitance
- **\( \tau \)** – characteristic shaping time (e.g. \( T_{\text{peak}} \))

**Graph:**
- Total noise
- Voltage noise
- Current noise
- 1/f noise
- Shaping time
**ENC for pseudo-gaussian shapers**

\[
ENC = \sqrt{\frac{F_v C_{\text{in}}^2}{T_{\text{peak}}} v_e^2 + F_i i_e^2 T_{\text{peak}} + F_f K_f C_{\text{in}}^2}
\]

The shape factors in pseudo-gaussian shaper with increasing shaping order:

<table>
<thead>
<tr>
<th>Shaper type</th>
<th>(F_v) factor</th>
<th>(F_i) factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>CR-RC</td>
<td>0.92</td>
<td>0.92</td>
</tr>
<tr>
<td>CR-RC(^2)</td>
<td>0.84</td>
<td>0.63</td>
</tr>
<tr>
<td>CR-CR(^3)</td>
<td>0.95</td>
<td>0.51</td>
</tr>
<tr>
<td>CR-RC(^4)</td>
<td>0.99</td>
<td>0.45</td>
</tr>
<tr>
<td>CR-RC(^5)</td>
<td>1.11</td>
<td>0.4</td>
</tr>
<tr>
<td>CR-RC(^6)</td>
<td>1.16</td>
<td>0.36</td>
</tr>
<tr>
<td>CR-RC(^7)</td>
<td>1.27</td>
<td>0.34</td>
</tr>
</tbody>
</table>

The contribution of current noise decreases with shaping order. 1/f noise depends strongly on technology but quantitatively is usually less important, especially for fast shaping.
**Energy/amplitude measurements**

- Synchronuos signals (e.g. collider experiments like ILC)
  - Signals sampled at peaking time by ADC or in analog memory

- Asynchronous signals (e.g. continuous beam like CLIC) – unknown time of signal appearance – time measurements also needed
  - Peak detector and stretcher (PDH) often used – too slow for CLIC
  - Continuous sampling with fast ADC and digital signal processing

For multichannel system a fast, scalable sampling frequency and power, small size ADC is needed!
Fast ADC - architectures

- **Flash**
  - Output rate = Clock rate
  - good for low resolution systems (<5 bit)

- **Pipeline**
  - Output rate = Clock rate
  - often used up to ~12-bit systems

- **Successive approximation (SAR)**
  - Output rate = Clock rate/Nr bits
  - often used up to ~12-bit resolution
  - too slow in the past - but with modern CMOS (<200nm) sampling rates beyond 50MS/s possible
  - extremely low power, e.g. ~1mW at 50MS/s possible
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LumiCal Readout architecture proposed at ILC

Prototypes designed in AMS 0.35um
Prototype LumiCal Front-end

\[
\frac{U_{\text{out}}(s)}{I_{\text{in}}(s)} = \frac{1}{C_f C_i R_s} \cdot \frac{s + 1/C_p R_p}{s + 1/C_f R_f} \cdot \frac{1}{(s + 1/C_i R_i)(s + 1/C_p (R_p \parallel R_s))}
\]

Existing prototypes:
8 channels in AMS0.35um
Cdet \approx 0 \div 100pF
Charge sensitive preamplifier + PZC
1st order shaper CR-RC (Tpeak \approx 60 ns)
Variable gain:
- Calibration mode - MIP sensitivity (~4fC)
- Physics mode - input charge up to 10 pC
Prototypes fabricated and tested
Power consumption 8.9 mW/channel
Event rate up to 3 MHz
Crosstalk < 1%

Pipeline ADC design

Parameters:
- 10-bit pipeline ADC
- 1.5 bit per stage architecture
- S/H stage + 9 pipeline stages
- Fully differential
- AMS 0.35um technology
- Area 0.87 mm²
- Max. sampling rate 25Ms/s
- Power pulsing

Results:
- Sampling rate 1kS/s-25MS/s
- Scalable power 0.85mW/MS/s
- SINAD~58 dB, ENOB=9.3 bit
- INL < 1 LSB
- DNL < 0.5 LSB

10-bit pipeline ADC

- High throughput – conversion rate = clock rate
- 1.5 bit per stage - redundancy reduces comparator requirements
- Fully differential architecture

S/H stage

1.5 bit pipeline stage
Testing ADC demanding scope and test pulse is not enough

- Static tests – linearity measurements
  - INL, DNL
- Dynamic tests – dynamic FFT measurements
  - SNHR, THD, SINAD, SFDR
- Other tests
  - Power pulsing, crosstalk, etc...

Building the setup needs: differential input, sine generator with very low harmonics, etc... . Requests: equipped lab, expertise and time!
Deconvolution principle for amplitude and time measurement

Pulse at output of shaper $v(t)$ is convolution of input signal (current from sensor – $s(t)$) and impulse response of readout chain $h(t)$:

$$v(t) = \int_{-\infty}^{+\infty} h(t-x) s(x) \, dx$$

Using data of continuously running ADC and taking advantage of known pulse shape one can perform invert procedure – deconvolution – to reconstruct event time and amplitude.

Attractive for asynchronous systems like CLIC and beam-tests.
Deconvolution principle...

Requirements:
- Simple hardware shaper realization
- Simple deconvolution formula

CR-RC shaper

Sensor pulse:
\[
I_{\text{sen}}(t) = \delta(t), \quad I_{\text{sen}}(s) = 1
\]

Deconvolution formula (s domain)
\[
D(s) = \frac{1}{V_{sh}(s)} = (s + 1/\tau)^2
\]

Deconvolution formula (z domain)
\[
z = e^{sT}, \quad D(z) = z^2 - 2ze^{-T/\tau} + e^{-2T/\tau}
\]

Deconvolution formula (time domain)
\[
d(t_i) = z^{-1}D(z) = V_{sh}(t_i) - 2e^{-T/\tau}V_{sh}(t_{i-1}) + e^{-2T/\tau}V_{sh}(t_{i-2})
\]
For \(\tau = T\):
\[
d(t_i) = V_{sh}(t_i) - 0.74V_{sh}(t_{i-1}) + 0.14V_{sh}(t_{i-2})
\]

CRRC response
\[
V_{sh}(s) = \frac{1}{(s + 1/\tau)^2}
\]

\(\tau\) - peaking time

Deconvolution with CR-RC shaping

\[ d_i = V_i - 2e^{-T/\tau} V_{i-1} + e^{-2T/\tau} V_{i-2} \]

- Only two multiplications and two additions (very fast and light!)
- Deconvolution produces non-zero data only when one or two first samples are on baseline, and second/third is on pulse
- **Initial time** of pulse is found from ratio of those samples
- **Amplitude** is found from sum of those samples, multiplied by time dependent correction factor
- Deconvolution reduces (infinite number) of CR-RC pulse samples to 1 or 2 non-zero samples
- Very good pile-up rejection capabilities!

CR-RC, \( T_{\text{sm}} = T_{\text{peak}} = 1 \), amp = 1

Synchronous sampling (t0 = int * Tsmp)

Asynchronous sampling (t0 = int * Tsmp)
CR-RC deconvolution properties

- Two events can be separated and precisely measured if they are distant 2-3 $T_{\text{smp}}$
- For $T_{\text{peak}} = T_{\text{smp}} = 60\text{ns}$ time resolution in range 2-7 ns is obtained
- SNR is only slightly deteriorated
- Monte Carlo simulations fits well to measurements

Sz. Kulis, M. Idzik "Study of readout architectures for triggerless high event rate detectors at CLIC" LCD-Note-2011-015
Deconvolution – example results

Results obtained for S/N~20 with the LumiCal front-end ASIC (CR-RC shaping, $T_{\text{peak}} \sim 60\text{ns}$) presented before and with standard silicon pad sensor

Good amplitude and time resolution - simulated in MC and confirmed experimentally!

$NF = \frac{S/N_{\text{in}}}{S/N_{\text{out}}} \text{[dB]}$

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SoC type multichannel readout

- ASIC advantages: multichannel implementation, low power, small size
- Complex multichannel system requires a number of peripherals:
  - DACs for voltage and current biasing
  - Reference voltage - bandgap
  - I/O circuits – LVDS driver/receiver standard is often used
  - Temperature monitoring circuits
  - PLLs
  - Data serializers and deserializers
  - Other...
Readout peripherals

10-bit low power high swing DAC

- 10th bit achieved by current reversing
- Nonlinearities DNL & INL < 0.42 LSB
- ENOB = 9.8 bit
- Settling time 0.5 – 2 μs
- Power consumption < 0.6 mW
- Tests completed

9 bit unit current sources matrix

Interconnection network

Current switches

Current mirror

Class AB output OPAMP

Bandgap reference and temperature sensor

\[ V_T = k_I k_R \left[ V_{th} \ln \left( k_D \right) - V_{OS} \right] \approx 5.259 \frac{mV}{K} \cdot T - 26.25 \cdot V_{os} \]

- Configuration implemented in IBM 0.25um and AMS 0.35um
- Power consumption < 100uW

M. Idzik, M. Ornat, “Design and operation of low power temperature sensor – bandgap reference circuit in submicron technology”, Proc. of 12\textsuperscript{th} Int. Conf. MIXDES 2005 22-25 June Kraków Poland
Design of fast low power PLL

- Second order Phase Locked Loop
- "Current starved" Voltage Controlled Oscillator
- Input frequency multiplied by 32
- Binary controlled multiplexed LVDS output from divider
- AMS 0.35um, 160 x 140 um²
- 4.5mW @1GHz

Multichannel digitizer
complex system design example

AMS 0.35um technology
8 channels of 10 bit ADC
- 1.5 bit per stage pipeline architecture
- S/H stage plus 9 pipeline stages in each channel
- Layout with 200um ADC pitch

Digital multiplexer/serializer:
- Serial mode (~250MHz): one data link per all channels (max fsmp ~ 3 MSps)
- Parallel mode (~250MHz): one data link per channel (max fsmp ~ 25 MSps)
- Test mode: single channel (max fsmp ~50 MSps)

High speed LVDS drivers & receivers (<=1GHz)
Various (7) DACs for analog controls
Precise BandGap reference source
Temperature sensor
Power pulsing
Multichannel Digitizer

Results

Performance:
- ENOB=9.7 bit up to 25 Ms/s (8 channels)
- Single ADC works up to 50 Ms/s
- Power consumption scales with sampling rate \( \sim 1.2 \text{mW/chan/MHz} \)
- Excellent uniformity between the channels, gain spread < 0.1%
- Crosstalk < -80 dB
- Power pulsing embedded, \( t_{ON} \sim 3 \text{ us} \)

Static measurements

SINAD
SNHR
THD
SFD

Dynamic measurements

Nonlinearity (LSB)

Level (dB)

Sampling Frequency (Hz)

Die size 2.6mm x 3.2mm

## Comparison to commercial 10-bit multichannel ADCs

<table>
<thead>
<tr>
<th>Parameter</th>
<th>This work TNS in print...</th>
<th>Kaviani et al. ESSCIRC 2002</th>
<th>AD9212</th>
<th>ADS5287</th>
<th>MAX1434</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nr channels</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Serialization</td>
<td>per channel or per chip</td>
<td>per chip</td>
<td>per channel</td>
<td>per channel</td>
<td>per channel</td>
</tr>
<tr>
<td>Architecture</td>
<td>10-bit pipeline</td>
<td>10-bit pipeline</td>
<td>10-bit pipeline</td>
<td>10-bit pipeline</td>
<td>10-bit pipeline</td>
</tr>
<tr>
<td>Technology</td>
<td>0.35 $\mu$m CMOS</td>
<td>0.25 $\mu$m CMOS</td>
<td>-</td>
<td>CMOS</td>
<td>BiCMOS</td>
</tr>
<tr>
<td>Power supply</td>
<td>3.3 V</td>
<td>2.5 V</td>
<td>1.8 V</td>
<td>3.3 $V_A$, 1.8 $V_D$</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Max. $f_{sample}$</td>
<td>25 MS/s</td>
<td>20 MS/s</td>
<td>65 MS/s</td>
<td>65 MS/s</td>
<td>50 MS/s</td>
</tr>
<tr>
<td>Input range</td>
<td>$2 V_{pp}$</td>
<td>-</td>
<td>$2 V_{pp}$</td>
<td>$2 V_{pp}$</td>
<td>$1.4 V_{pp}$</td>
</tr>
<tr>
<td>Total power per channel +I/O (&lt;15%)</td>
<td>~1.2 mW/MS/s</td>
<td>41 mW @20MS/s</td>
<td>100 mW @65MS/s</td>
<td>74 mW @65 MS/s</td>
<td>96 mW @50MS/s</td>
</tr>
<tr>
<td>Area</td>
<td>8.2 mm$^2$</td>
<td>4 mm$^2$</td>
<td>9x9 mm$^2$ (package)</td>
<td>9x9 mm$^2$ (package)</td>
<td>14x14 mm$^2$ (package)</td>
</tr>
<tr>
<td>INL</td>
<td>&lt;0.68 LSB</td>
<td>-</td>
<td>&lt;0.5 LSB</td>
<td>&lt;1 LSB</td>
<td>&lt;1 LSB</td>
</tr>
<tr>
<td>DNL</td>
<td>&lt;0.62 LSB</td>
<td>-</td>
<td>&lt;0.4 LSB</td>
<td>&lt;0.55 LSB</td>
<td>&lt;0.5 LSB</td>
</tr>
<tr>
<td>SINAD</td>
<td>~60.3 dB</td>
<td>54.3 dB</td>
<td>≥60 dB</td>
<td>≥60.4 dB</td>
<td>≥60 dB</td>
</tr>
<tr>
<td>ENOB</td>
<td>9.7</td>
<td>8.7</td>
<td>≥9.7</td>
<td>≥9.7</td>
<td>≥9.7</td>
</tr>
<tr>
<td>$T_{power , on}$</td>
<td>≤10 $T_{cik}$</td>
<td>-</td>
<td>375 $\mu$s</td>
<td>-</td>
<td>100 ms</td>
</tr>
<tr>
<td>$\sim 3 \mu$s @ILC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Even if designed in rather old technology our design compares quite well to the state of the art commercial multichannel ADCs.
Complete readout system example

not only ASICs make the system...

- 32 channels fully equipped channels (Front-end +ADC) + FPGA data conc.
- ADC sampling rate is up to 20 MS/s (6.4 Gbps)
- Extended trigger mechanism
  - External CMOS / LVDS
  - Self triggering on ADC values
  - Software
- Data can be transferred using USB
- Signal handshaking with Trigger Logic Unit (TLU)
- ADC Clock source
  - Internal (asynchronous with beam operation)
  - External (beam clock used to synchronize with beam) ILC mode

Power delivery and pulsing

Performance with power pulsing

Front-end power consumption

Front-end switch ON time

Digitizer temperature
LumiCal Detector prototype in FCAL beam-test

- Gain
  - HH 19107.5 LSB/pC
  - LH 3241.0 LSB/pC
  - HL 471.1 LSB/pC
  - LL 80.3 LSB/pC

- MIP spectrum
  - Signal: 39.19 LSB
  - Noise: 1.52 LSB
  - SNR: 21.8
  - entries: 7093 Chi2/N: 0.93

- Energy dep. vs nr X0

Instrumented Area
Outline

- Introduction to forward detectors in ILC/CLIC
- Front-end electronics signal processing
  - Noise, Preamplifier, Shaper, S/N and ENC, ADC
- Core ASICs and signal processing for LumiCal Detector
  - Preamplifier-Shaper ASIC
  - Pipeline ADC ASIC
  - Readout with deconvolution
- Integration of Complex Readout System for LumiCal
  - Peripheral blocks for multichannel system
  - Multichannel Digitizer ASIC
  - Prototype multichannel readout system
- Developments in progress...
Development of ASICS for new readout chain in progress...

- Change of technology and/or architecture to get: lower power, higher speed, radiation hardness
- Design of new front-end in IBM 130nm in progress
  - Last specifications under discussion...
  - Expected drop in power ~5 times
- First prototype of SAR ADC in IBM 130nm just submitted
  - Segmented DAC architecture
  - Expected drop in power >=20 times
  - Max. sampling rate >=40Ms/s (LHC rate)
  - The only analog part – comparator, (fits to modern submicron CMOS)
  - Capacitive DAC network (serves as sampling capacitance)
  - Asynchronous logic improves speed
Modern CMOS processes offer higher speed but lower gain!
Design more difficult!
Architecture for very high rates at CLIC

Gated integrator + CDS

Operation:
- Reset before the beam train
- Integration during the beam train (156ns for CLIC)

Occupancy of LumiCal pads due to incoherent pairs

“Physics and Detectors at CLIC”, CLIC Conceptual Design Report 2011

S. Kulis, M. Idzik, “Study of readout architectures for triggerless high event rate detectors at CLIC”, CERN LCD-Note-2011-015 2009
Readout example

δ-like charge deposition →

Pulse from the sensor →

Readout with CR-RC shaping and deconvolution →

\[ T_{\text{peak}} = 30\text{ns}, \ T_{\text{smp}} = 10\text{ns} \]

Readout with gated integrator and CDS →

\[ T_{\text{int}} = 5\text{ns}, \ T_{\text{smp}} = 10\text{ns} \]

Occupancy ~ 1-1.5% per PAD per BX
Summary

- As seen on LumiCal case, the forthcoming experiments are setting more and more challenges for: high speed, low power, concurrent amplitude&time measurements, radiation hard...
- To fulfill growing demands the ASICs need to be more complex (approaching SoC) and deep submicron technologies need to be used.
- Deep submicron technology means limited analog features – more difficult design, growing part of digital signal processing (DSP), and of course higher price.
- Growing demands for DSP opens the possibility for higher integration of ASICs and FPGAs (faster development and much cheaper) for present and future readout systems.
Thank you for attention
Signal timing measurements

To measure the time of signal occurrence, fast discriminator is added after shaper output. Main uncertainties are:

- **Time jitter error**
  - Due to noise

- **Time walk**
  - Due to amplitude variation

Instead of S/N the slope to noise ratio is optimized: Steeper slope – better timing resolution – worse amplitude resolution
Example front-end under developed for straw tubes in PANDA

Readout chain

- Preamplifier
- Shaper
- Tail cancellation
- Baseline holder (BLH)
- Leading edge discriminator
- Fast LVDS output
- Analog output

Design goals:
Timing measurement (~1ns)
Amplitude measurements
Straw ASIC-first measurement

- **Timewalk**
  - Graph showing timewalk vs. input charge.

- **Jitter**
  - Graph showing jitter vs. time.
  - \( \sigma = 0.14 \) ns.

- **s-curves**
  - Graph showing s-curves for different input charge values.

- **Gain**
  - Graph showing gain vs. input charge.
  - \( K_0 = 9.35 \) mV/IC, \( V_0 = 1.173 \) V.
Straw ASIC - tail cancellation

Tail cancellation network has \( \sim 4000 \) possible settings. Here only few are shown.
Amplifier in modern CMOS

some ideas...

Cascode amplifier  Self-Cascode  Regulated cascode

Low intrinsic gain and small supply voltage make amplifier design difficult!
δ-like charge deposition →

Pulse from the sensor →

Readout with CR-RC shaping and deconvolution →
\[ T_{\text{peak}} = 30\text{ns}, T_{\text{smp}} = 10\text{ns} \]

Readout with gated integrator and CDS →
\[ T_{\text{int}} = 5\text{ns}, T_{\text{smp}} = 10\text{ns} \]
Transceiver architecture

Transmitter (Tx)
• Parallel synchronous to serial asynchronous data converter
• Up to ~1GHz output clock from PLL

Receiver (Rx)
• Serial asynchronous to parallel synchronous
• PLL clock generated and synchronized with transmitter by CDR (burst mode) circuit

CMOS technology scaling
more channels, lower power, smaller size

Relations for long channel devices

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Constant-field scaling</th>
<th>Generalized field scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>Physical dimensions: L, W, Tox, wire pitch</td>
<td>1/S</td>
<td>1/S</td>
</tr>
<tr>
<td>Body doping concentration</td>
<td>S</td>
<td>E/S</td>
</tr>
<tr>
<td>Voltage</td>
<td>1/S</td>
<td>E/S</td>
</tr>
<tr>
<td>Circuit density</td>
<td>1/S^2</td>
<td>1/S^2</td>
</tr>
<tr>
<td>Capacitance per circuit</td>
<td>1/S</td>
<td>1/S</td>
</tr>
<tr>
<td>Circuit speed</td>
<td>S</td>
<td>S (goal)</td>
</tr>
<tr>
<td>Circuit power</td>
<td>1/S^2</td>
<td>E^2/S^2</td>
</tr>
<tr>
<td>Power density</td>
<td>1</td>
<td>E^2</td>
</tr>
<tr>
<td>Power-delay product</td>
<td>1/S^3</td>
<td>E^2/S^3</td>
</tr>
</tbody>
</table>

S – scaling factor
E=V/S – normalized electric field

Additional advantage – thinner oxide – less trapping – better radiation hardness!

Moore law works well...
HEP: 0.8um, 0.35um, LHC-0.25um, FAIR-0.18um?, S-LHC-0.13um?, 65nm?
FPGA – Field Programmable Gate Array for complex readout systems

- Advantages
  - Rapid development
  - Huge possibilities (billions of gates)
  - Low cost
  - Abundance of configurable resources
  - Smallest CMOS processes – low power

- HEP applications
  - Proof of concept for digital designs
  - ASIC testing & verification (e.g. ADC parametrization)
  - Data AcQuisition (DAQ) and Trigger processing units
  - New applications coming (e.g. TDC)...
LVDS receiver

Direct implementation of self-biased differential amplifier

Readout peripherals

L-2L DAC

Architecture

An architecture based on MOS implementation of R–2R ladder (L–2L)
Main benefits:
- Small number of elements (4N+1)
- Simple layout

Principle of operation

Current flowing into series–parallel identically designed transistors is equally divided between them[1]

Implementation

Design assumptions

- Static DAC with 8 bit resolution.
- Low power consumption < 100 µW
- Small core size < 0.05 mm²
- Application – fine voltages trimming in multichannel readout systems

D.Przyborowski, M.Idzik, “Development of low-power small-area L-2L CMOS DACs for multichannel readout systems”, JINST 7 C01026 2012
ASIC design flow

- Schematic and simulations
  - Preamplifier, Shaper, I/O, etc...
  - Standard DC, AC, TRAN simulations, MC(!) and Worst Case simulations

- Layout
  - Drawn manually (or Layout XL guided)
  - Digital part synthesized automatically with SoC Encounter

- Verifications
  - DRC – checking design rules
  - LVS (layout vs schematic) - comparing layout with original design
  - QRC – parasitic extraction (for post-layout simulations)

Post-layout simulations and design-layout iterations!
Generating the GDS2 file for submission
Pipeline ADC – key blocks

- Fully differential amplifier+CMFB
- Dynamic latch comparator
- Digital correction

A lot of consumed power goes to amplifiers and clock distribution