Development of ASICs for forward calorimetry in future linear collider

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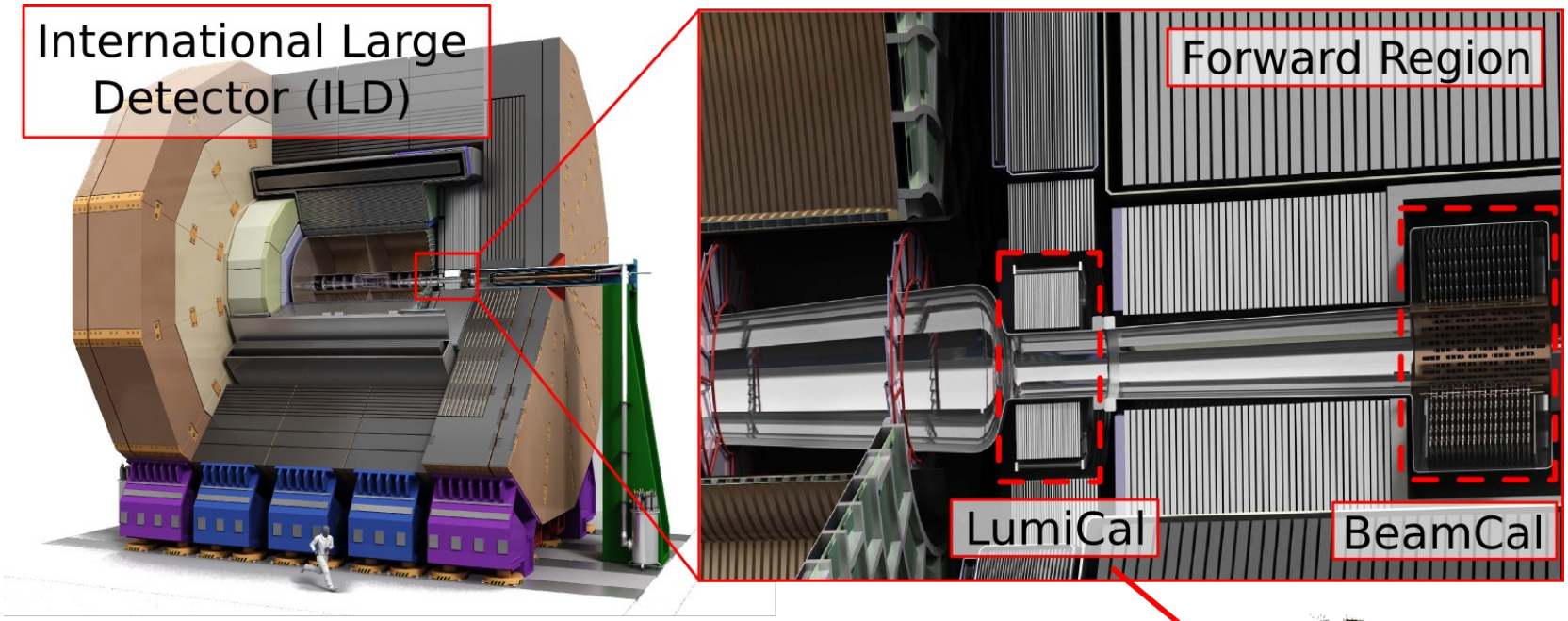
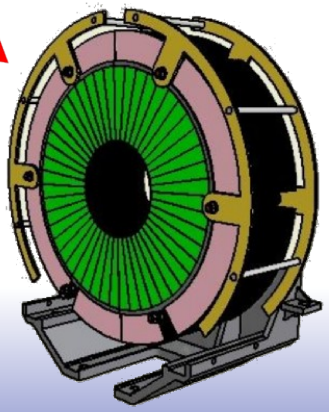
Outline

- Introduction to forward detectors in ILC/CLIC
- Front-end electronics signal processing
  - Noise, Preamplifier, Shaper, S/N and ENC, ADC
- Core ASICs and signal processing for LumiCal Detector
  - Preamplifier-Shaper ASIC
  - Pipeline ADC ASIC
  - Readout with deconvolution
- Integration of Complex Readout System for LumiCal
  - Peripheral blocks for multichannel system
  - Multichannel Digitizer ASIC
  - Prototype multichannel readout system
- Developments in progress...

LumiCal Detector in ILD



- **Aim:** Precise measurement of integrated luminosity (based on counting BhaBha events)
- **Construction :** sampling calorimeter 30 (ILC) / 40 (CLIC) layers Si/W



H. Abramowicz et al. , "Forward Instrumentation for ILC Detectors" JINST 5:P12002, 2010

LumiCal baseline design

Parameter	ILC	CLIC
Absorber material	Tungsten	Tungsten
Absorber thickness[mm]	3.5	3.5
Sensor [μm]	Si 300	Si 300
R inner [mm]	80	100
R outter [mm]	195.2	290
Θ inner [mrad]	31	37
Θ outter [mrad]	78	110
Z pos [mm]	2500	2654
Layers	30	40
Mass [kg]	210	660

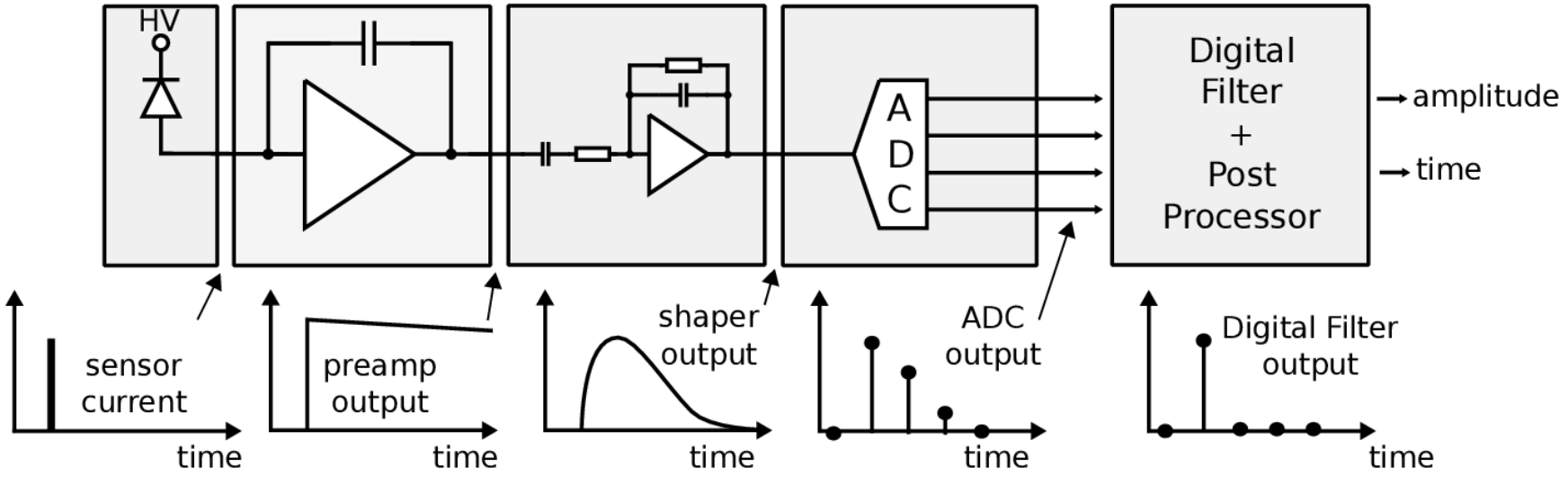
Linear Collider Parameters

Parameter	ILC	CLIC	
Centre-of-mass energy (GeV)	**500**	**500**	**3000**
Total (Peak 1%) luminosity (10^{34})	2.0(1.5)	2.3(1.4)	5.9(2.0)
Total site length (km)	31	13.0	48.3
Loaded accel. gradient (MV/m)	31.5	80	100
Main linac RF frequency (GHz)	**1.3 (Super Cond.)**	**12 (Normal Conducting)**	
Beam power/beam (MW)	20	4.9	14
Bunch charge (10^9 e+/-)	20	6.8	3.72
Bunch separation (ns)	**330**	**0.5**	
Beam pulse duration (ns)	**1000000**	**177**	**156**
Repetition rate (Hz)	**5**	**50**	
…	…	…	…
Total power consumption (MW)	216	129.4	415

Readout requirements for ILC and CLIC different:

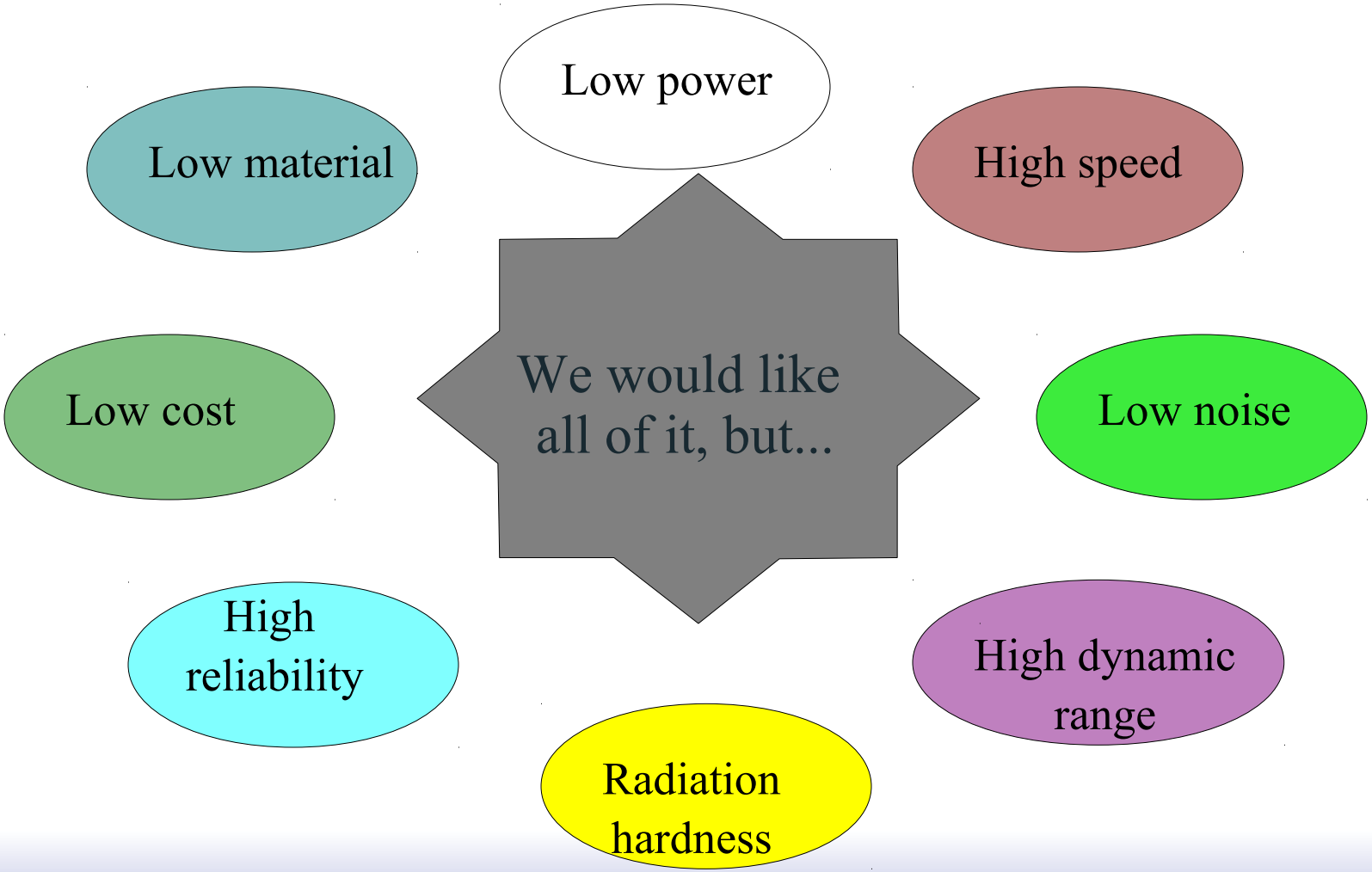
- Synchronous with beam measurement of signal feasible at ILC
- Asynchronous amplitude and time measurement needed for CLIC
- Power pulsing feasible for ILC and CLIC

"Future" readout architecture
for amplitude and time measurement



Is it possible to proceed with similar developments for ILC and CLIC ?

Readout electronics requirements



Technology limitations - compromise needed!

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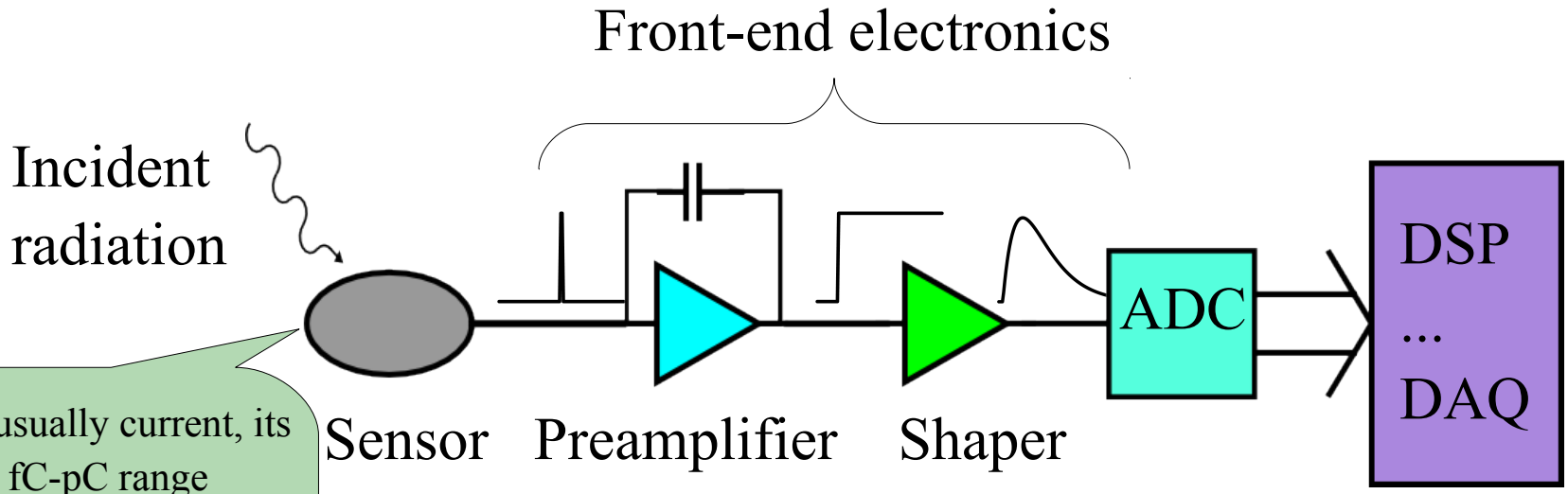
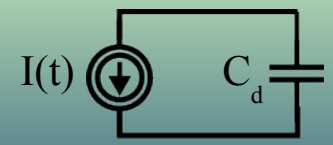
Readout electronics general architecture

Readout electronics processes signals from sensors to measure:

- energy released by radiation ► spectroscopy measurements
- time of signal occurrence ► timing measurements
- position where the radiation hits the sensor ► tracking, imaging

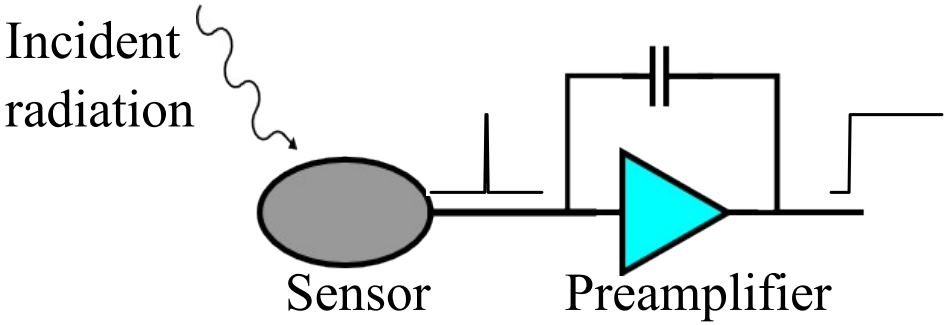


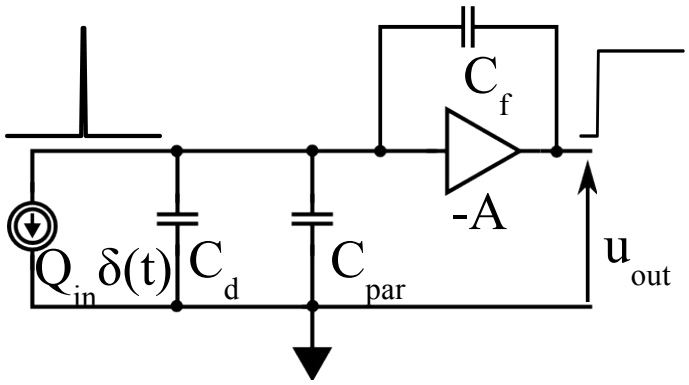
- Signal usually current, its charge in fC-pC range
- Sensor usually capacitive in 0.1-100 pF range



Front-end electronics noise performance is usually expressed by the Signal to Noise (S/N) ratio (typically S/N>10 required), or even better by the Equivalent Noise Charge (ENC), e.g. charge for which S/N=1

Charge Preamplifier





- The most often used charge sensitive preamplifier configuration integrates sensor current giving the output proportional to the charge released in the sensor and so to the deposited energy (in silicon ~3.6 eV per electron-hole pair)
- Preamplifier amplifies sensor signal enough so that the noise sources in following stages do not deteriorate S/N
- Preamplifier should contribute minimum possible noise

$$u_{out}(t) = \frac{Q_{in}}{C_f\left(1+\frac{1}{A}\frac{C_f+C_{in}}{C_f}\right)} \cdot 1(t)$$

u_{out} depends mainly on C_f

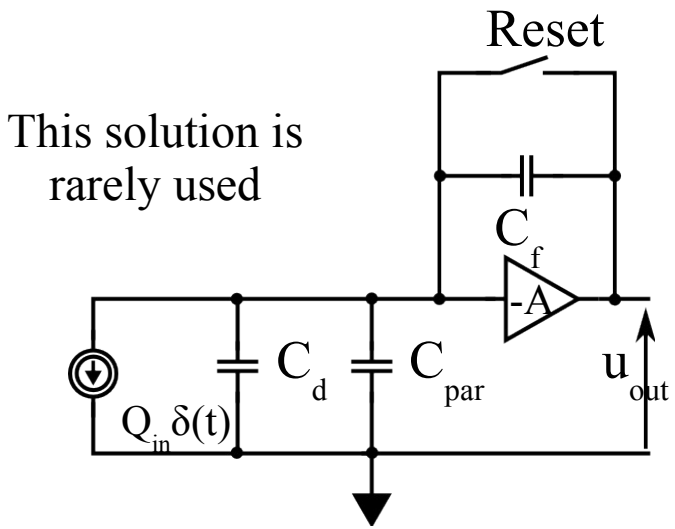
if $A \rightarrow \infty$

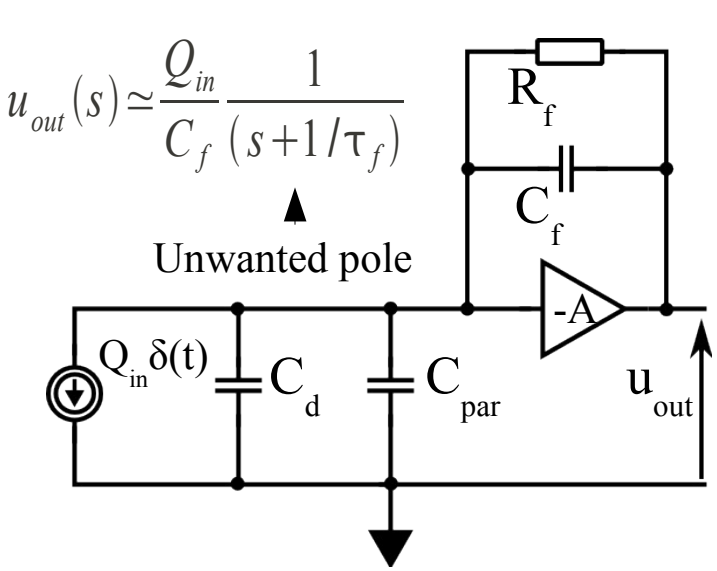
$$u_{out}(t) = \frac{Q_{in}}{C_f} \cdot 1(t)$$

Problems: No DC bias at input,
No discharge of C_f.

Typical gain: C_f=0.2pF→ 20mV/fC

Charge Preamplifier pulsed reset - continuous reset





- Reset switch allows the removal of charge from feedback capacitance C_f
- Charge may be removed periodically
- Drawbacks of this solution are: dead time, switch noise, leakage current

- Resistor R_f continously discharges the feedback capacitance C_f after the pulse and takes away leakage current
- Time constant $\tau_f = R_f C_f$ is much longer than the front-end shaping time, typically 10^1-10^3 μs
- Drawbacks are: additional thermal noise, spurious long tail appearing at the shaper output after the pulse (baseline change) – may be solved with pole-zero cancellation

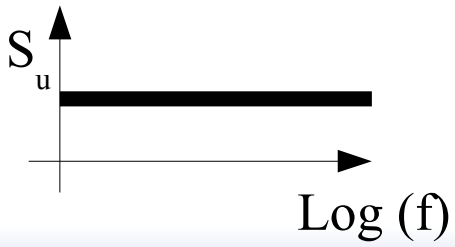
Noise in CMOS – main components

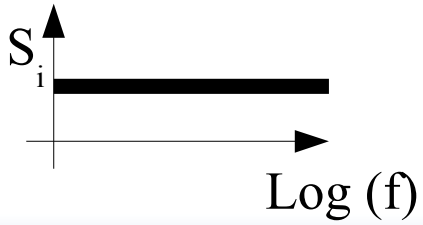
- Thermal noise (Johnson, Nyquist)
- Shot noise (Schottky)
- 1/f or flicker noise

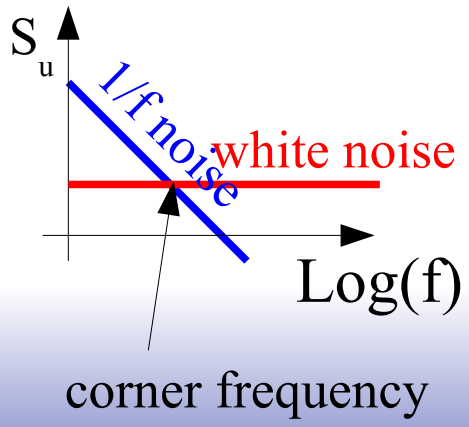
$$S(f)=\frac{d\langle v^2\rangle}{df}=4kTR$$

$$S(f)=\frac{d\langle i^2\rangle}{df}=2qI$$

$$S(f)=\frac{d\langle v^2\rangle}{df}=\frac{K_f}{f}$$

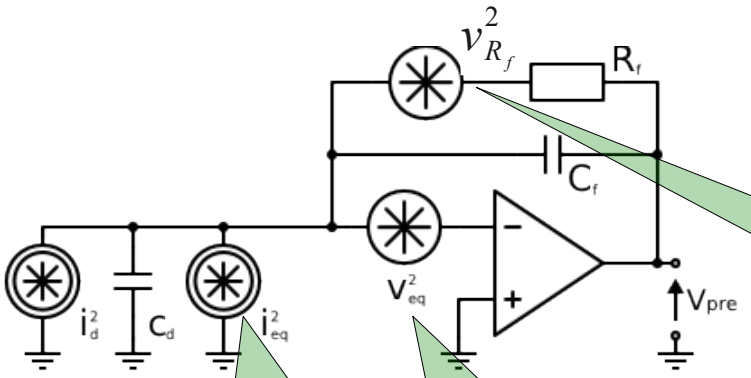






Front-end electronics noise

It is assumed that only the sensor and preamplifier contribute to output noise. It is justified since the signal after the preamplifier is already amplified. The equivalent noise diagram of sensor-preamplifier:



$$i_d^2 \equiv \frac{d\langle i_d^2 \rangle}{df} = 2qI_d$$

Shot noise related to sensor leakage current

$$v_{R_f}^2 \equiv \frac{d\langle v_{R_f}^2 \rangle}{df} = 4kT\,R_f$$

Thermal noise of feedback resistance

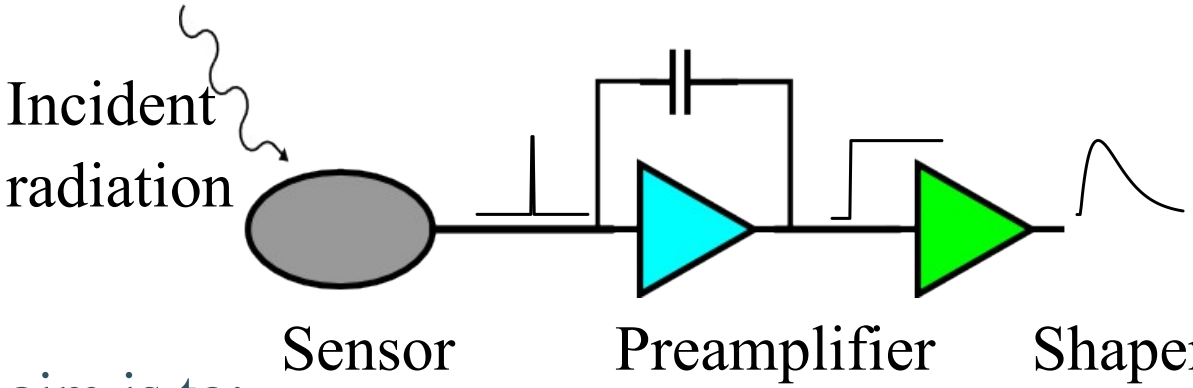
Equivalent input voltage and current noise sources of preamplifier

$$v_{eq}^2 \equiv \frac{d\langle v_{eq}^2 \rangle}{df} = v_e^2 + \frac{K_f}{f}$$

$$i_{eq}^2 \equiv \frac{d\langle i_{eq}^2 \rangle}{df} = i_e^2$$

$$v_{pre}^2 \equiv \frac{d\langle v_0^2 \rangle}{df} = \left|\frac{C_{in}+C_f}{C_f}\right|^2 \left(v_e^2 + \frac{K_f}{f}\right) + \left|\frac{1}{2j\pi f C_f}\right|^2 \left(i_e^2 + i_d^2 + i_{R_f}^2\right)$$

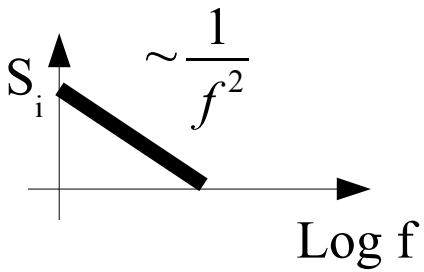
Shaper - filter



Shaper aim is to:

- Filter the signal spectrum to improve the S/N ratio. This is done by restricting the bandwidth
- Amplify the signal to the requested amplitude
- Set the signal length to permit operation with the expected rates

Noise spectrum at preamplifier output

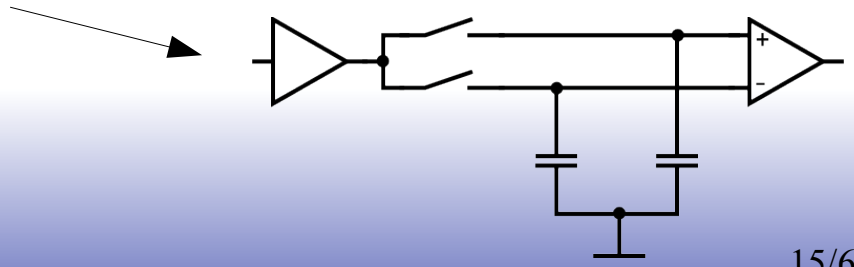


Low-pass filter
reduces voltage noise

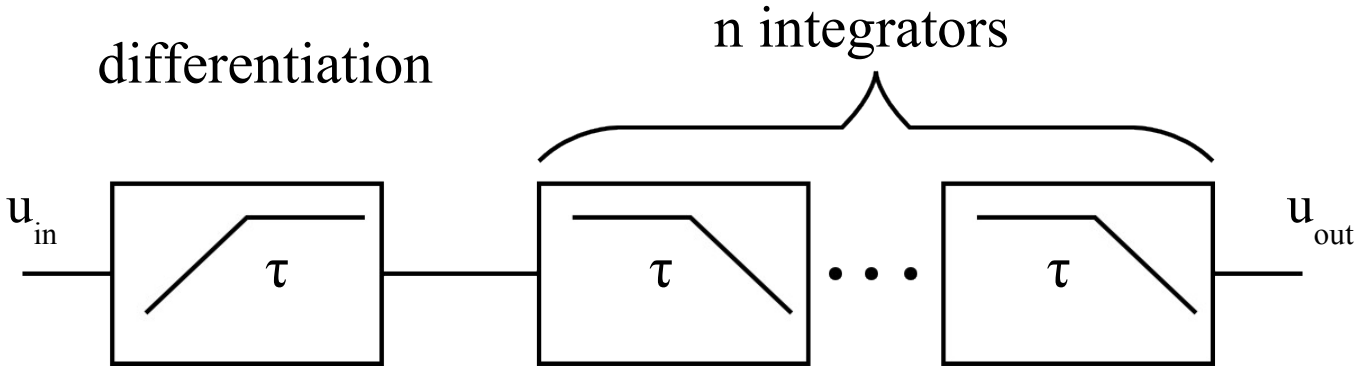
High-pass filter
reduces current noise

Shaper architectures

- Time invariant shapers – filter parameters do not change in time – most of applications!
  - simple implementation,
  - S/N performance close to optimum filter,
  - in particular the CR-RC^n filter - the most frequently used
- Time variant shapers – filter parameters change during processing of individual pulses
  - e.g. Correlated Double Sampling CDS



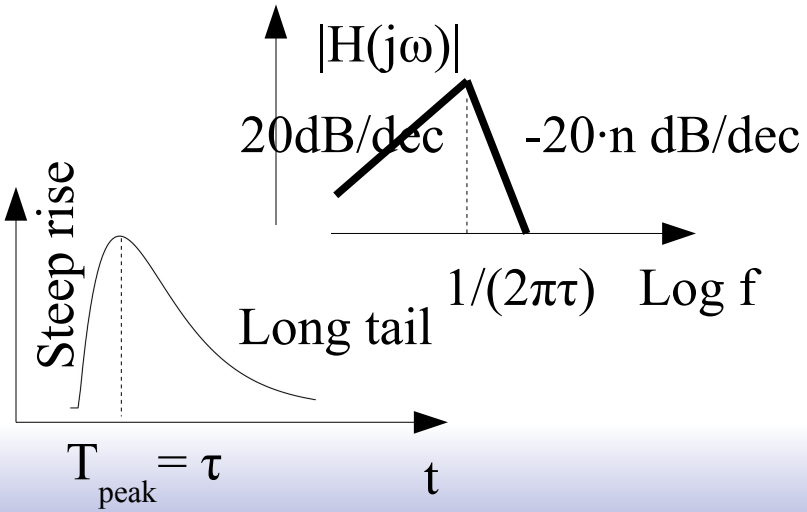
Pseudo-Gaussian Shaper



CR-RC^n shaper ($\tau=\tau_i=\tau_d$) called pseudo-gaussian or semi-gaussian shaper gives a polinomial approximation of a gaussian signal shape. Number of integrators gives the order of pseudo-gaussian shaping

$$H(s)=\frac{u_{out}(s)}{u_{in}(s)}=\frac{s\tau}{(s+1/\tau)}\cdot\frac{1}{(s+1/\tau)^n}$$

$$u_{out}(t)\simeq\frac{Q_{in}}{C_f}\cdot\left(\frac{t}{\tau}\right)^n\exp\left(-\frac{t}{\tau}\right)$$



In most cases CR-RC or CR-RC^2 are used !

ENC for pulse shapers

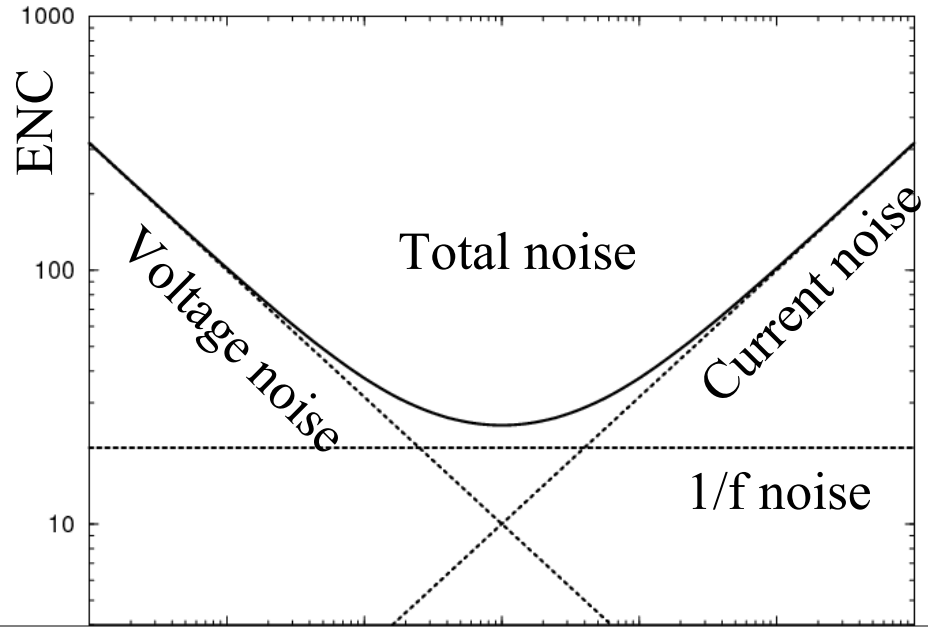
$$ENC = \sqrt{\frac{F_v C_{in}^2 v_e^2}{\tau} + F_i i_e^2 \tau + F_f K_f C_{in}^2}$$

voltage noise
$\propto 1/\tau$
$\propto C_{in}^2$

current noise
$\propto \tau$
independent of C_{in}

1/f noise
independent of τ
$\propto C_{in}^2$

- F_v, F_i, F_f – specific shape factors
- v_e^2, i_e^2 – voltage, current white noise densities $v_e^2 \sim 1/g_m$
- K_f – "1/f" noise constant
- C_{in} – total input capacitance
- τ – characteristic shaping time (e.g T_{peak})

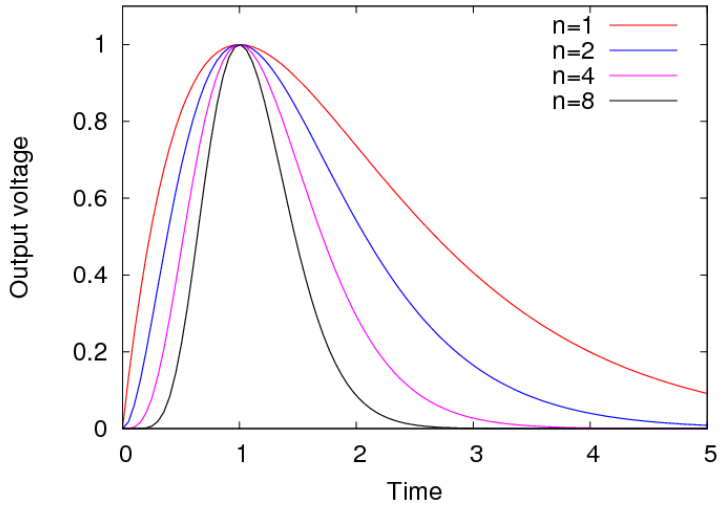


ENC for pseudo-gaussian shapers

$$ENC = \sqrt{\frac{F_v C_{in}^2 v_e^2}{T_{peak}} + F_i i_e^2 T_{peak} + F_f K_f C_{in}^2}$$

The shape factors in pseudo-gaussian shaper with increasing shaping order:

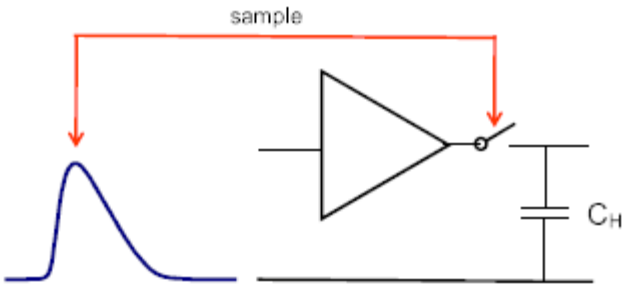
Shaper type	F_v factor	F_i factor
CR-RC	0.92	0.92
CR-RC^2	0.84	0.63
CR-CR^3	0.95	0.51
CR-RC^4	0.99	0.45
CR-RC^5	1.11	0.4
CR-RC^6	1.16	0.36
CR-RC^7	1.27	0.34



The contribution of current noise decreases with shaping order. 1/f noise depends strongly on technology but quantitatively is usually less important, especially for fast shaping.

Energy/amplitude measurements

- Synchronuos signals (e.g. collider experiments like ILC)
  - **Signals sampled at peaking time by ADC or in analog memory**

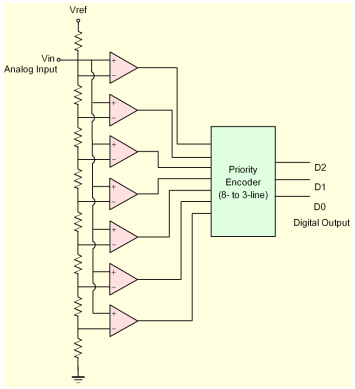


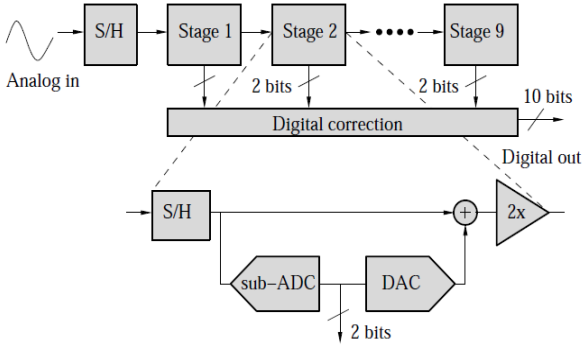
- Asynchronous signals (e.g. continuous beam like CLIC) – unknown time of signal appearance – time measurements also needed
  - Peak detector and stretcher (PDH) often used – too slow for CLIC
  - **Continuous sampling with fast ADC and digital signal processing**

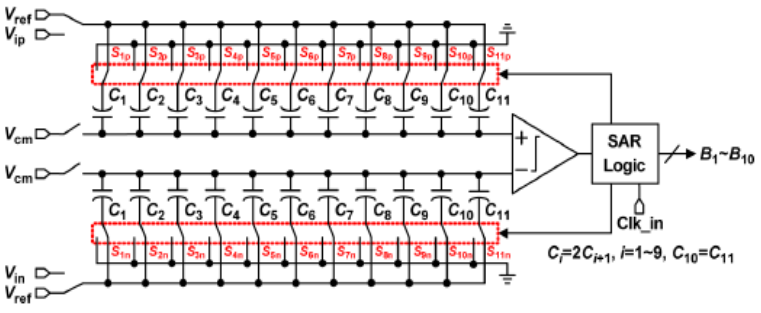
For multichannel system a fast, scalable sampling frequency and power, small size ADC is needed!

Fast ADC - architectures

- Flash
  - Output rate = Clock rate
  - good for low resolution systems (<5 bit)
- Pipeline
  - Output rate = Clock rate
  - often used up to ~12-bit systems
- Successive approximation (SAR)
  - Output rate = Clock rate/Nr bits
  - often used up to ~12-bit resolution
  - too slow in the past - but with modern CMOS (<200nm) sampling rates beyond 50MS/s possible
  - extremely low power, e.g. ~1mW at 50MS/s possible







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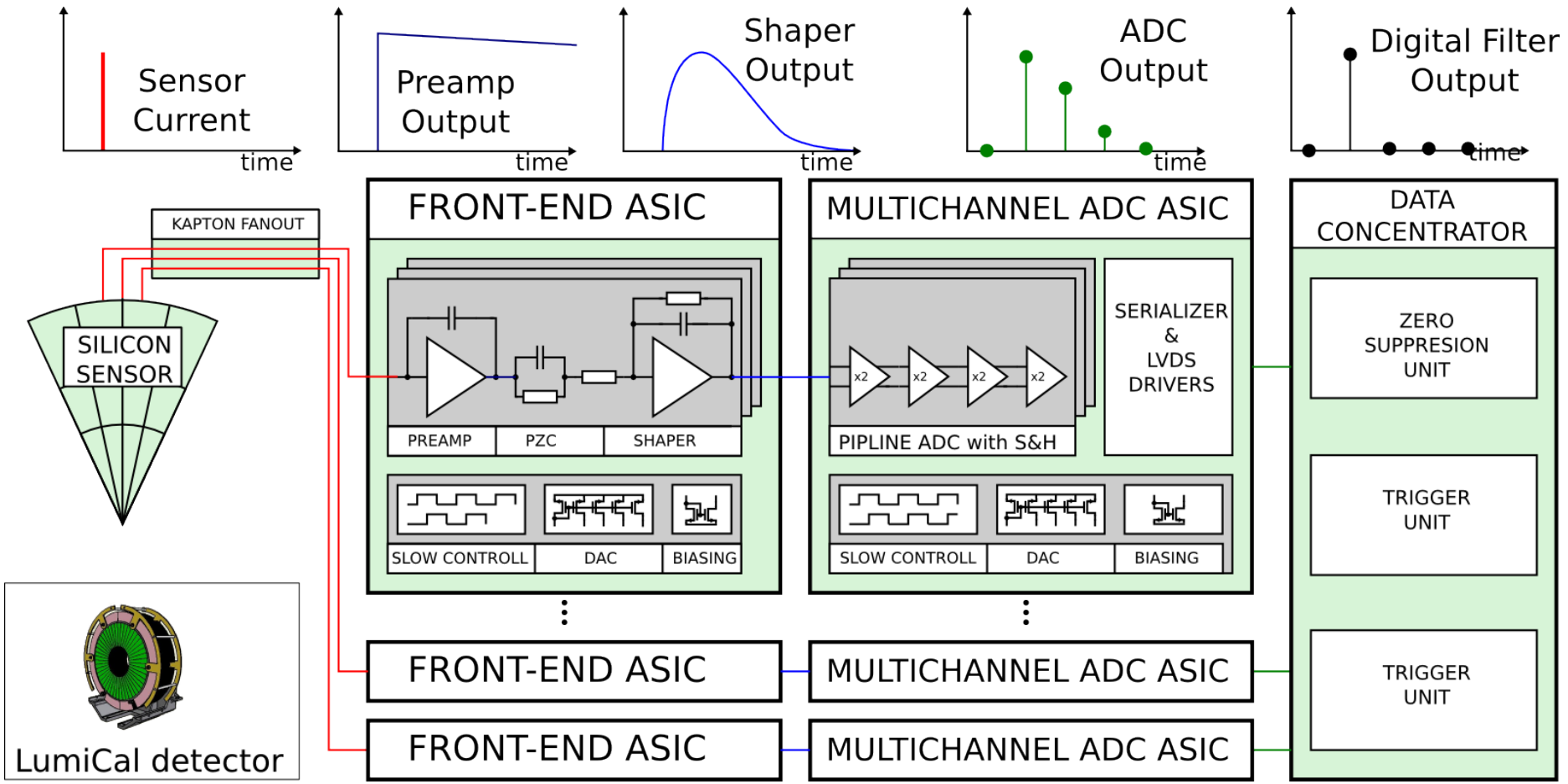
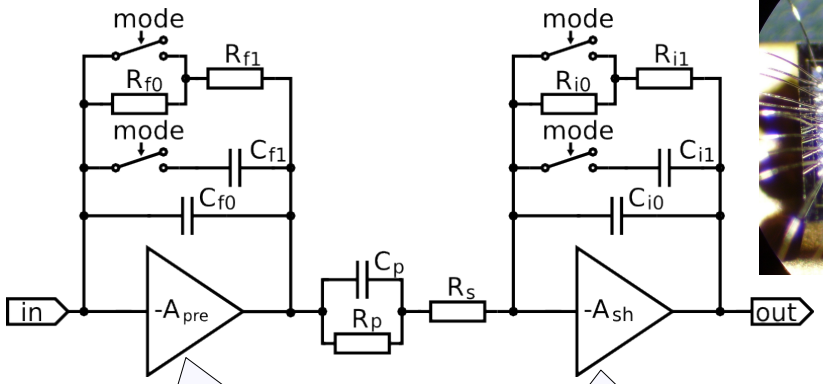
LumiCal Readout architecture proposed at ILC

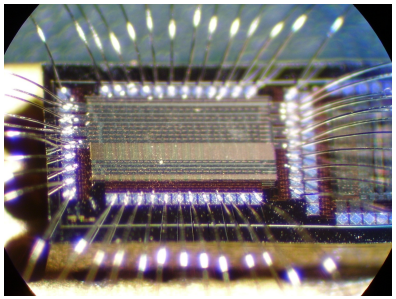


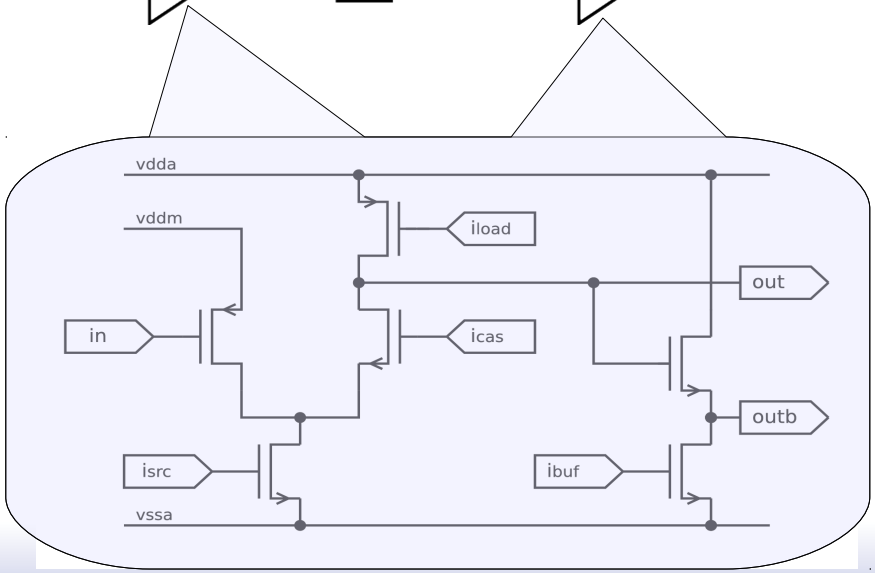
Prototypes designed in AMS 0.35um

Prototype LumiCal Front-end

$$\frac{U_{out}(s)}{I_{in}(s)} = \frac{1}{C_f C_i R_s} \cdot \frac{s + 1/C_p R_p}{s + 1/C_f R_f} \cdot \frac{1}{(s + 1/C_i R_i)(s + 1/C_p (R_p \| R_s))}$$







Existing prototypes:

8 channels in AMS0.35um

Cdet ≈ 0 ÷ 100pF

Charge sensitive preamplifier + PZC

1st order shaper CR-RC (Tpeak ≈ 60 ns)

Variable gain:

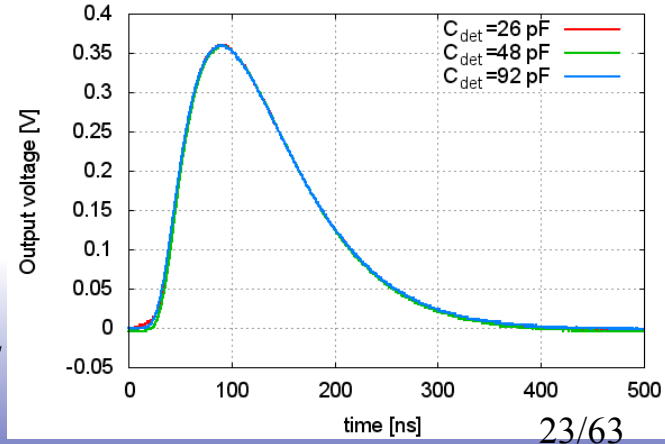
- Calibration mode - MIP sensitivity (~4fC)
- Physics mode - input charge up to 10 pC

Prototypes fabricated and tested

Power consumption 8.9 mW/channel

Event rate up to 3 MHz

Crosstalk < 1%



M. Idzik, Sz. Kulis, D. Przyborowski, "Development of front-end electronics for the luminosity detector at ILC", NIM A 608. 32 p.169-174, 2009

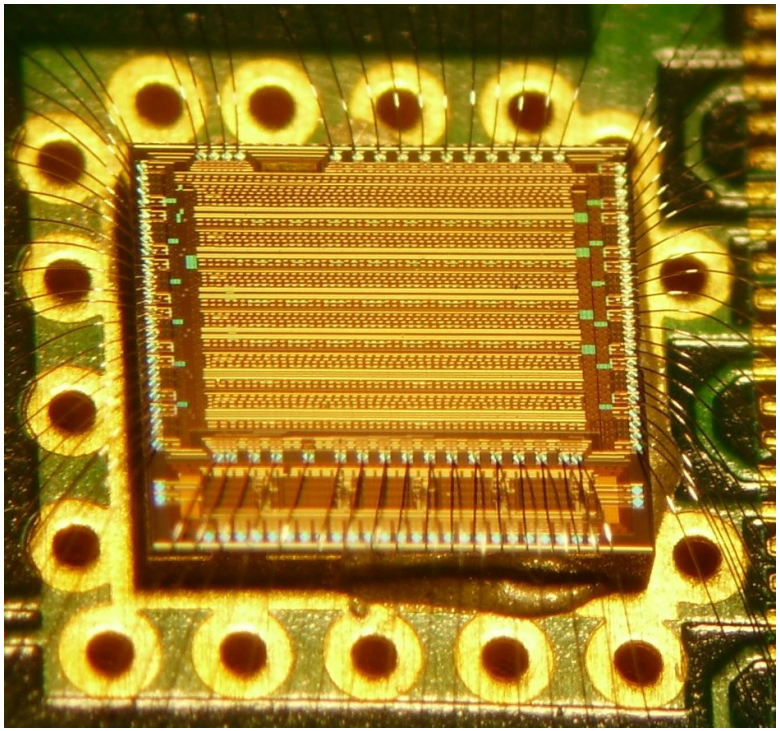
Pipeline ADC design

Parameters:

- 10-bit pipeline ADC
- 1.5 bit per stage architecture
- S/H stage + 9 pipeline stages
- Fully differential
- AMS 0.35um technology
- Area 0.87 mm^2
- Max. sampling rate 25Ms/s
- Power pulsing

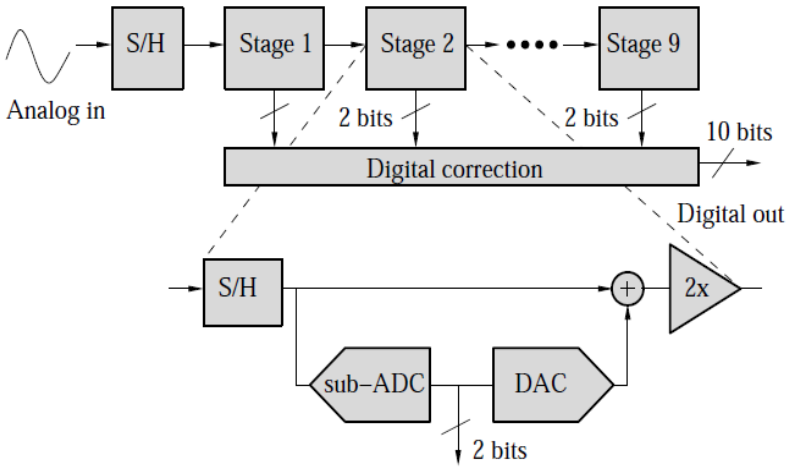
Results:

- Sampling rate 1kS/s-25MS/s
- Scalable power 0.85mW/MS/s
- SINAD~58 dB , ENOB=9.3 bit
- INL < 1 LSB
- DNL < 0.5 LSB

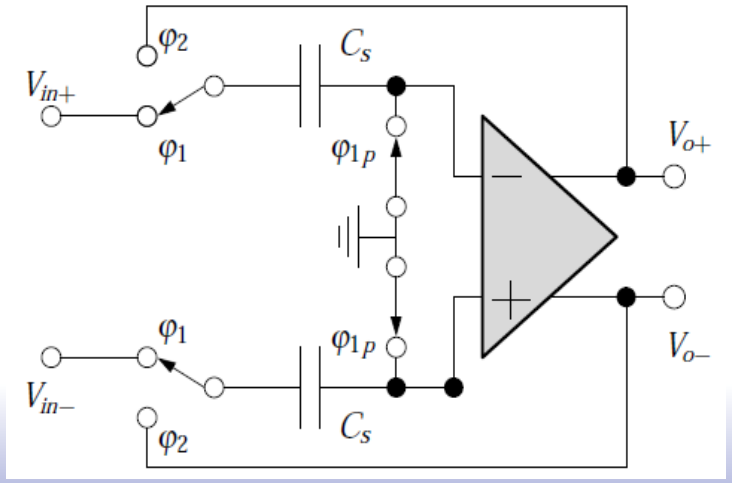


M. Idzik, K. Swientek,T. Fiutowski, Sz. Kulis, P. Ambalathankandy "A power scalable 10-bit pipeline ADC for Luminosity Detector at ILC", JINST 6 P01004, 2011

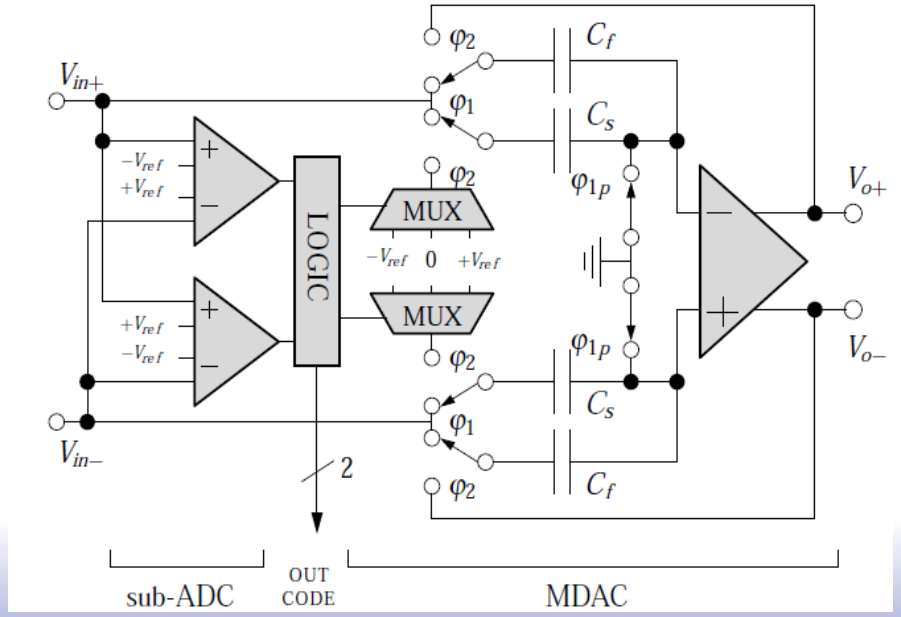
10-bit pipeline ADC



- High throughput – conversion rate = clock rate
- 1.5 bit per stage - redundancy reduces comparator requirements
- Fully differential architecture



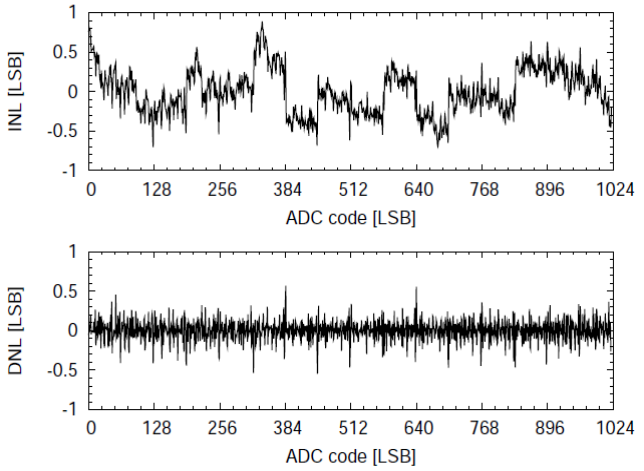
S/H stage

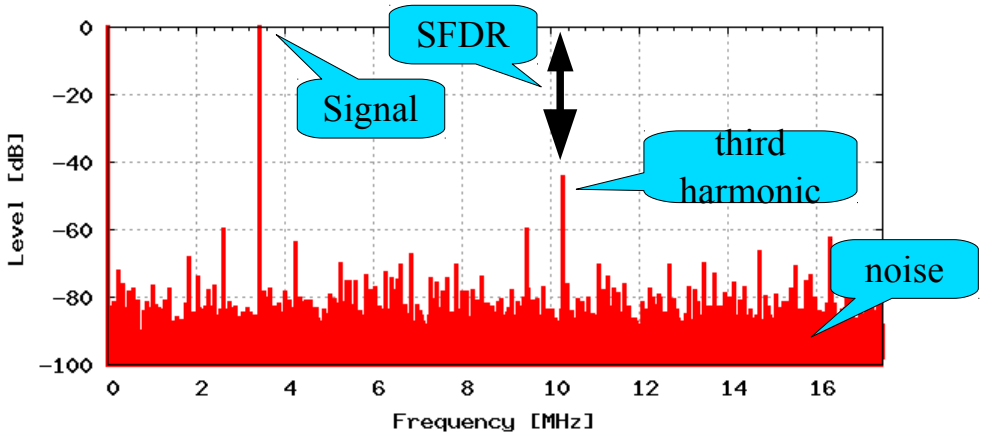


1.5 bit pipeline stage

Testing ADC demanding
scope and test pulse is not enough

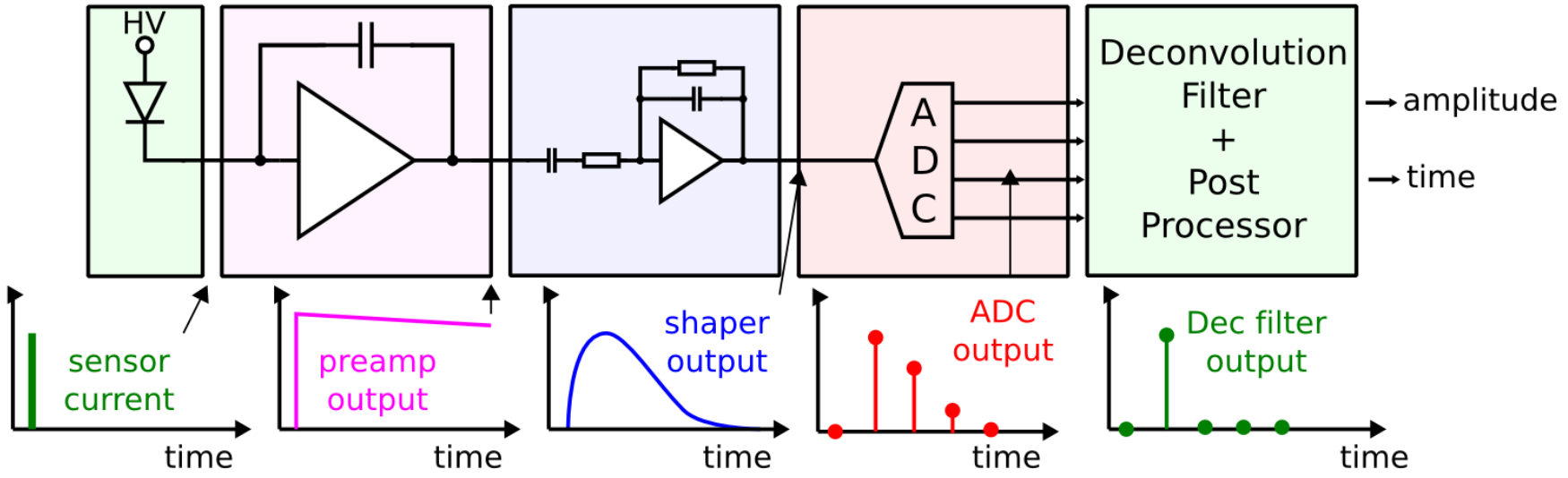
- Static tests – linearity measurements
  - INL, DNL
- Dynamic tests – dynamic FFT measurements
  - SNHR,THD, SINAD, SFDR
- Other tests
  - Power pulsing, crosstalk, etc...





Building the setup needs: differential input, sine generator with very low harmonics, etc... . Requests: equipped lab, expertise and time !

Deconvolution principle
for amplitude and time measurement



•Pulse at output of shaper v(t) is convolution of input signal (current from sensor – s(t)) and impulse response of readout chain h(t):

$$v(t) = \int_{-\infty}^{+\infty} h(t-x)\,s(x)\,dx$$

•Using data of continuously running ADC and taking advantage of known pulse shape one can perform invert procedure – **deconvolution** – to reconstruct event time and amplitude

Attractive for asynchronous systems like CLIC and beam-tests

Deconvolution principle...

Requirements :
- Simple hardware shaper realization
- Simple deconvolution formula

→ CR-RC shaper

Sensor pulse:

$$I_{sen}(t) = \delta(t)$$
$$I_{sen}(s) = 1$$

CRRC response

$$V_{sh}(s) = \frac{1}{(s + 1/\tau)^2}$$

τ - peaking time

Deconvolution formula (s domain)

$$D(s) = \frac{1}{V_{sh}(s)} = (s + 1/\tau)^2$$

$z = e^{sT}$

Deconvolution formula (z domain)

$$D(z) = z^2 - 2ze^{-T/\tau} + e^{-2T/\tau}$$

z^{-1} is a unit time delay
T – sampling interval

Deconvolution formula (time domain)

$$d(t_i) = z^{-1}\left(D(z)\right) = V_{sh}(t_i) - 2e^{-T/\tau} V_{sh}(t_{i-1}) + e^{-2T/\tau} V_{sh}(t_{i-2})$$

For $\tau = T$:

$$d(t_i) = V_{sh}(t_i) - 0.74\, V_{sh}(t_{i-1}) + 0.14\, V_{sh}(t_{i-2})$$

T. Bienz, "Strangeonium spectroscopy at 11GeV/c and Cherenkov ring...", Ph.D Thesis, Stanford 1990

Deconvolution with CR-RC shaping

$$d_i = V_i - 2e^{-T/\tau} V_{i-1} + e^{-2T/\tau} V_{i-2}$$

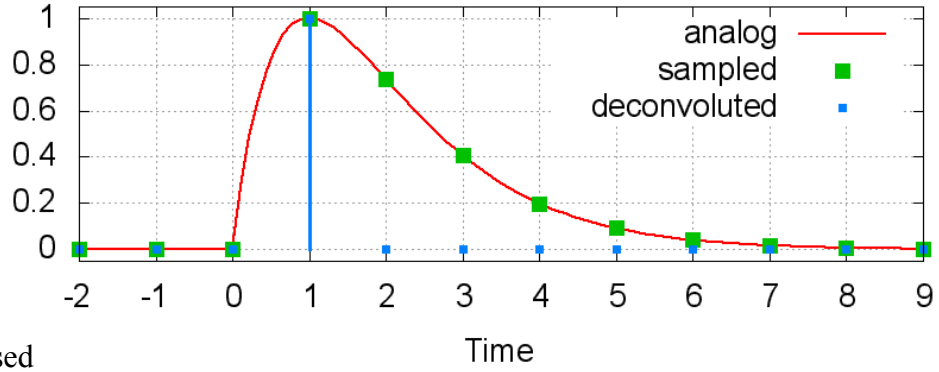
CR-RC, $T_{smp} = T_{peak} = 1$, amp = 1

- Only two multiplications and two additions (very fast and light !)
- Deconvolution produces non-zero data only when one or two first samples are on baseline, and second/third is on pulse
- **Initial time** of pulse is found from ratio of those samples

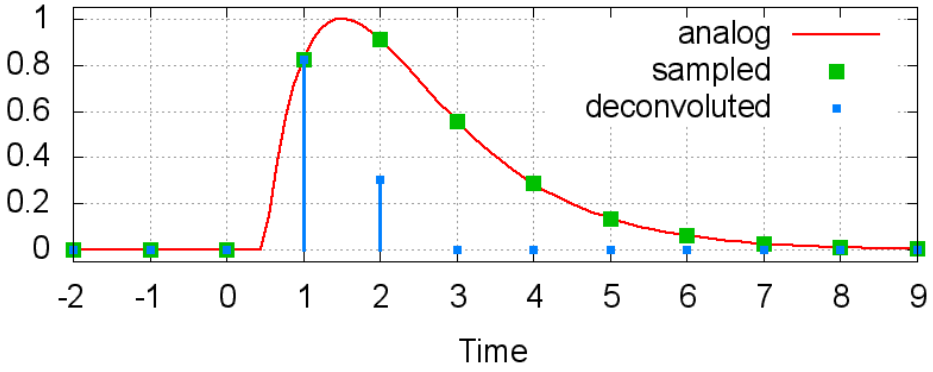
} Look Up Tables used
Can be done off-line

- **Amplitude** is found from sum of those samples, multiplied by time dependent correction factor
- Deconvolution reduces (infinite number) of CR-RC pulse samples to 1 or 2 non zero samples
- Very good pile-up rejection capabilities!

Synchronous sampling (t0 = int * Tsmp)

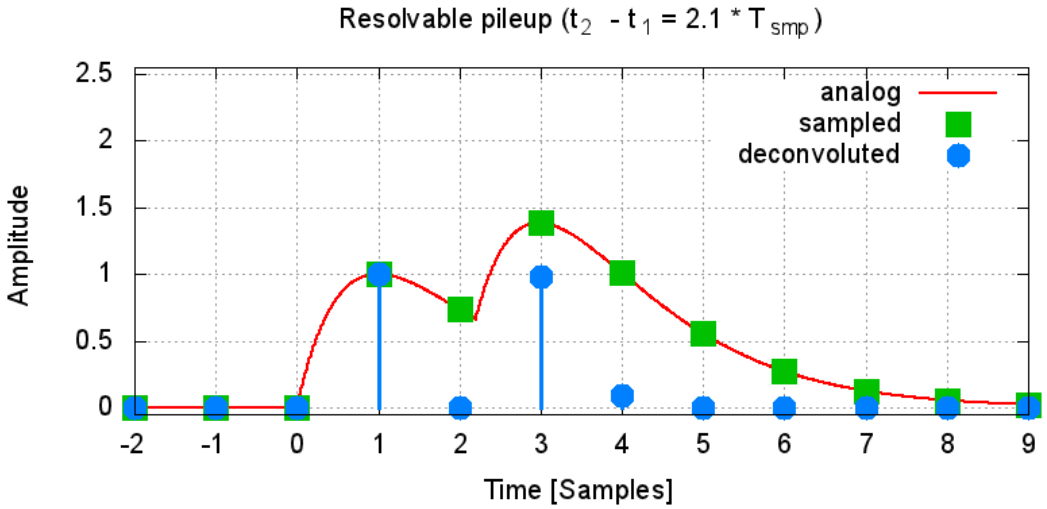


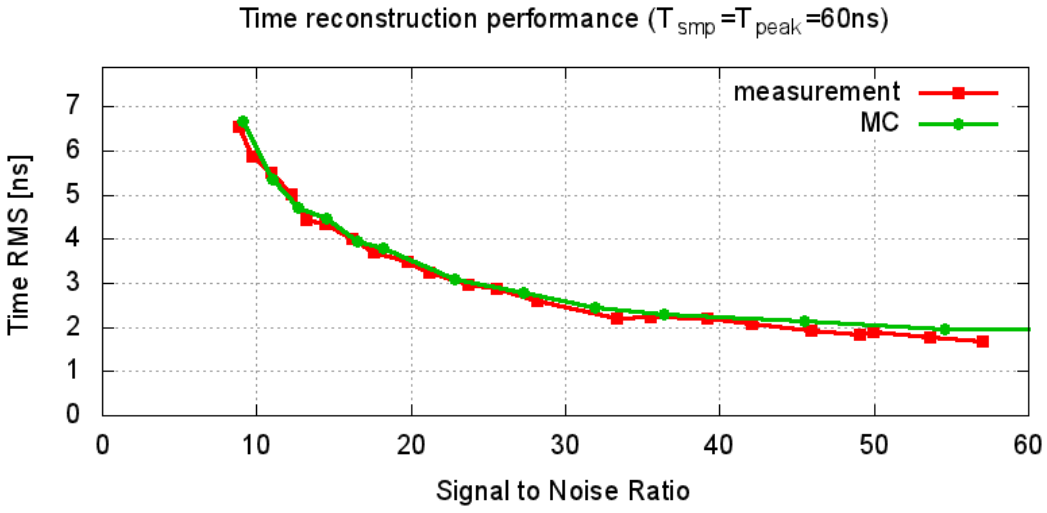
Asynchronous sampling (t0 = int * Tsmp)



CR-RC deconvolution properties

- Two events can be separated and precisely measured if they are distant 2-3 T_{smp}
- For $T_{peak} = T_{smp}$ = 60ns time resolution in range **2-7 ns** is obtained
- SNR is only slightly deteriorated
- Monte Carlo simulations fits well to measurements

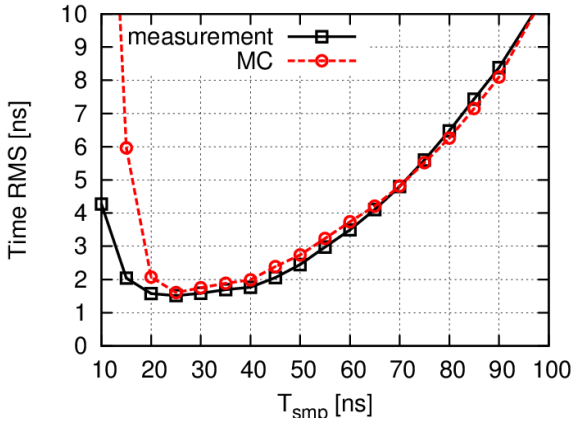


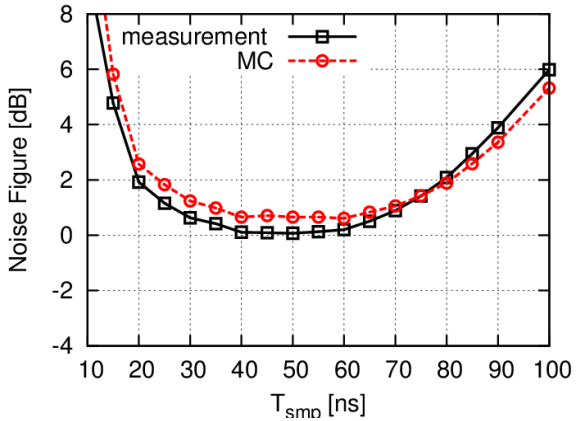


Sz. Kulis, M. Idzik "Study of readout architectures for triggerless high event rate detectors at CLIC" LCD-Note-2011-015

Deconvolution – example results

Results obtained for S/N~20 with the LumiCal front-end ASIC (CR-RC shaping, T_{peak}~60ns) presented before and with standard silicon pad sensor





$$NF = \frac{S/N_{in}}{S/N_{out}}[dB]$$

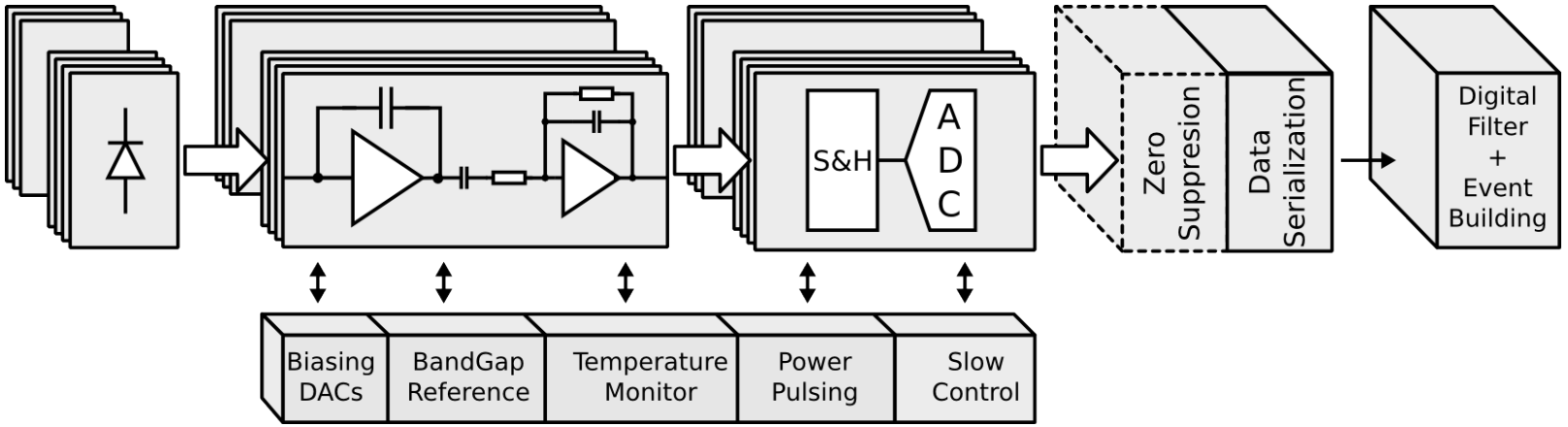
Good amplitude and time resolution - simulated in MC and confirmed experimentally!

Sz. Kulis, M. Idzik, "Triggerless Readout with Time and Amplitude Reconstruction of Event based on Deconvolution Algorithm ", Acta Physica Polonica B Proc. Suppl. 4 p. 49-58, 2011

Outline

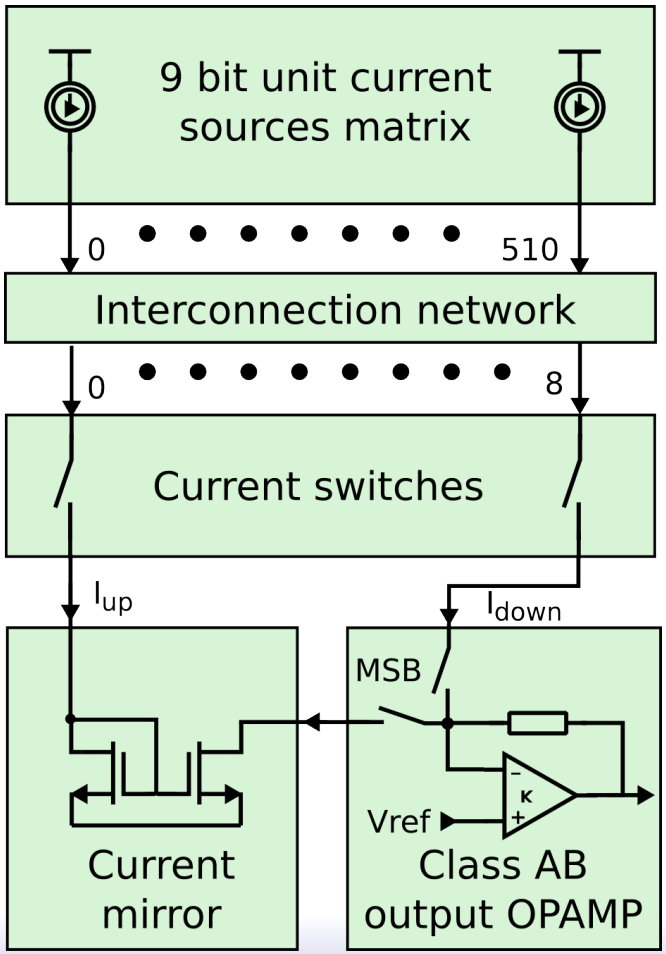
- Introduction to forward detectors in ILC/CLIC
- Front-end electronics signal processing
  - Noise, Preamplifier, Shaper, S/N and ENC, ADC
- Core ASICs and signal processing for LumiCal Detector
  - Preamplifier-Shaper ASIC
  - Pipeline ADC ASIC
  - Readout with deconvolution
- Integration of Complex Readout System for LumiCal
  - Peripheral blocks for multichannel system
  - Multichannel Digitizer ASIC
  - Prototype multichannel readout system
- Developments in progress...

SoC type multichannel readout



- ASIC advantages: **multichannel implementation , low power, small size**
- Complex multichannel system requires a number of peripherals:
  - DACs for votage and current biasing
  - Reference voltage - bandgap
  - I/O circuits – LVDS driver/receiver standard is often used
  - Temperature monitoring circuits
  - PLLs
  - Data serializers and deserializers
  - Other ...

Readout peripherals
10-bit low power high swing DAC



- 10th bit achieved by current reversing
- nonlinearities DNL & INL < 0.42 LSB
- ENOB = 9.8 bit
- settling time 0.5 – 2 µs
- power consumption < 0.6 mW
- tests completed

D.Przyborowski, M.Idzik, "A 10-bit low-power small-area high-swing CMOS DAC", IEEE Trans. Nucl. Sci., vol. 57, no. 2, pp. 292–299, 2010

Bandgap reference and temperature sensor

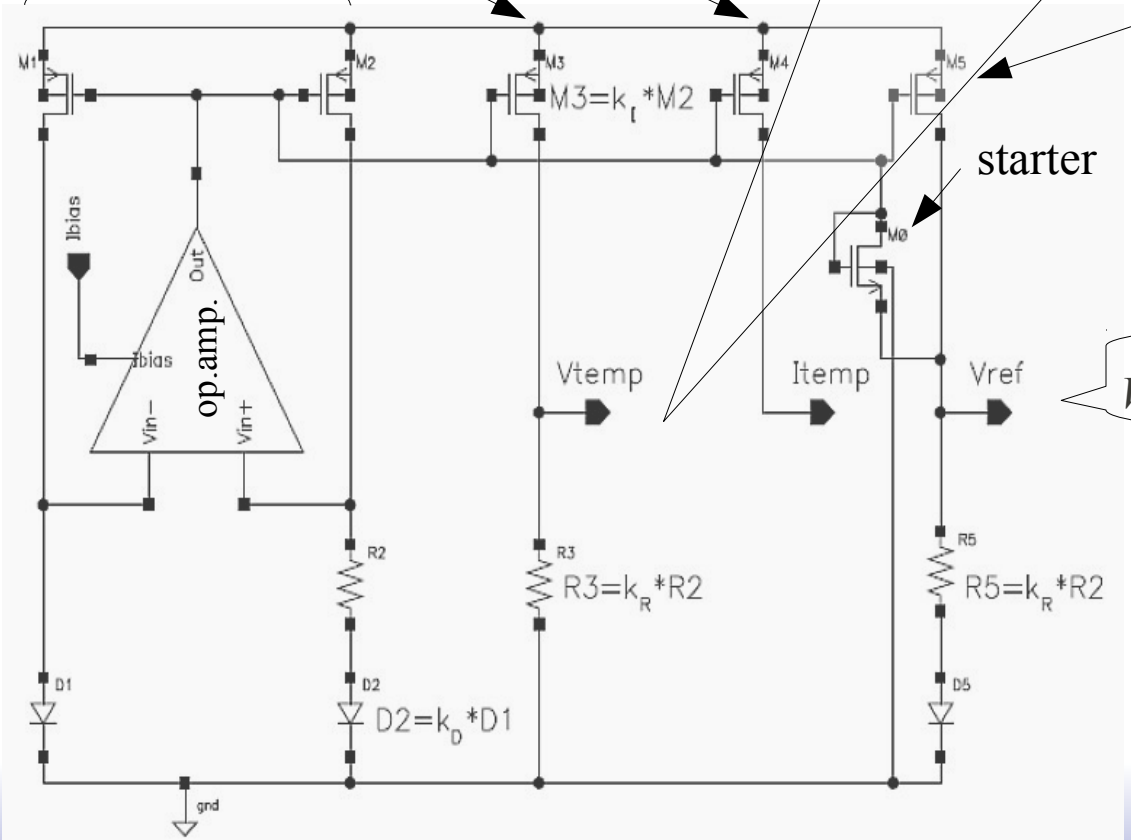
PTAT voltage branch

PTAT current branch

PTAT core

reference voltage branch

$$V_T = k_I k_R \left[V_{th} \ln\left(k_D\right) - V_{OS} \right] \approx 5.259 \frac{mV}{K} \cdot T - 26.25 \cdot V_{os}$$

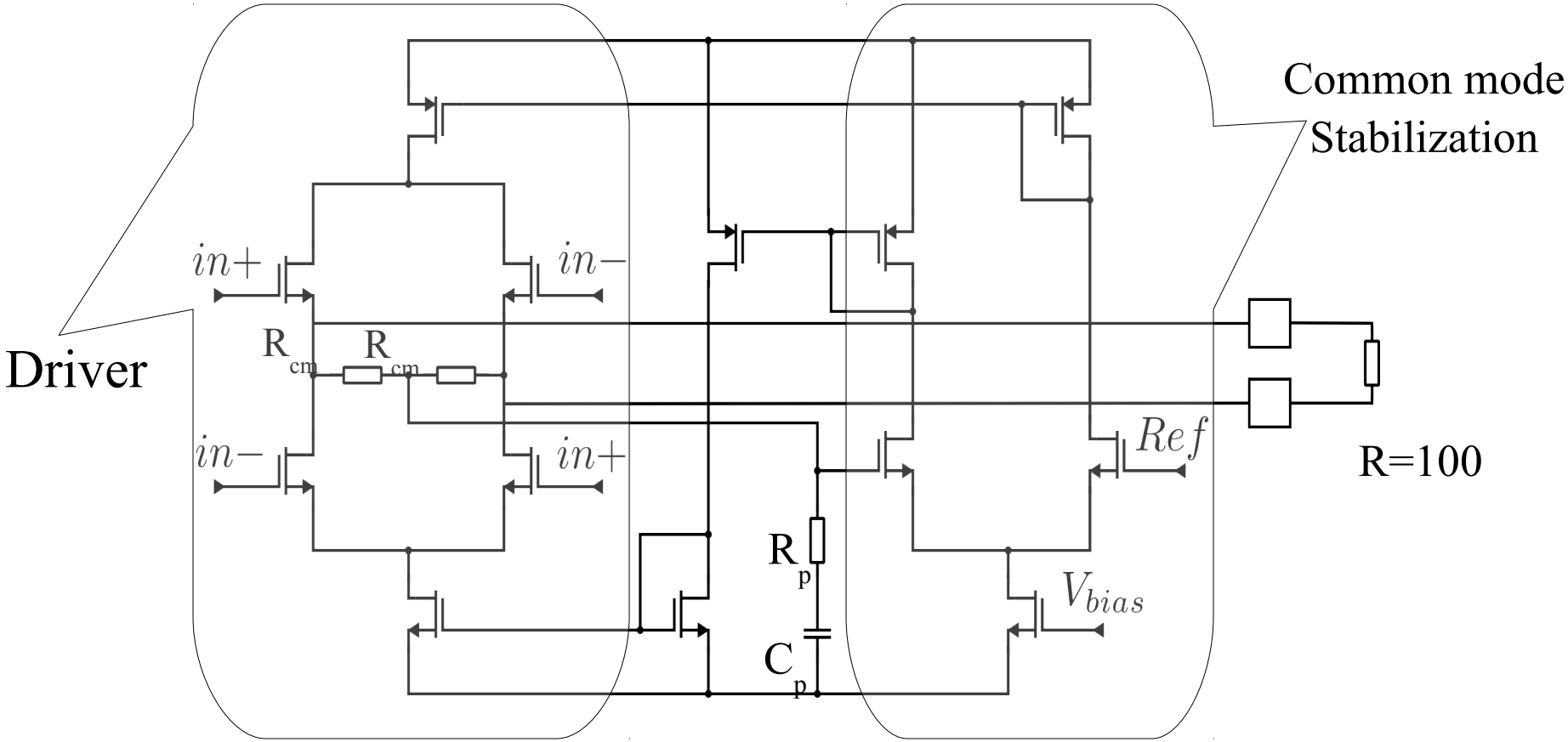


$$V_{ref} = E_g / q + (3+m) V_{th} \approx 1.2\,V$$

- Configuration implemented in IBM 0.25um and AMS 0.35um
- Power consumption < 100uW

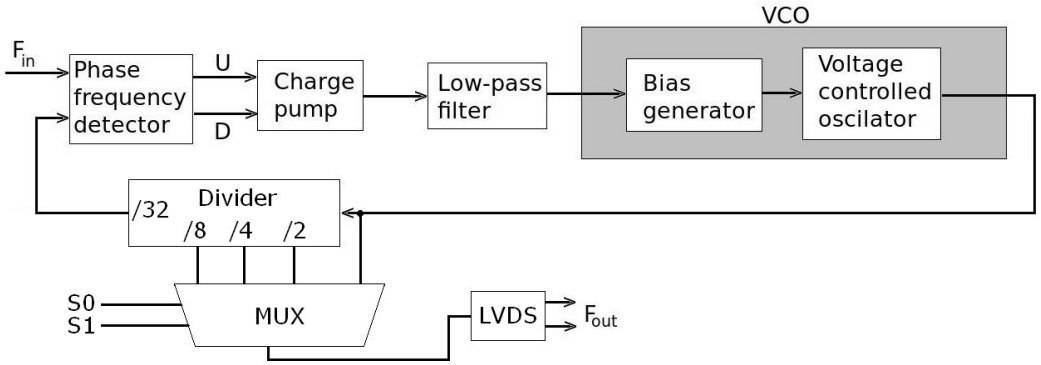
M. Idzik, M. Ornat, "Design and operation of low power temperature sensor – bandgap reference circuit in submicron technology", Proc. of 12th Int. Conf. MIXDES 2005 22-25 June Kraków Poland

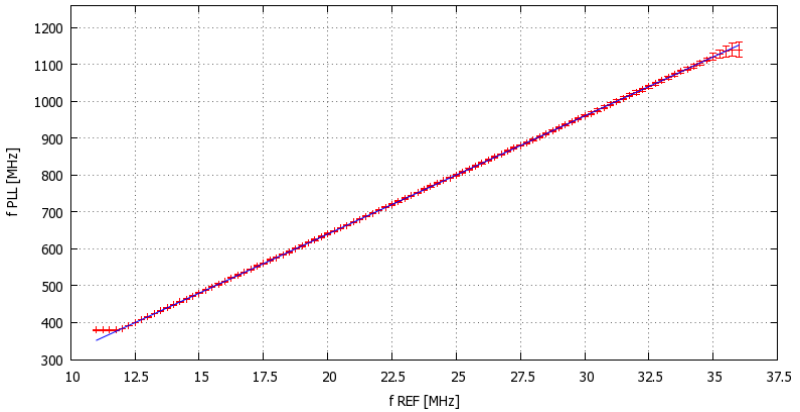
LVDS driver



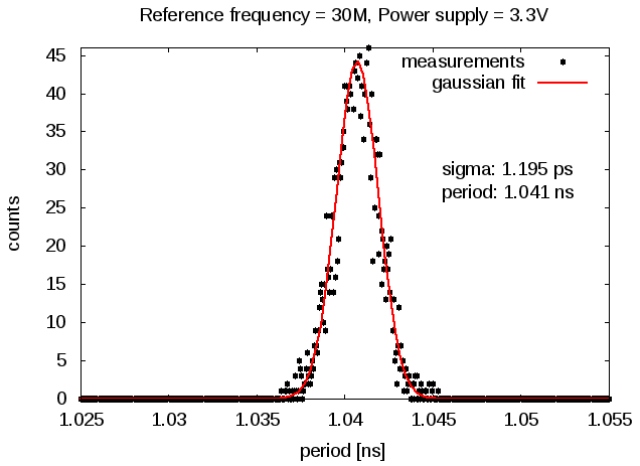
A. Boni, A. Pierazzi, D. Vecchi, LVDS I/O Interface for Gb/s-per-Pin Operation in 0.35 µm CMOS, IEEE J. Solid-State Circuits, vol. 36, no. 4, pp. 706–711, April 2001

Design of fast low power PLL





- Second order Phase Locked Loop
- "Current starved" Voltage Controlled Oscillator
- Input frequency multiplied by 32
- Binary controlled multiplexed LVDS output from divider
- AMS 0.35um, 160 x 140 um^2
- 4.5mW @1GHz



J. Moron, M.Firlej, M.Idzik, "Development of low-power PLL and PLL-based serial transceiver", presented at TWEPP 2011

Multichannel digitizer
complex system design example

AMS 0.35um technology

8 channels of 10 bit ADC

- 1.5 bit per stage pipeline architecture
- S/H stage plus 9 pipeline stages in each channel
- Layout with 200um ADC pitch

Digital multiplexer/serializer:

- Serial mode (~250MHz): one data link per all channels (max fsmp ~ 3 MSps)
- Parallel mode (~250MHz): one data link per channel (max fsmp ~ 25 MSps)
- Test mode: single channnel (max fsmp ~50 MSps)

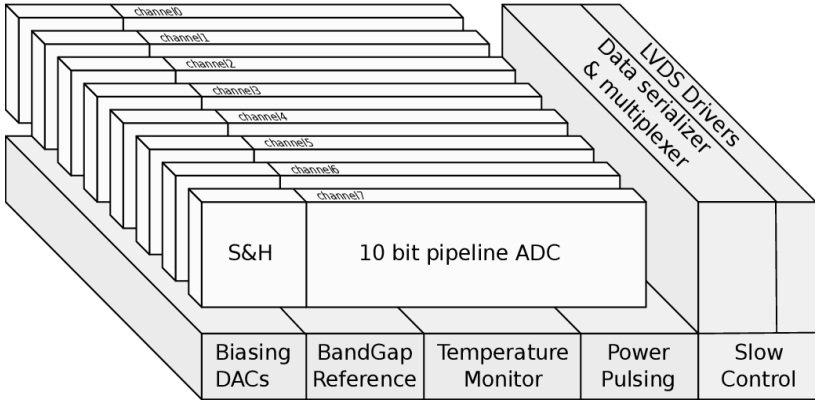
High speed LVDS drivers&receivers (<=1GHz)

Various (7) DACs for analog controls

Precise BandGap reference source

Temperature sensor

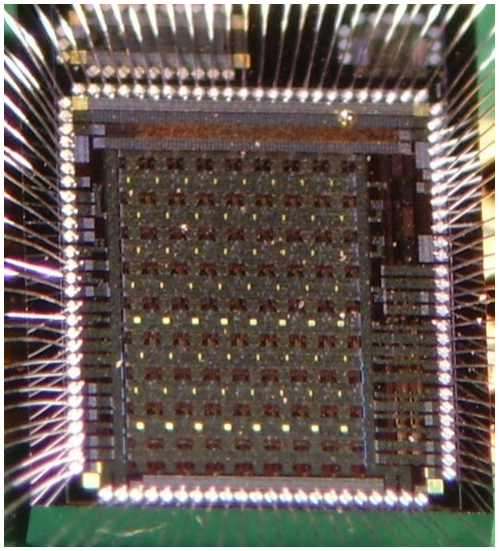
Power pulsing



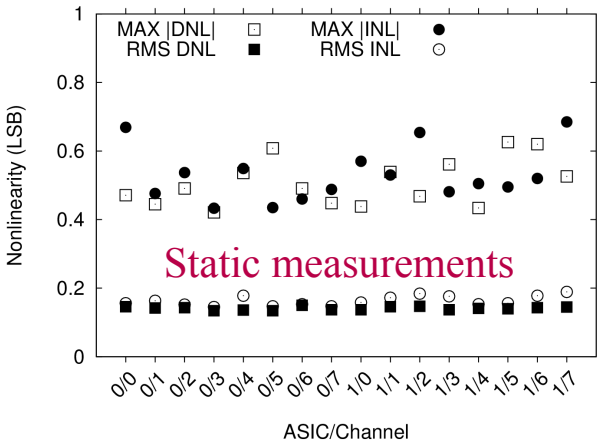
Multichannel Digitizer Results

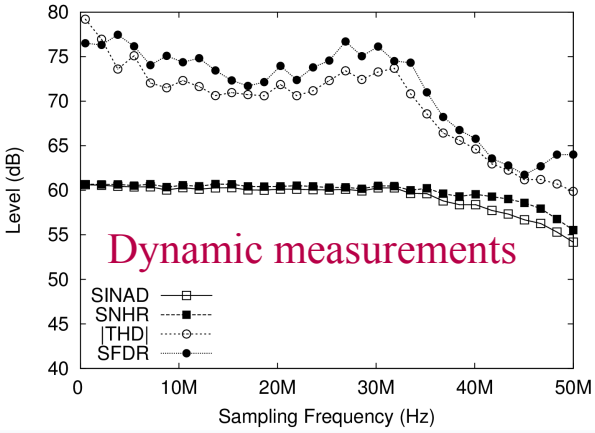
Performance:

- ENOB=9.7 bit up to 25 Ms/s (8 channels)
- Single ADC works up to 50 Ms/s
- Power consumption scales with sampling rate ~ 1.2mW/chan/MHz
- Excellent uniformity between the channels, gain spread < 0.1%
- Crosstalk < -80 dB
- Power pulsing embedded, t_{ON} ~3 us



Die size 2.6mm x 3.2mm





M. Idzik, K. Swientek, T. Fiutowski, Sz. Kulis, D. Przyborowski "A 10-bit multichannel digitizer ASIC for detectors in particle physics experiments", IEEE Trans. Nucl. Sci. accepted for publication

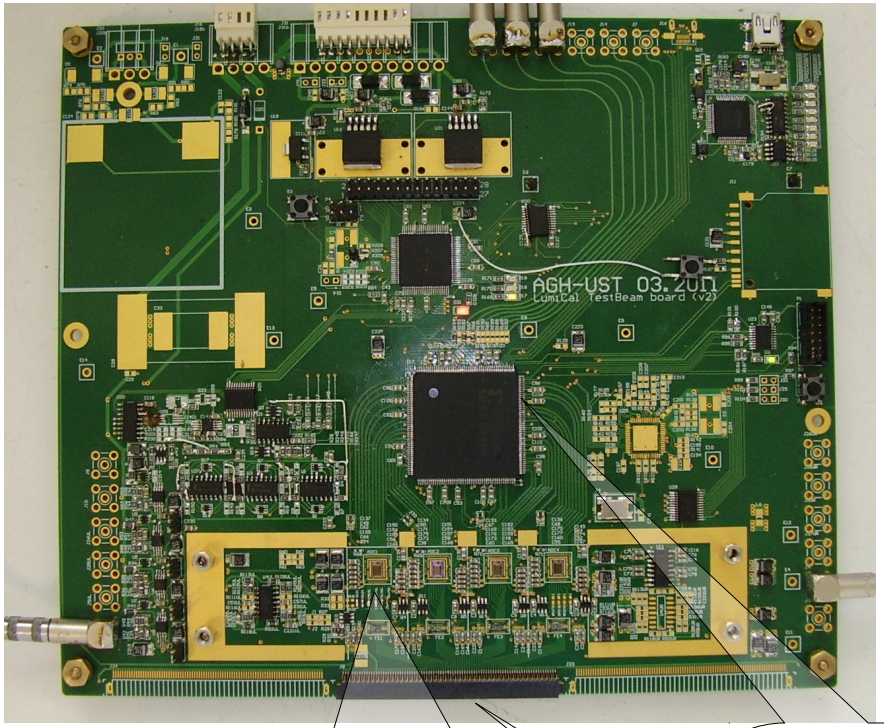
Comparison to commercial 10-bit multichannel ADCs

Parameter	This work TNS in print...	Kaviani et al. ESSCIRC 2002	AD9212	ADS5287	MAX1434
Nr channels	8	8	8	8	8
Serialization	per channel or per chip	per chip	per channel	per channel	per channel
Architecture	10-bit pipeline	10-bit pipeline	10-bit pipeline	10-bit pipeline	10-bit pipeline
Technology	0.35 μm CMOS	0.25 μm CMOS	-	CMOS	BiCMOS
Power supply	3.3 V	2.5 V	1.8 V	3.3 V_A, 1.8 V_D	1.8 V
Max. f_{sample}	25 MS/s	20 MS/s	65 MS/s	65 MS/s	50 MS/s
Input range	2 V_{pp}	-	2 V_{pp}	2 V_{pp}	1.4 V_{pp}
Total power per channel	~1.2 mW/MS/s +I/O (<15%)	41 mW @20MS/s	100 mW @65MS/s 68 mW @40MS/s	74 mW @65 MS/s 46 mW @30 MS/s	96 mW @50MS/s
Area	8.2 mm^2	4 mm^2	9x9 mm^2 (package)	9x9 mm^2 (package)	14x14 mm^2 (package)
INL	<0.68 LSB	-	<0.5 LSB	<1 LSB	<1 LSB
DNL	<0.62 LSB	-	<0.4 LSB	<0.55 LSB	<0.5 LSB
SINAD	~60.3 dB	54.3 dB	≥60 dB	≥60.4 dB	≥60 dB
ENOB	9.7	8.7	≥9.7	≥9.7	≥9.7
$T_{power\ on}$	≤10 T_{clk} ~3 μs @ILC	-	375 μs	-	100 ms

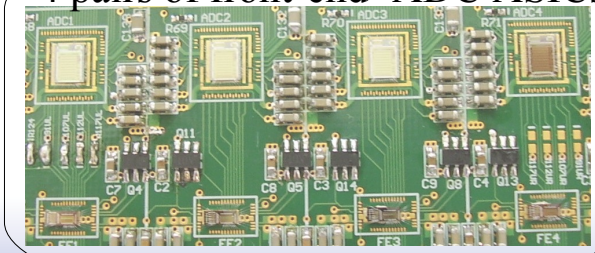
Even if designed in rather old technology our design compares quite well to the state of the art commercial multichannel ADCs

Complete readout system example

not only ASICs make the system...



4 pairs of front-end+ADC ASICs



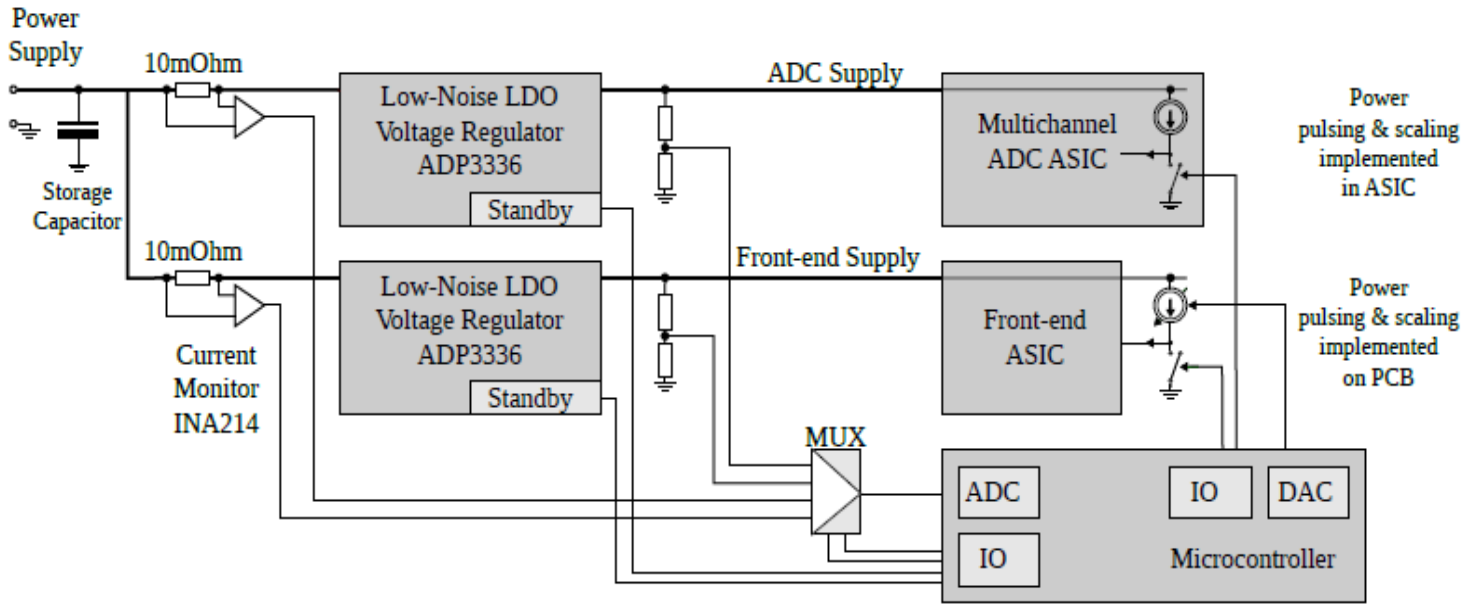
Data concentrator
Xilinx Spartan 3E

sensor connector

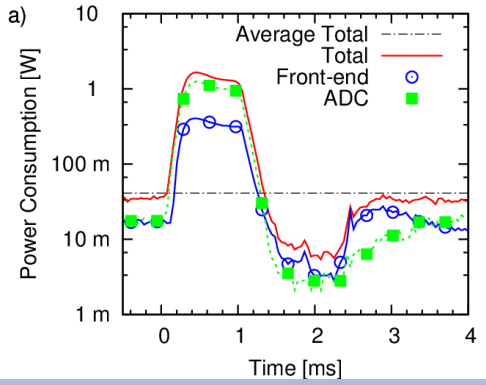
- 32 channels fully equipped channels (Front-end +ADC) + FPGA data conc.
- ADC sampling rate is up to 20 MS/s (6.4 Gbps)
- Extended trigger mechanism
  - External CMOS / LVDS
  - Self triggering on ADC values
  - Software
- Data can be transferred using USB
- Signal handshaking with Trigger Logic Unit (TLU)
- ADC Clock source
  - Internal (asynchronous with beam operation)
  - External (beam clock used to synchronize with beam) ILC mode

Sz. Kulis, A. Matoga, M. Idzik, K. Swientek, T. Fiutowski, D. Przyborowski "A general purpose multichannel readout system for radiation detectors", JINST 7 T01004 2012

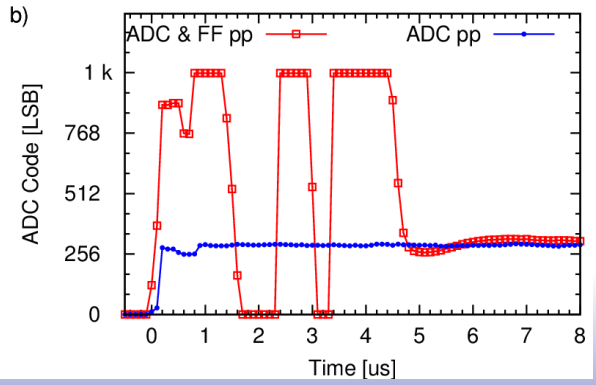
Power delivery and pulsing



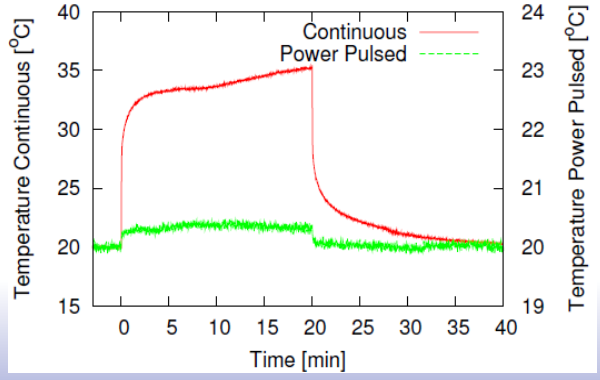
Performance with power pulsing



Front-end power consumption



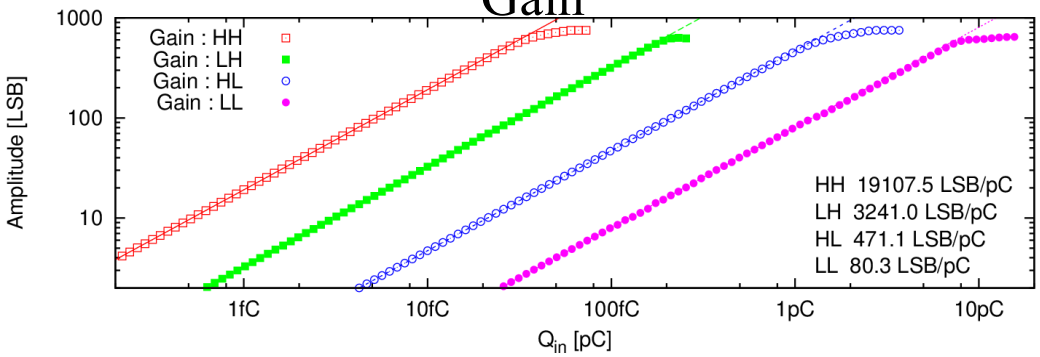
Front-end switch ON time



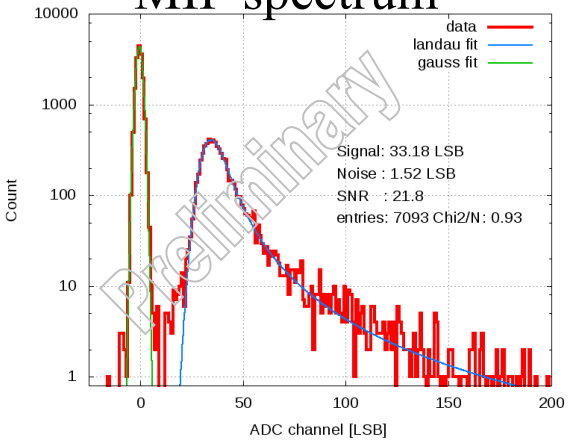
Digitizer temperature

LumiCal Detector prototype in FCAL beam-test

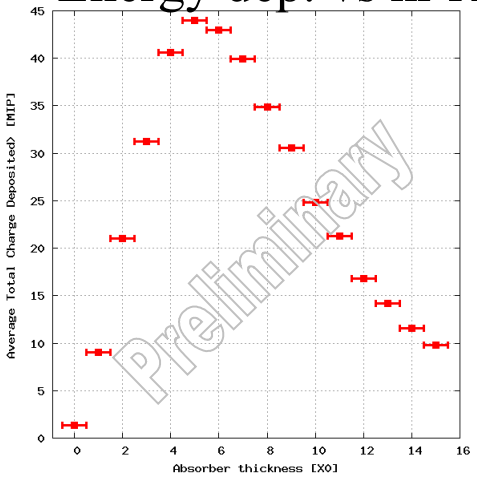
Gain



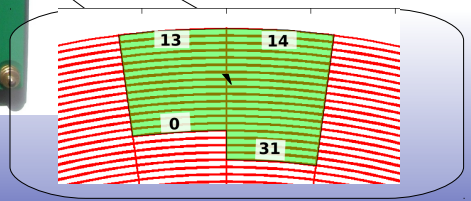
MIP spectrum



Energy dep. vs nr X0



Instrumented Area



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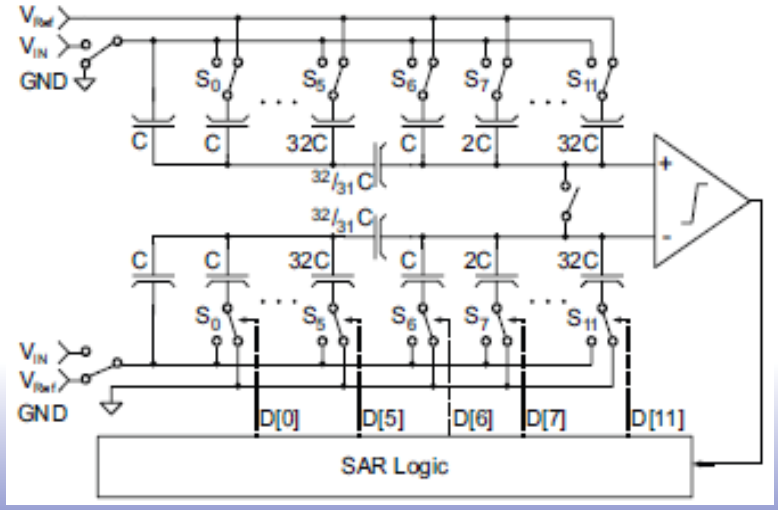
  - Prototype multichannel readout system
- Developments in progress...

Development of ASICS for new readout chain in progress...

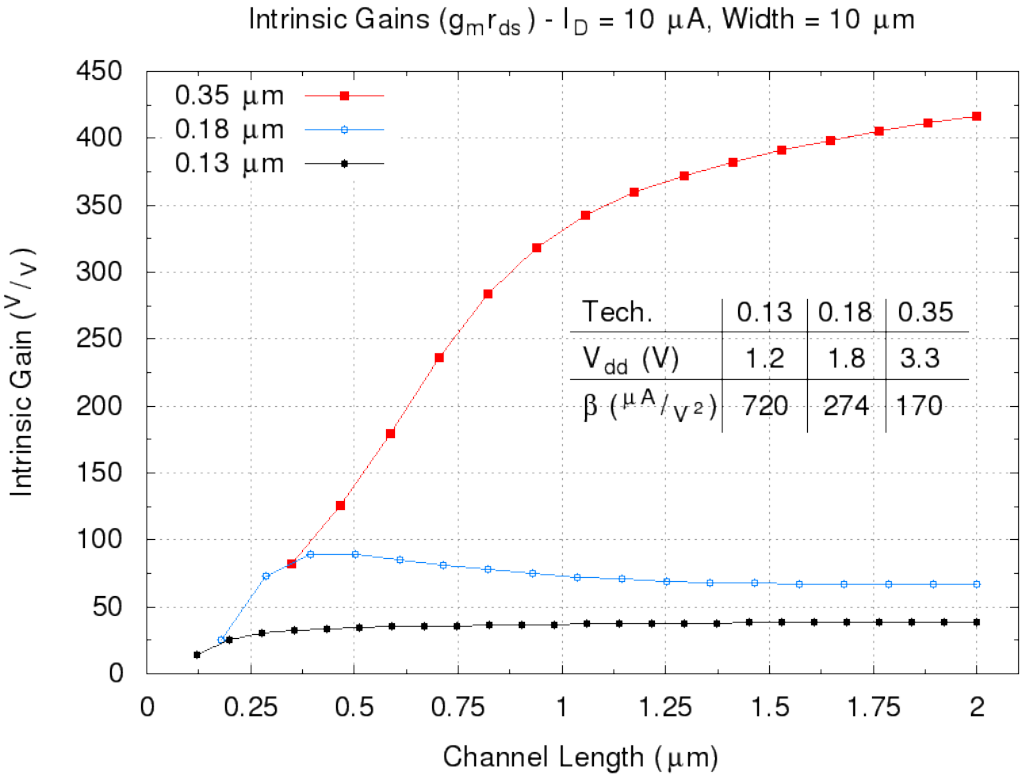
- Change of technology and/or architecture to get: lower power, higher speed, radiation hardness
- Design of new front-end in IBM 130nm in progress
  - Last specifications under discussion...
  - Expected drop in power ~5 times
- First prototype of SAR ADC in IBM 130nm just submitted
  - Segmented DAC architecture
  - Expected drop in power >=20 times
  - Max. sampling rate >=40Ms/s (LHC rate)
  - The only analog part – comparator,
    (fits to modern submicron CMOS)
  - Capacitive DAC network
    (serves as sampling capacitance)
  - Asynchronous logic improves speed



Design in modern CMOS

Comparison of CMOS generations

NMOS intrinsic gain



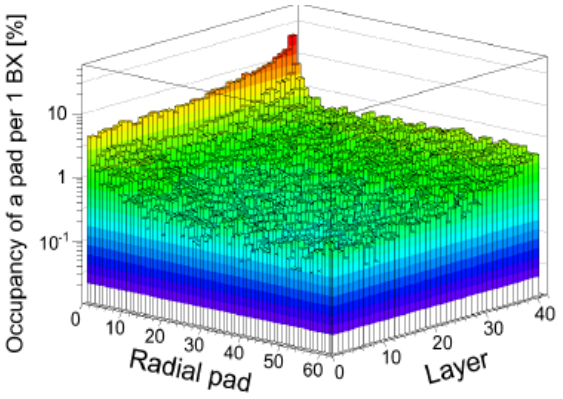
Modern CMOS processes offer higher speed but lower gain !
Design more difficult!

Architecture for very high rates at CLIC
Gated integrator + CDS

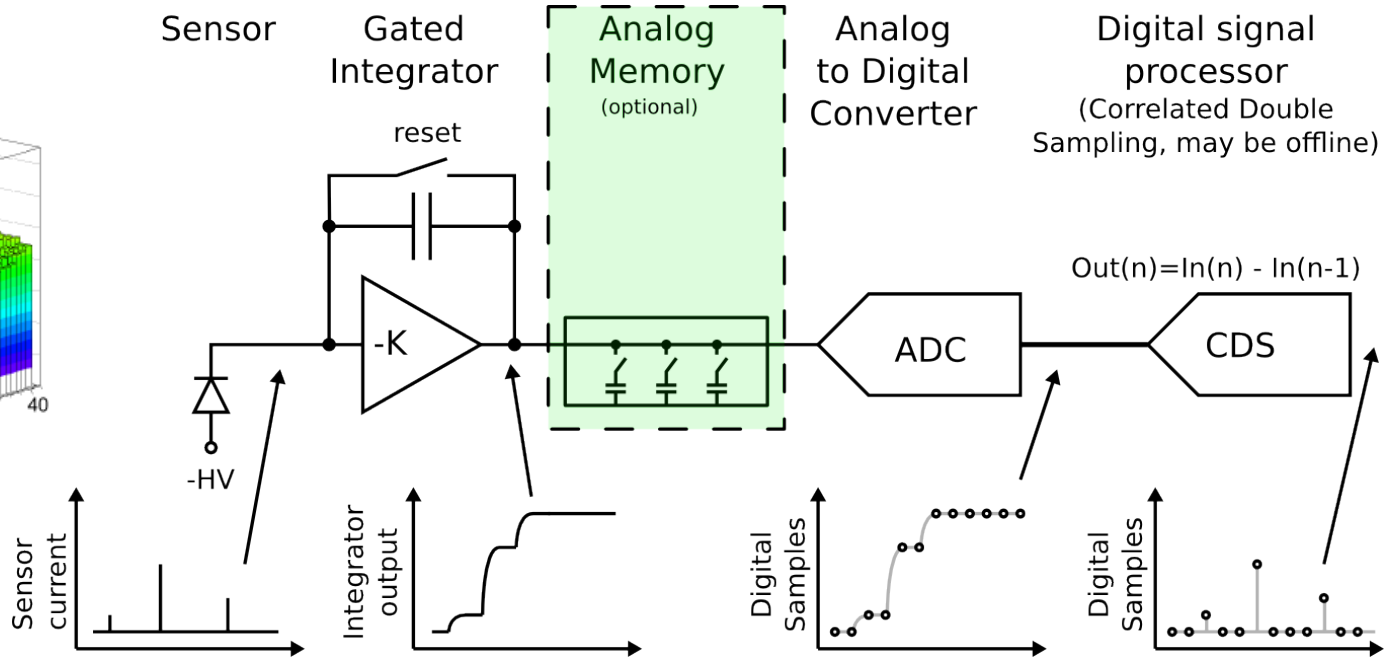
Operation:

- Reset before the beam train
- Integration during the beam train (156ns for CLIC)

Occupancy of LumiCal pads due to incoherent pairs



"Physics and Detectors at CLIC", CLIC Conceptual Design Report 2011



Sz. Kulis, M. Idzik, "Study of readout architectures for triggerless high event rate detectors at CLIC", CERN LCD-Note-2011-015 2009

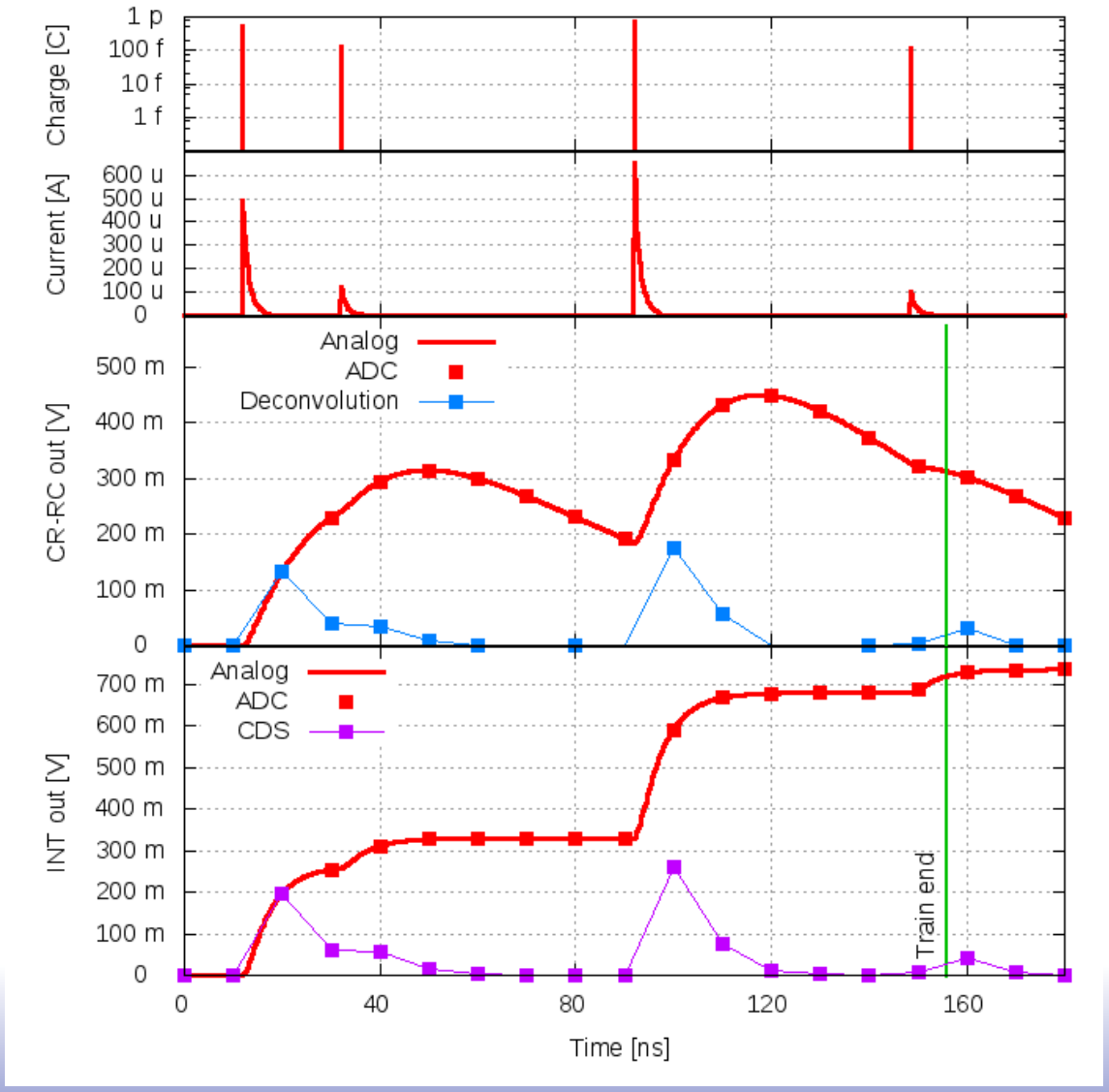
Readout example

δ-like charge deposition →

Pulse from the sensor →

Readout with CR-RC shaping and deconvolution → T_{peak}=30ns, T_{smp}=10ns

Readout with gated integrator and CDS → T_{int}=5ns, T_{smp}=10ns



Occupancy ~ 1-1.5% per PAD per BX

Summary

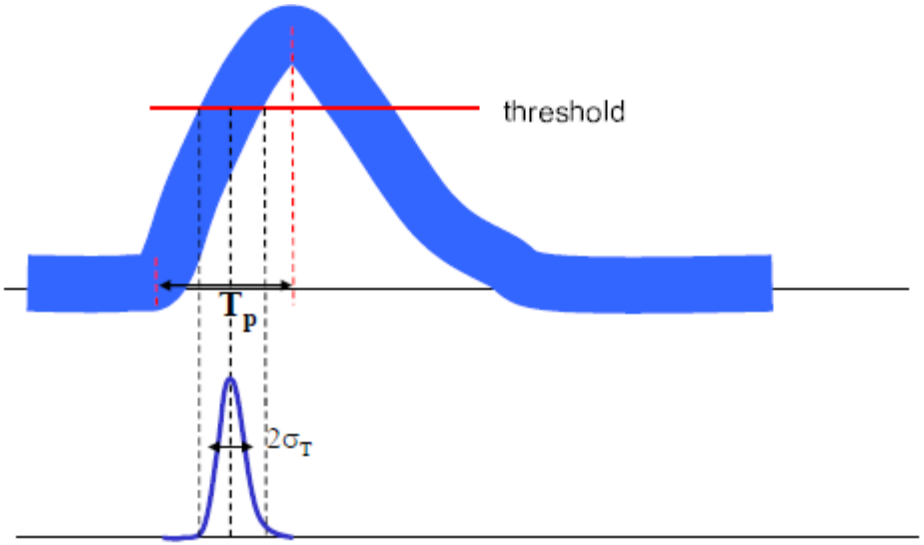
- As seen on LumiCal case, the forthcoming experiments are setting more and more challenges for: high speed, low power, concurrent amplitude&time measurements, radiation hard...
- To fulfill growing demands the ASICs need to be more complex (approaching SoC) and deep submicron technologies need to be used.
- Deep submicoron technology means limited analog features – more difficult design, growing part of digital signal processing (DSP), and of course higher price.
- Growing demands for DSP opens the possibility for higher integration of ASICs and FPGAs (faster development and much cheaper) for present and future readout systems.

Thank you for attention

Signal timing measurements

To measure the time of signal occurrence, fast discriminator is added after shaper output. Main uncertainties are:

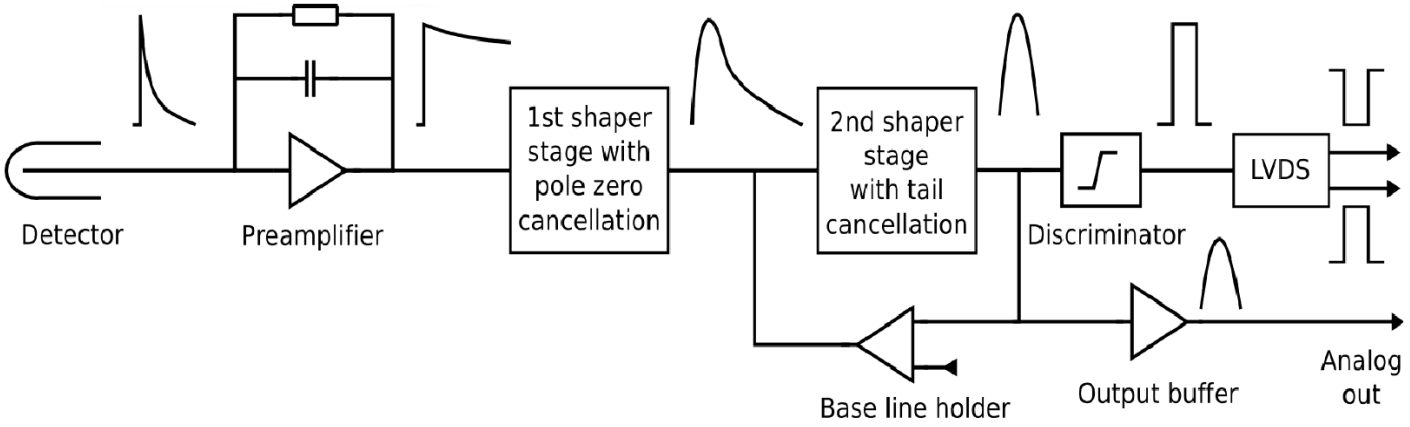
- Time jitter error
  - Due to noise



- Time walk
  - Due to amplitude variation

Instead of S/N the slope to noise ratio is optimized. Steeper slope – better timing resolution – worse amplitude resolution

Example front-end under developed for straw tubes in PANDA

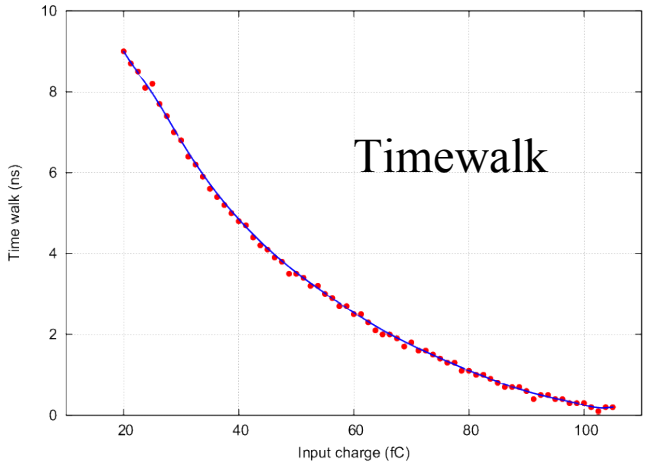


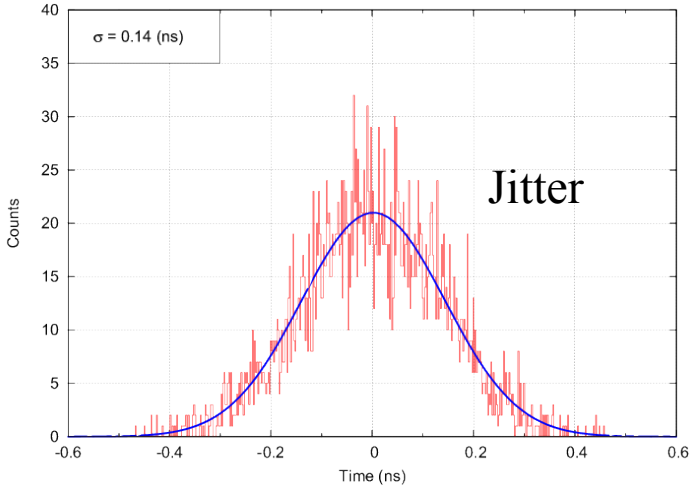
Readout chain

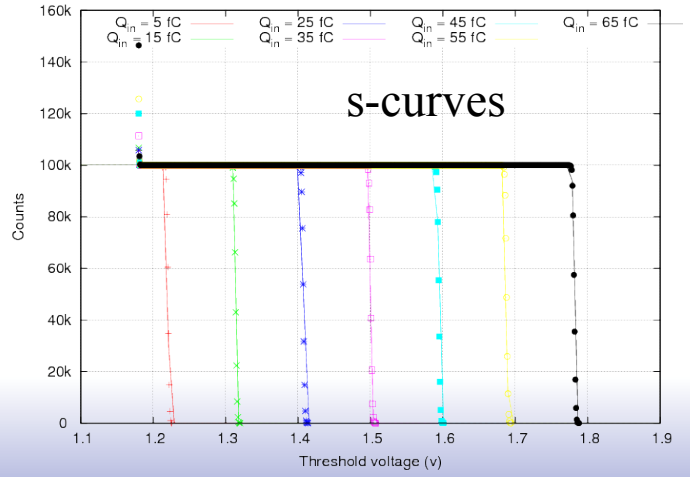
- **Preamplifier**
- **Shaper**
- Tail cancellation
- Baseline holder (BLH)
- **Leading edge discriminator**
- Fast LVDS output
- Analog output

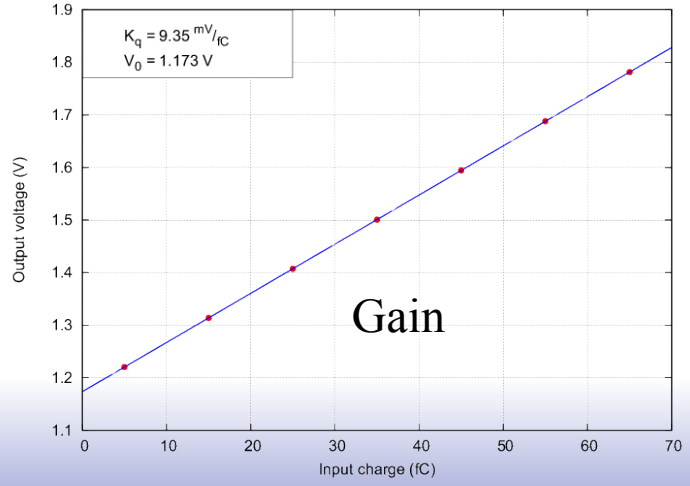
Design goals:
Timing measurement (~1ns)
Amplitude measurements

Straw ASIC-first measurement

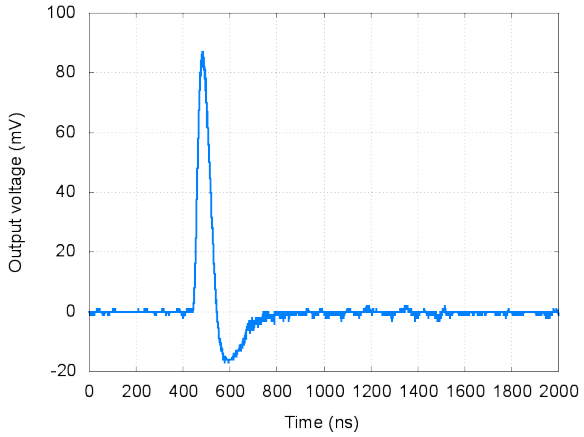


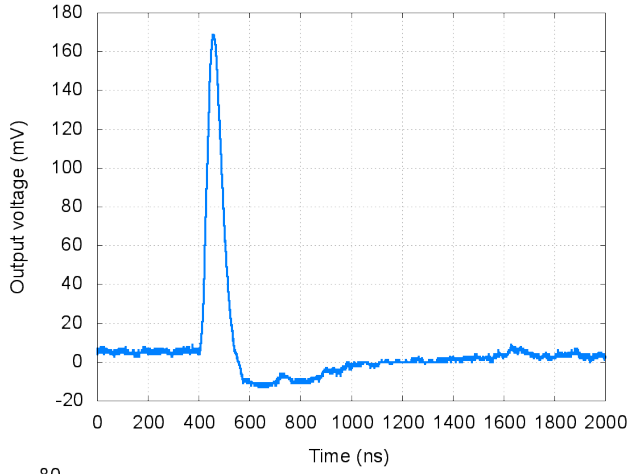


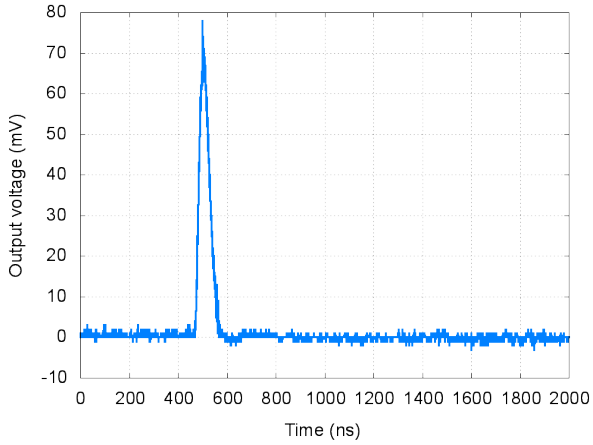


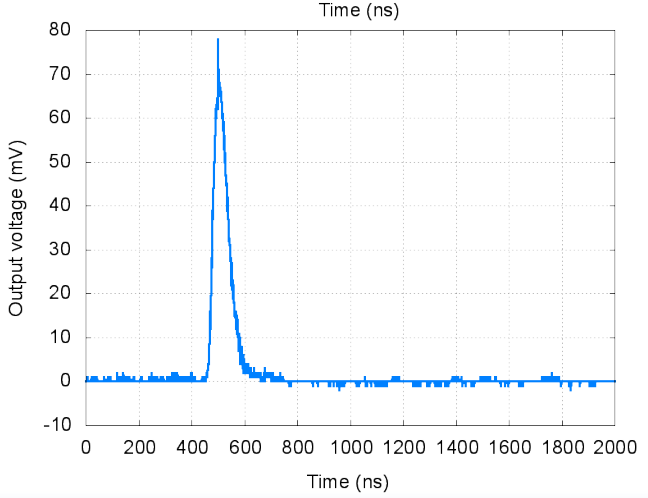


Straw ASIC – tail cancellation





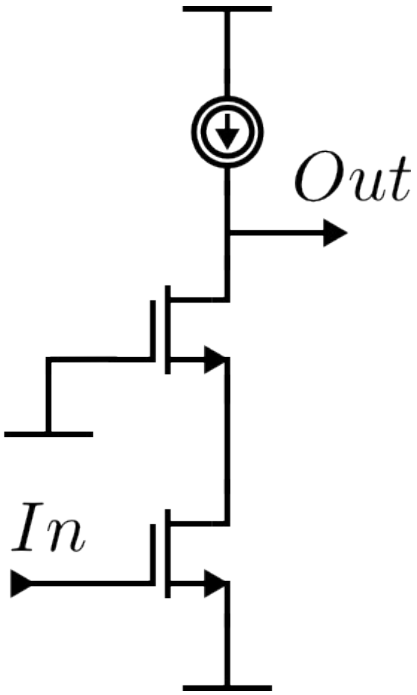


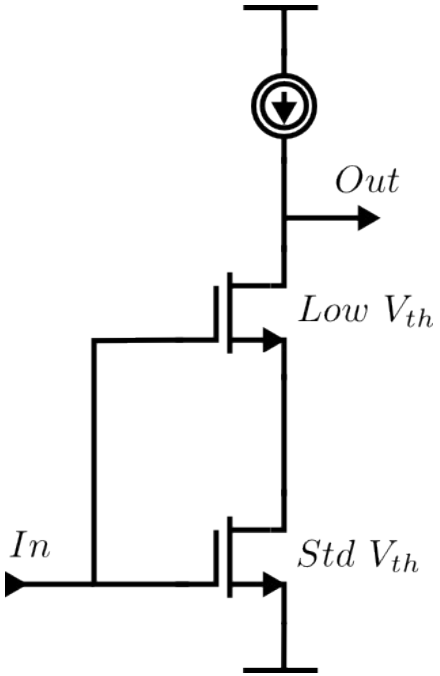


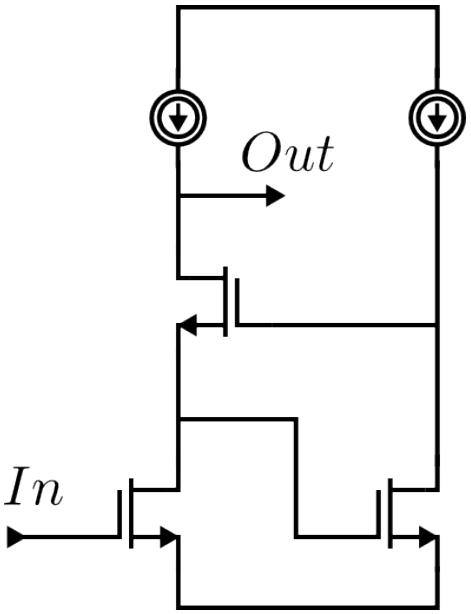
Tail cancellation network has ~4000 possible settings. Here only few are shown.

Amplifier in modern CMOS
some ideas...

Cascode amplifier Self-Cascode Regulated cascode







Low intrinsic gain and small supply voltage make amplifier design difficult !

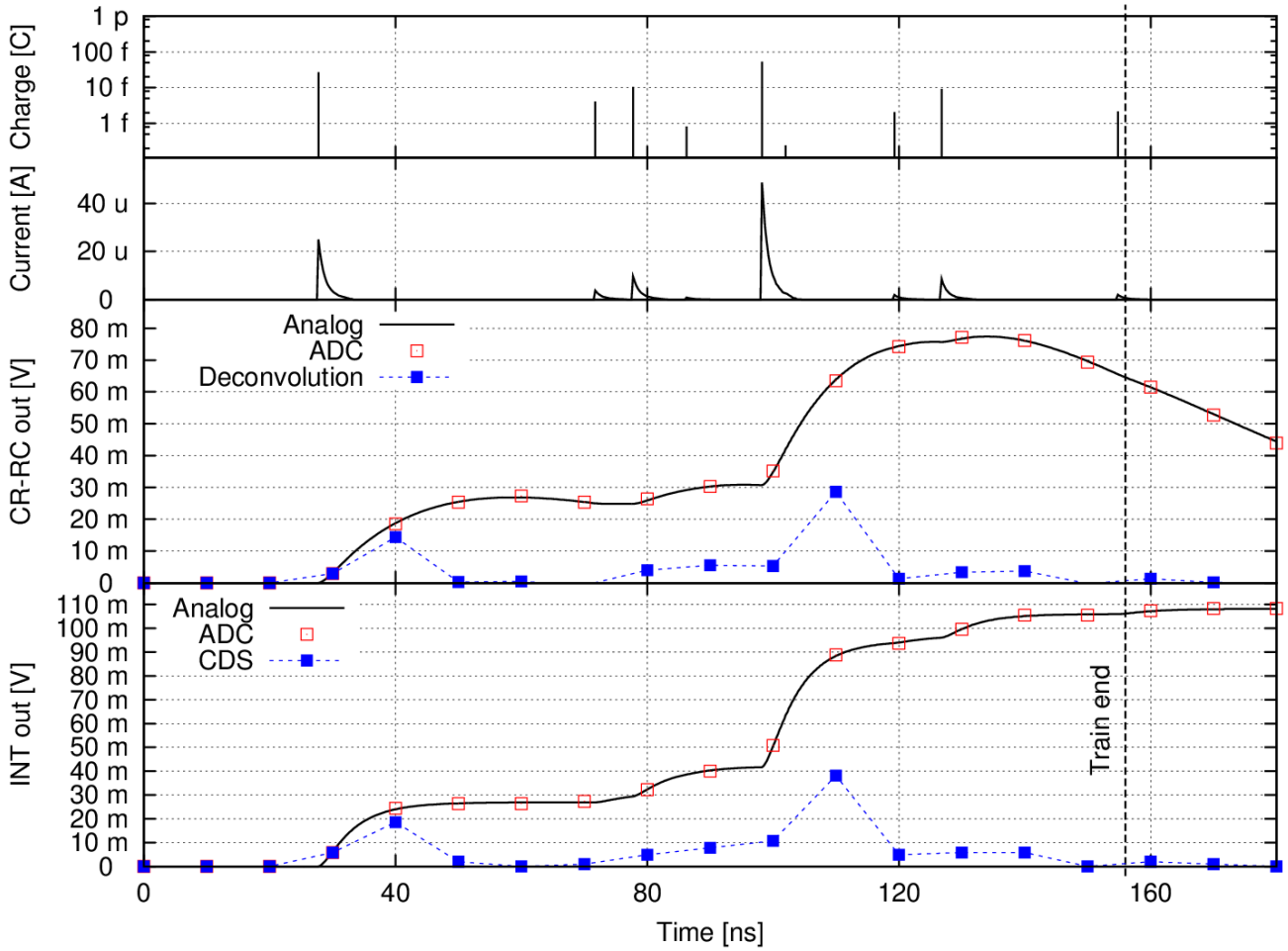
Readout example

δ-like charge deposition →

Pulse from the sensor →

Readout with CR-RC shaping and deconvolution → T_{peak}=30ns, T_{smp}=10ns

Readout with gated integrator and CDS → T_{int}=5ns, T_{smp}=10ns



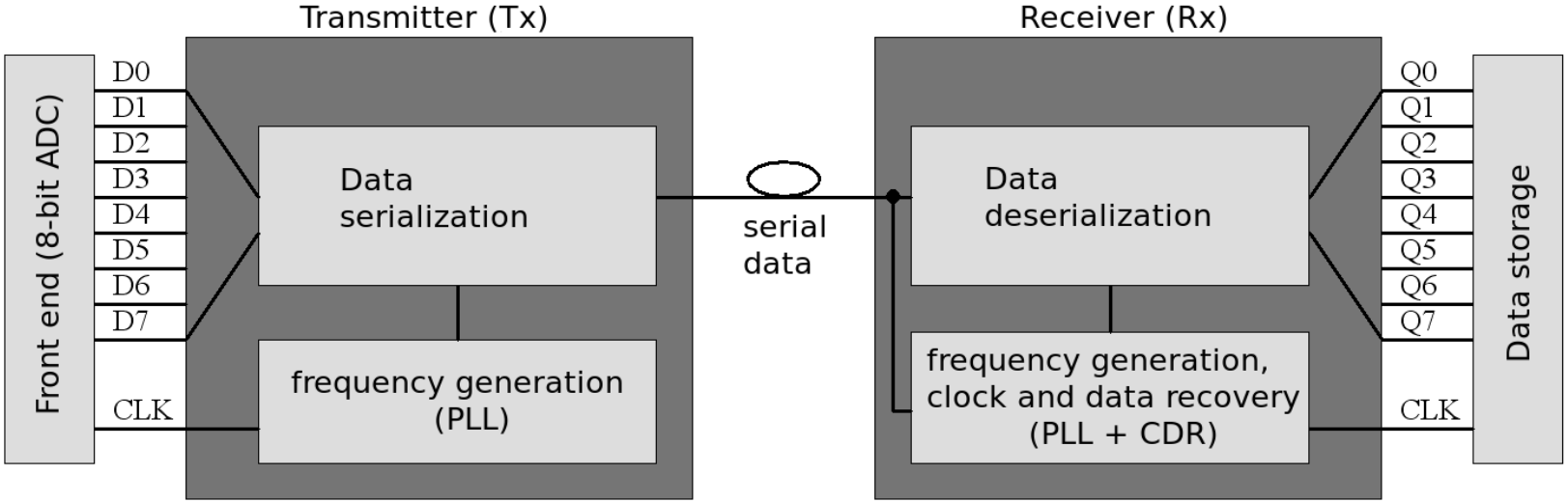
Transceiver architecture

Transmitter (Tx)

- Parallel synchronous to serial asynchronous data converter
- Up to ~1GHz output clock from PLL

Receiver (Rx)

- Serial asynchronous to parallel synchronous
- PLL clock generated and synchronized with transmitter by CDR (burst mode) circuit

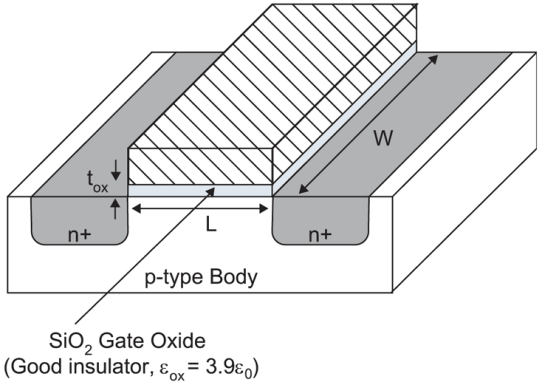


J. Moron, M.Firlej, M.Idzik, "Development of Fast Transceiver for Serial Data Transmission in Luminosity Detector at Future Linear Collider", Acta Physica Polonica B, Proc. Suppl. 4 p.41-48 2011

CMOS technology scaling
more channels, lower power, smaller size

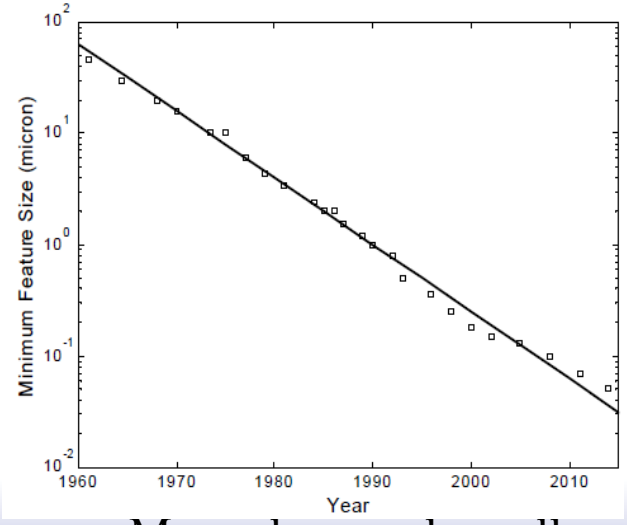
Relations for long channel devices

Parameter	Constant-field scaling	Generalized field scaling
Physical dimensions: L, W, Tox, wire pitch	1/S	1/S
Body doping concentration	S	E/S
Voltage	1/S	E/S
Circuit density	$1/S^2$	$1/S^2$
Capacitance per circuit	1/S	1/S
Circuit speed	S	S (goal)
Circuit power	$1/S^2$	E^2/S^2
Power density	1	E^2
Power-delay product	$1/S^3$	E^2/S^3



S – scaling factor

E=V/S – normalized electric field

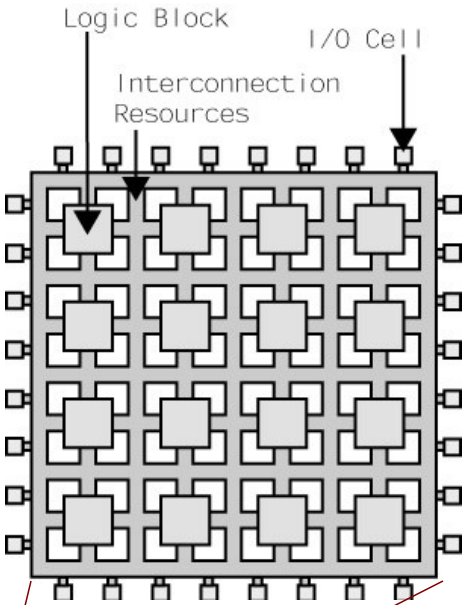


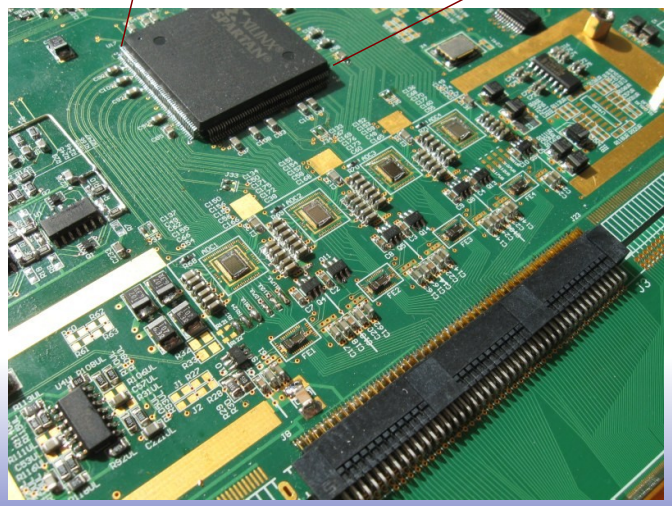
Moore law works well...

HEP: 0.8um, 0.35um, LHC-0.25um, FAIR-0.18um?, S-LHC-0.13um?, 65nm?

Additional advantage – thinner oxide – less trapping – better radiation hardness!

FPGA – Field Programmable Gate Array for complex readout systems

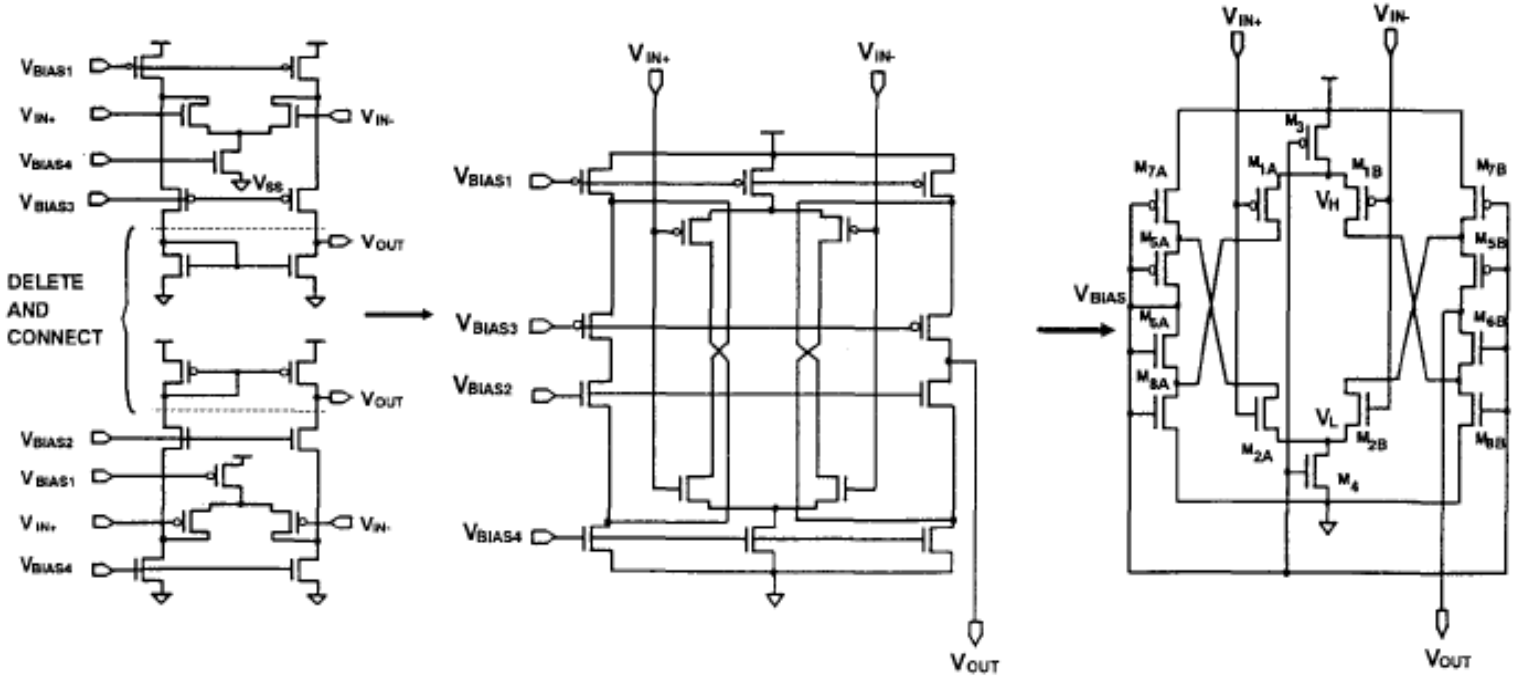




- Advantages
  - Rapid development
  - Huge possibilities (billions of gates)
  - Low cost
  - Abundance of configurable resources
  - Smallest CMOS processes – low power
- HEP applications
  - Proof of concept for digital designs
  - ASIC testing & verification (e.g. ADC parametrization)
  - Data AcQuisition (DAQ) and Trigger processing units
  - New applications coming (e.g. TDC)...

LVDS receiver

Direct implementation of self-biased differential amplifier



M. Bazes, Two Novel Fully Complementary Self-Biased CMOS Differential Amplifiers, IEEE J. Solid-State Circuits, vol. 26, no. 2, pp. 165–168, February 1991.

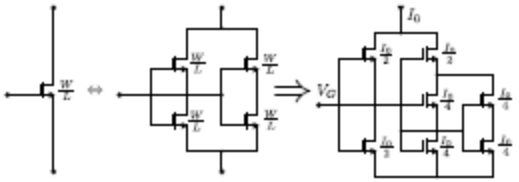
Readout peripherals
L-2L DAC

Architecture

An architecture based on MOS implementation of R–2R ladder (L–2L)
Main benefits:

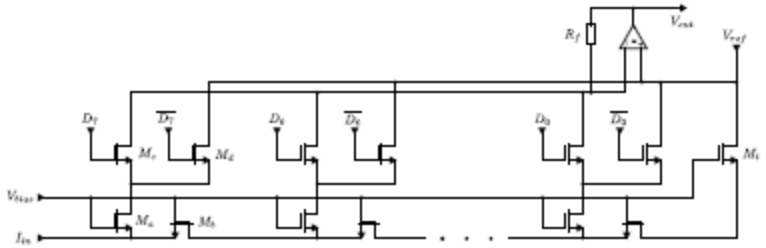
- Small number of elements (4N+1)
- Simple layout

Principle of operation



Current flowing into series–parallel identically designed transistors is equally divided between them[1]

Implementation



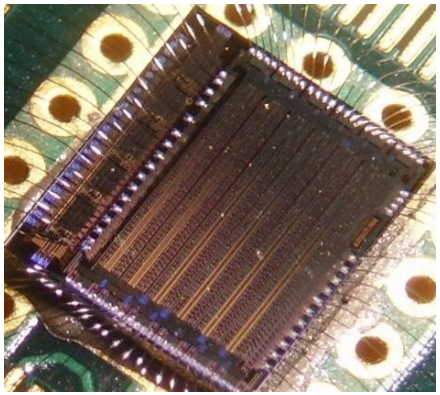
Design assmptions

- Static DAC with 8 bit resolution.
- Low power consumption $< 100\ \mu W$
- Small core size $< 0.05\ mm^2$
- Application – fine voltages trimming in multichannel readout systems

D.Przyborowski, M.Idzik, "Development of low-power small-area L-2L CMOS DACs for multichannel readout systems", JINST 7 C01026 2012

ASIC design flow

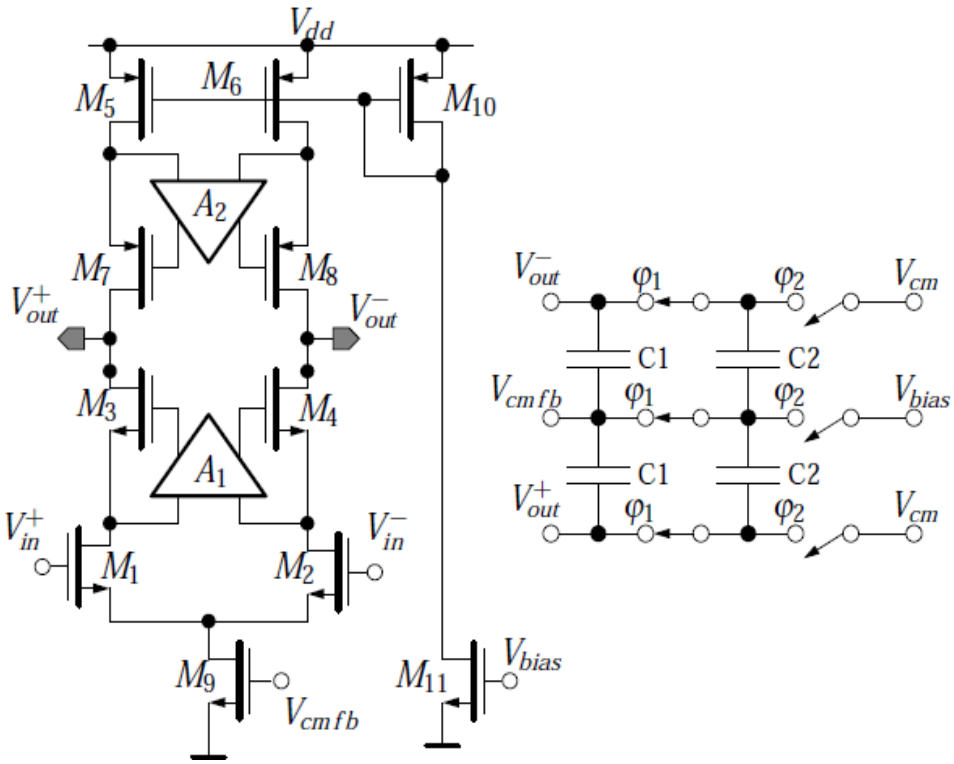
- Schematic and simulations
  - Preamplifier, Shaper, I/O, etc...
  - Standard DC, AC, TRAN simulations, MC(!) and Worst Case simulations
- Layout
  - Drawn manually (or Layout XL guided)
  - Digital part synthesized automatically with SoC Encounter



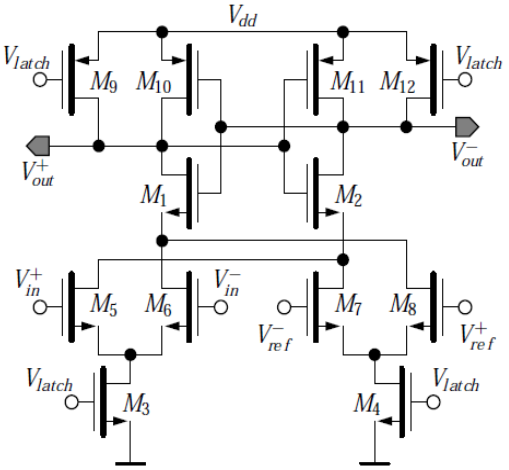
- Verifications
  - DRC – checking design rules
  - LVS (layout vs schematic) -comparing layout with original design
  - QRC – parasitic extraction (for post-layout simulations)
- Post-layout simulations and design-layout iterations !
- Generating the GDS2 file for submission

Pipeline ADC – key blocks

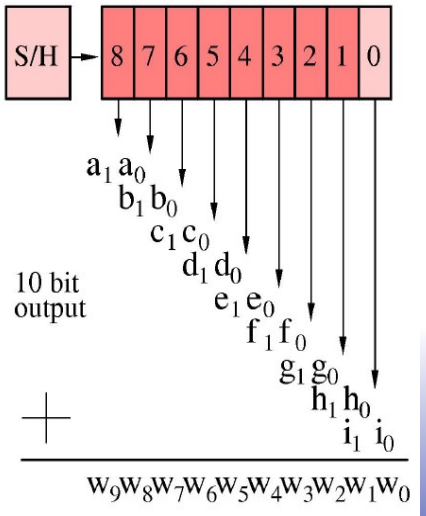
- Fully differential amplifier+CMFB



- Dynamic latch comparator



- Digital correction



- Denote stage output as $s_i = \{0, 1, 2\}$
- Then digital correction is

$$w = \sum_{i=0}^{8} 2^i s_i$$

A lot of consumed power goes to amplifiers and clock distribution