From Fundamental Detector Research to Industrial Embedded Power Device Technology Development

Joint Instrumentation Seminar
DESY, Hamburg University and XFEL

Colloquium in honor of Prof. Gunnar Lindström's 80th birthday

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Abstract

- Following the "More than Moore" paradigm, restructuring of parts of the semiconductor industry is currently taking place: Added value generation is being sought in the chip-level integration of devices offering unique functionality with dense CMOS logic, as opposed to the former shrink approach towards ever smaller structure sizes (Moore's Law).
- An example is presented in the area of embedded power devices that are capable of handling voltages up to several times 10 Volts in a 1.5 Volt core voltage analog/mixed-signal logic platform. Key aspects to be considered in the technology development are device performance factors like specific on-resistance, robustness (e.g. safe operating area and electrostatic discharge), reliability, latch-up, and substrate noise effects. Results from TCAD process and device simulation, device characterization, and statistical data analysis are presented.
- The speaker gives account of the knowledge and qualifications acquired during his diploma and PhD time in Prof. Gunnar Lindström's group on "Detector Research & Development" (formerly "Gruppe Nukleare Meßtechnik") whenever useful reference to his current field of work can be made. An industry perspective is thus provided on the value of fundamental research and the qualifications required for a successful career in the semiconductor industry.

Contents

- Infineon: The Company
- Embedded-Power Device Development at Infineon Dresden
- Anecdotal References to “Good Old Times” at Nukleare Meßtechnik

Infineon at a Glance

The Company

- Infineon provides semiconductor and system solutions, focusing on three central needs of our modern society: Energy Efficiency, Mobility and Security
- Revenue in FY 2010*: 3.295 billion EUR
- 25,119 employees worldwide (as of April 2011)
- Strong technology portfolio with about 15,400 patents and patent applications (as of Feb. 2011)
- More than 20 R&D locations
- Germany's largest semiconductor company

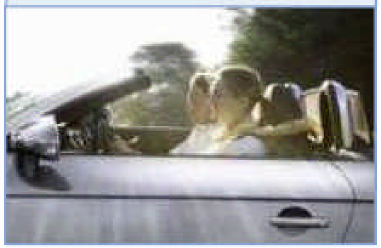
*Note: Figures according to IFRS with Wireline and Wireless as discontinued operations; as of September 30, 2010

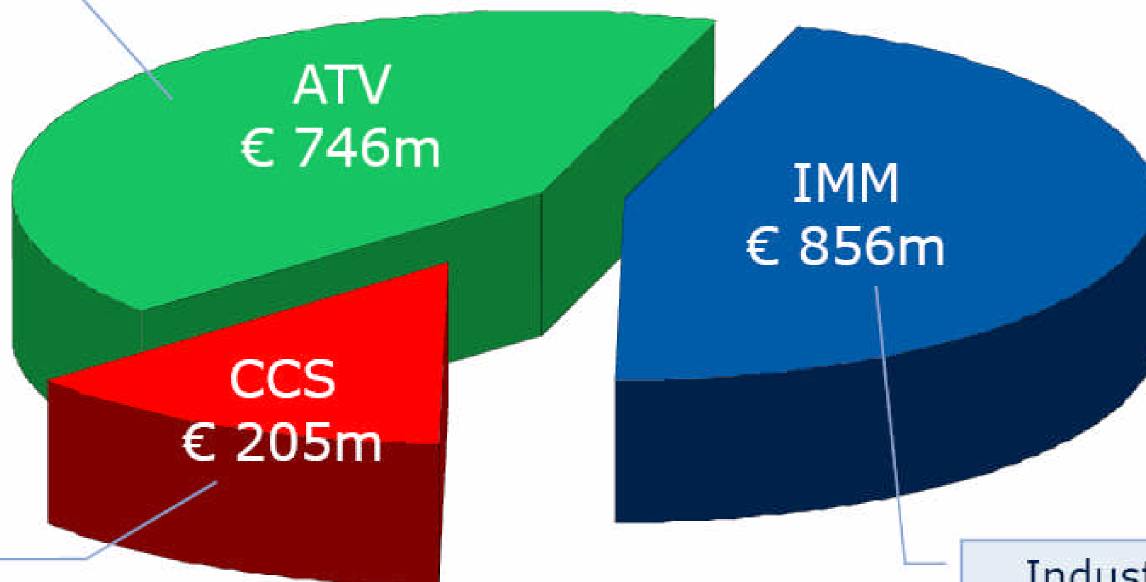
Source: Infineon company presentation May 3rd, 2011, www.infineon.com

Revenue Split by Division

6-months FY 2011 revenue split

Automotive





Chip Card & Security

Industrial & Multimarket

Source: Infineon company presentation May 3rd, 2011, www.infineon.com

Infineon Semiconductor Technology Portfolio

Infineon

Technology portfolio fits needs of logic and power applications

Power/Analog

incl. Green Robust

Analog Bipolar: DOPL, Ax, BIPEP, B4C
Analog BICMOS: B6CA, B6CA-CT, B7CA, SPT170
500 - 350nm HV-CMOS-SOI
Smart Power : 1200-130nm BIP/CMOS/DMOS
SPTx (Automotive, EDP) (BCD)
Smart : (SmartMOS) CMOS/DMOS, SMARTx, MSMARTx, SSMARTx Opto-TRIAC

DMOS: Low Voltage Trench Mosfets (OptiMOS)
HV-DMOS: Superjunction MosFET (CoolMOS)
IGBT: Trench IGBT 600-6500V, rev. cond., fast recov. diodes
SiC: Diode; MOS/JFET

all of them adopted for automotive and industrial requirements

MEMS/Sensors

Analog ICs: B6CA, B7CA
Coreless Transformer
Magnetic: BxCAS, C9FLRN_GMR
Opto: OP-DI, OP-TR, OP-C9N, µ-modules

Pressure: BxCSP, TIREPx
Silicon-Microphones

CMOS

Digital CMOS: 800nm – 65nmTechnology Nodes (Platform <180nm incl. RF, AMS)
Analog/Mixed Signal: 500nm – 180nm Technology Nodes (CxNA)
eNVM: EEPROM: IMEMR, C9FL, OTP: C5OP (Automotive)
eFlash/EEPROM: 250nm – 65nm CxFL (Chip Card), CxFLA, CxFLN (Automotive)
HV-CMOS: 130nm, C11HV

RF/Bipolar

RF BICMOS: 25GHz – 100GHz: B6HFC, B9COPT, B10C
Bipolar IC: 2GHz...200GHz RF-Bipolar: BxHF
HiPAC: Al/Cu Integrated Passives
P7Mxx, P7Dxx, P8Mxx, P9Mxx

SiGe: B7HFM, B7HF_SLC, B7HF200
RF Switches: C7NP, C11NP

Bipolar/Discretes/MMIC:
RF-Transistors NF-TR; BxHF(D/M),
Power Amplifier: LDMOS, LDxM, LDxIC, LD9AB
Diodes: NF-DI, Tuner: DxT, Schottky: DxS

SiGe: B7HFD/M, B7HF_SD
RFMOS: HFM
PIN: DxP

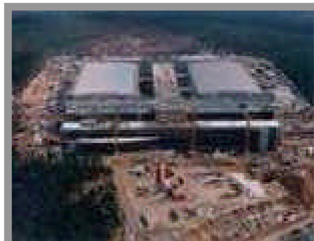
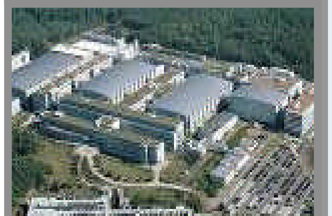
Source: Infineon company presentation May 3rd, 2011, www.infineon.com

Infineon – Worldwide Production Sites Frontend and Backend

Frontend Backend

Source: Infineon company presentation May 3rd, 2011, www.infineon.com

Infineon Technologies Dresden (IFD)


12/93 Siemens AG decided to build a first-class semiconductor fab in Dresden

10/95 Production start 200mm fab

02/98 Joint Venture with Motorola for first 300mm pilot-line worldwide

04/99 Carve-out of Semiconductor division from Siemens
=> Foundation of Infineon AG:
Siemens Microelectronics Center Dresden becomes Infineon Technologies Dresden

05/00 Laying of the cornerstone for first 300mm fab worldwide

05/05 Opening of Infineon Research and Development Center (RDC)
Opening of Center Nanoelectronic Technologies (CNT),
Public Private Partnership (PPP) between FraunhoferGesellschaft, AMD and Infineon

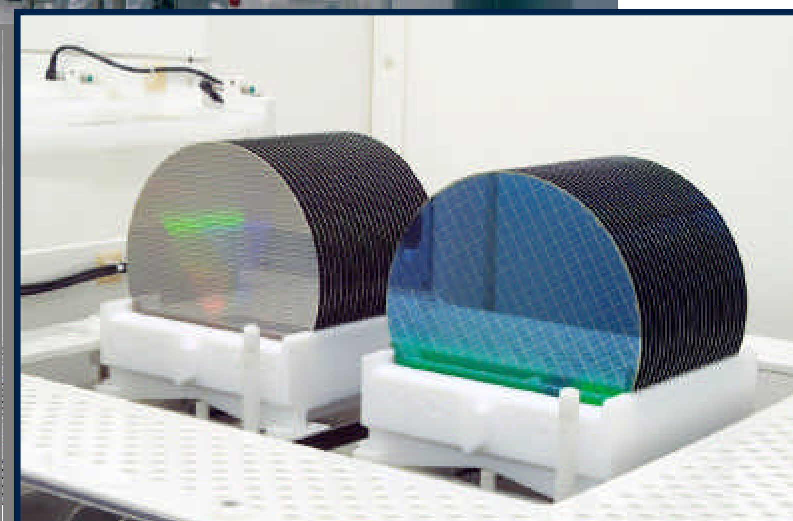
05/06 Infineon carved-out its Memory Products Business
=> Foundation of Qimonda

03/08 Infineon Dresden becomes an entire Logic site

Source: Infineon Dresden site presentation 2010

Front-End Production at Infineon Dresden

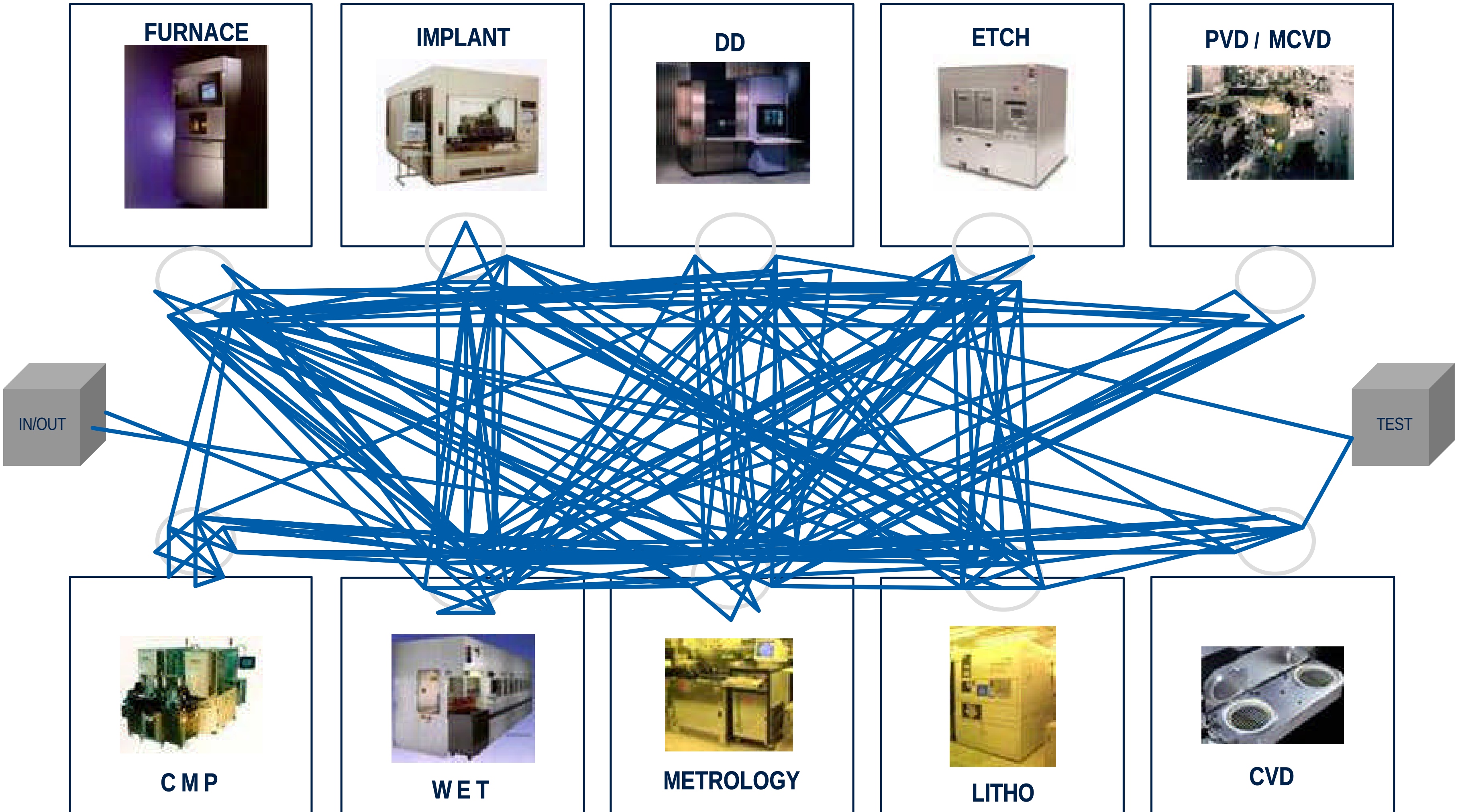
- State-of-the-art semiconductor processing line for large-scale integration of electronic circuits on 200 mm silicon wafers
- 0.25 µm to 90 nm technology nodes
- Aluminum and copper metallization
- Research and development site



Picture source: www.infineon.com media for journalists

Production Complexity

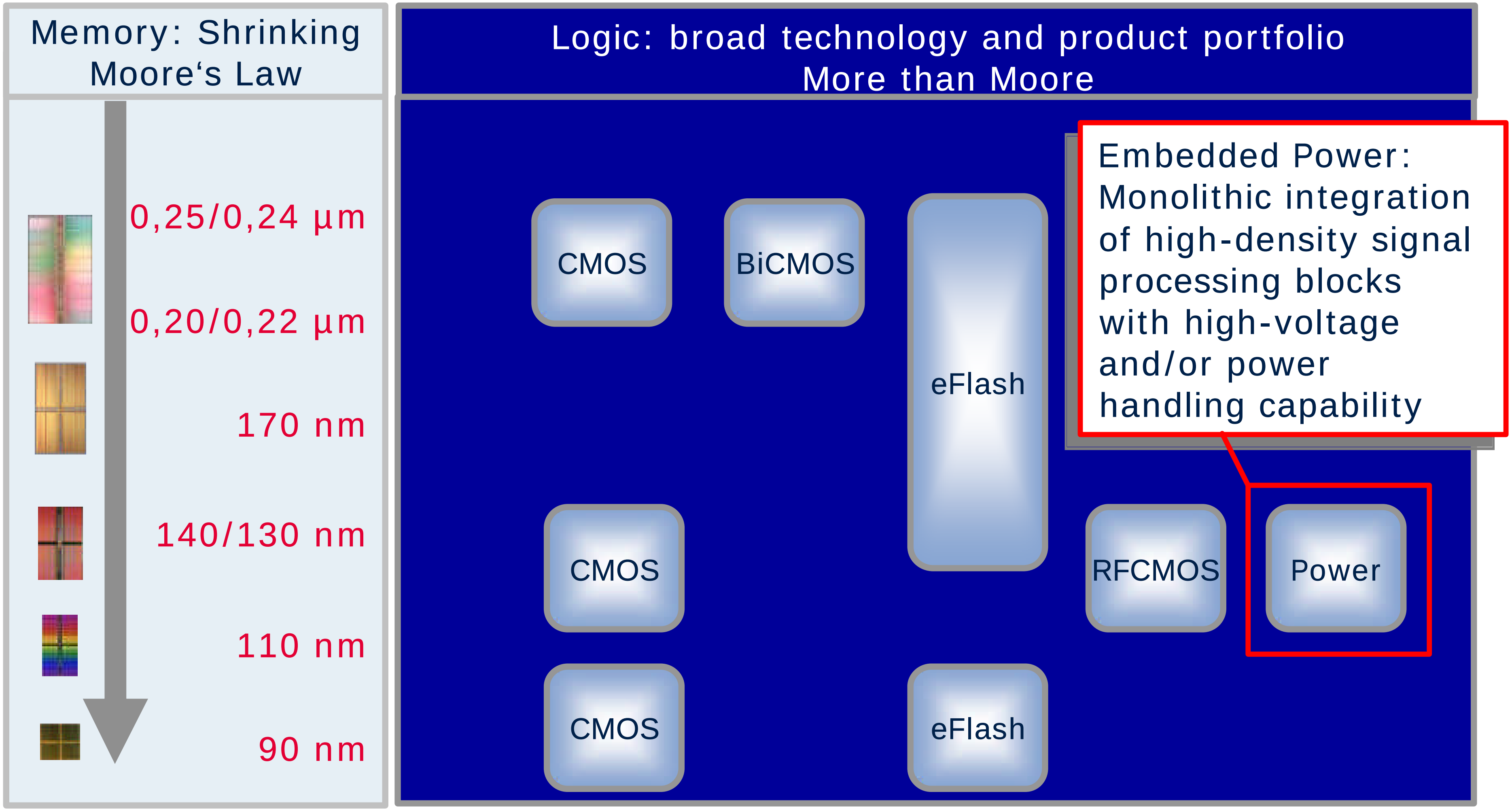
Several hundred process steps for each wafer



Example: Pilot-Line featuring all necessary tools and processes for a product cycle

Source: Infineon Dresden site presentation 2010

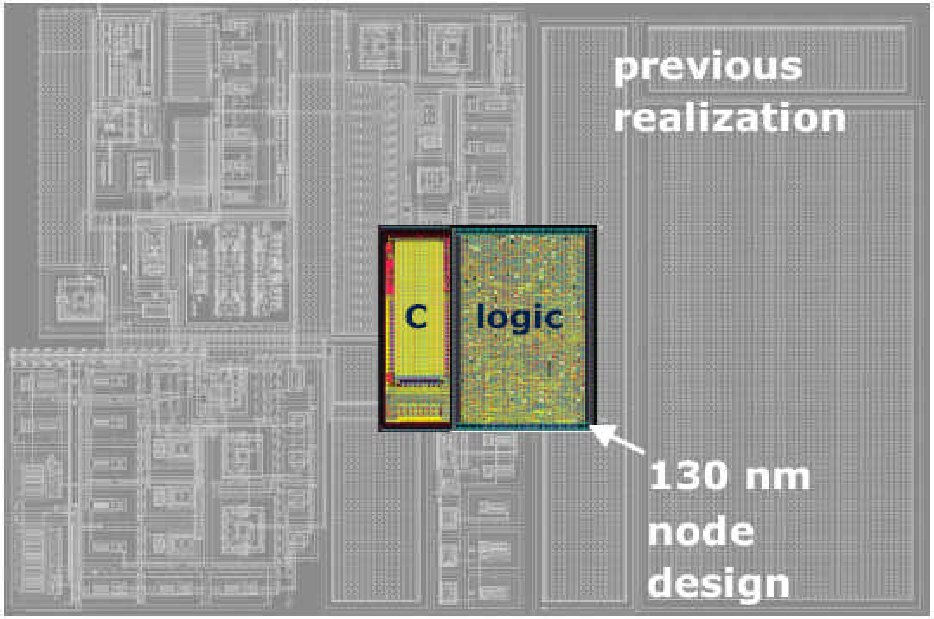
„More than Moore“



Source: Infineon Dresden site presentation 2010

Value Proposition for Embedded Power @ IFD a): Gate Density

- Address the industry trend towards higher on-chip functionality as a key differentiator in the IC market
- Re-use of intellectual-property (IP) blocks for reduced time-to-market
- Area shrink (e.g. by realizing analog functions in the digital domain)

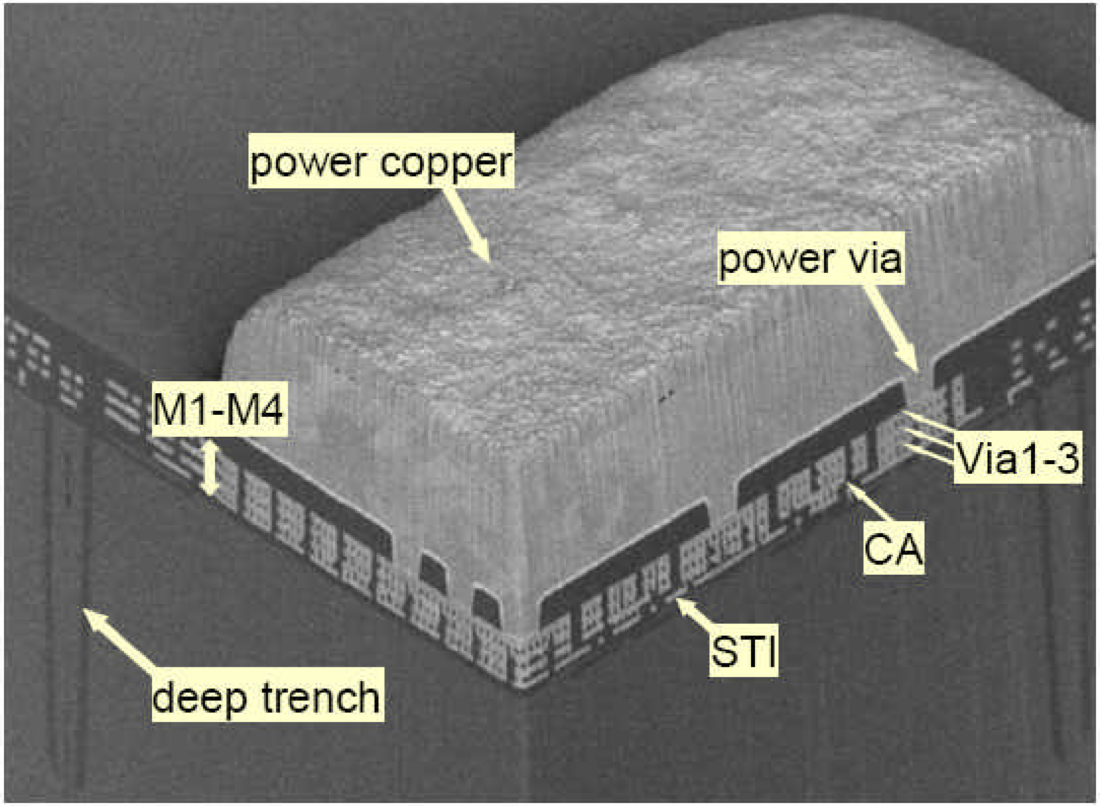


Digital switched-capacitor based replacement of an analog control circuit

Ralf Rudolf et al., „Automotive 130 nm Smart-Power-Technology including embedded Flash Functionality“, proceedings of the ISPSD2011

Value Proposition for Embedded Power @ IFD b): Deep-Submicron Process Line

- Feature size, process tolerances
- Yield stability / defect density control
- All-copper metalization for optimum thermal management

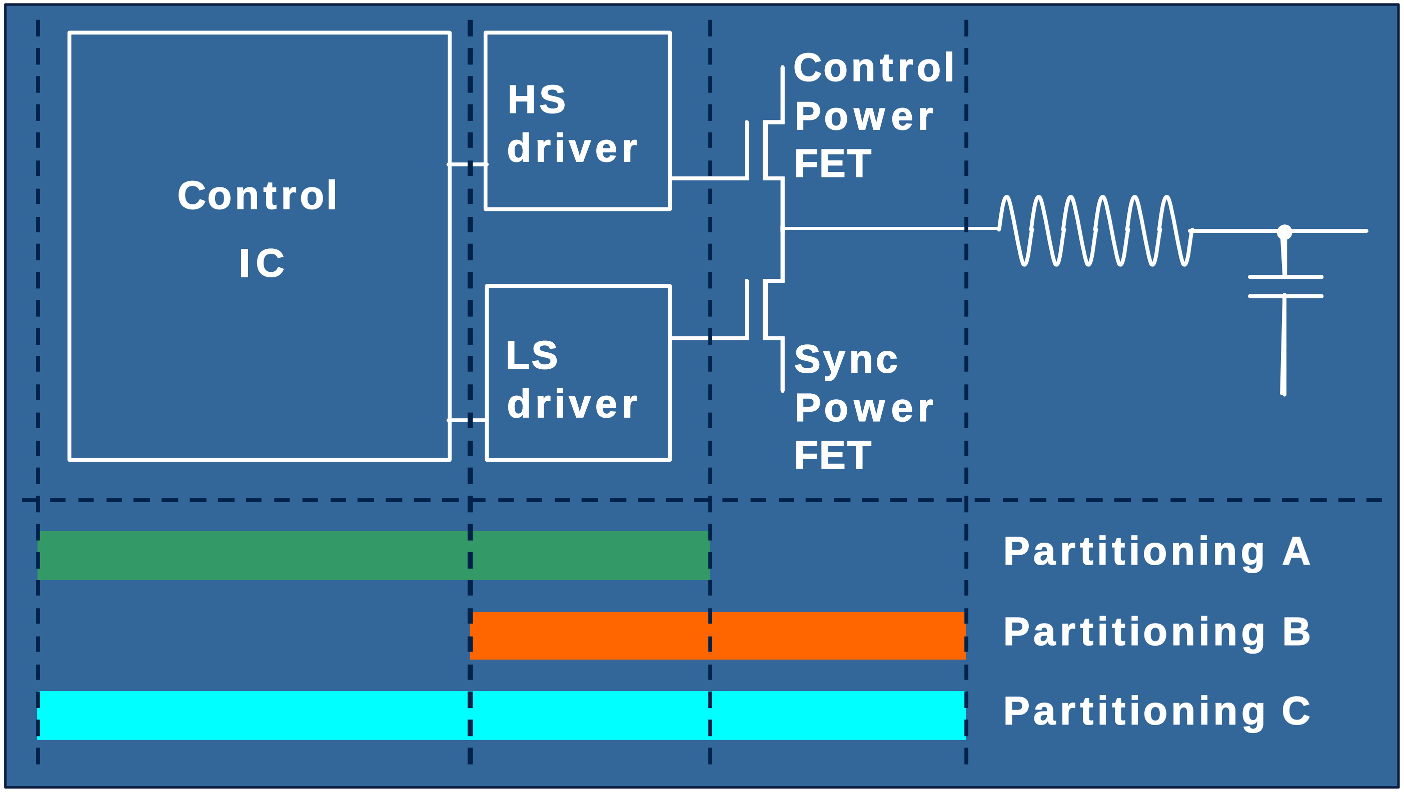


BEOL stack cross section

Ralf Rudolf et al., „Automotive 130 nm Smart-Power-Technology including embedded Flash Functionality", proceedings of the ISPSD2011

Fields of Application for Embedded-Power Technologies

Example: Regulated-voltage generation using
buck converter and/or synchronous rectification (SR)



Depending on cost factors, performance factors, and target market requirements, the choice of the appropriate system partitioning decides on the competitiveness of the product.

IFD Research and Development Activities for Embedded-Power Technologies

- TCAD (Technology Computer Aided Design)
  - detailed representation of the IFD process flows with in-depth unit-process background information
  - delivering reliable pre-silicon electrical device characteristics
- Highly automated testchip layout and characterization
- Shared reticle program, dual/quad multi-level reticle mask options
- Efficient unit process development
- Competitive flow-factor for development lots
- Various lab characterization capabilities including high-power SMUs and TLP/SOA set-up

Process Blocks and Features of C11HV

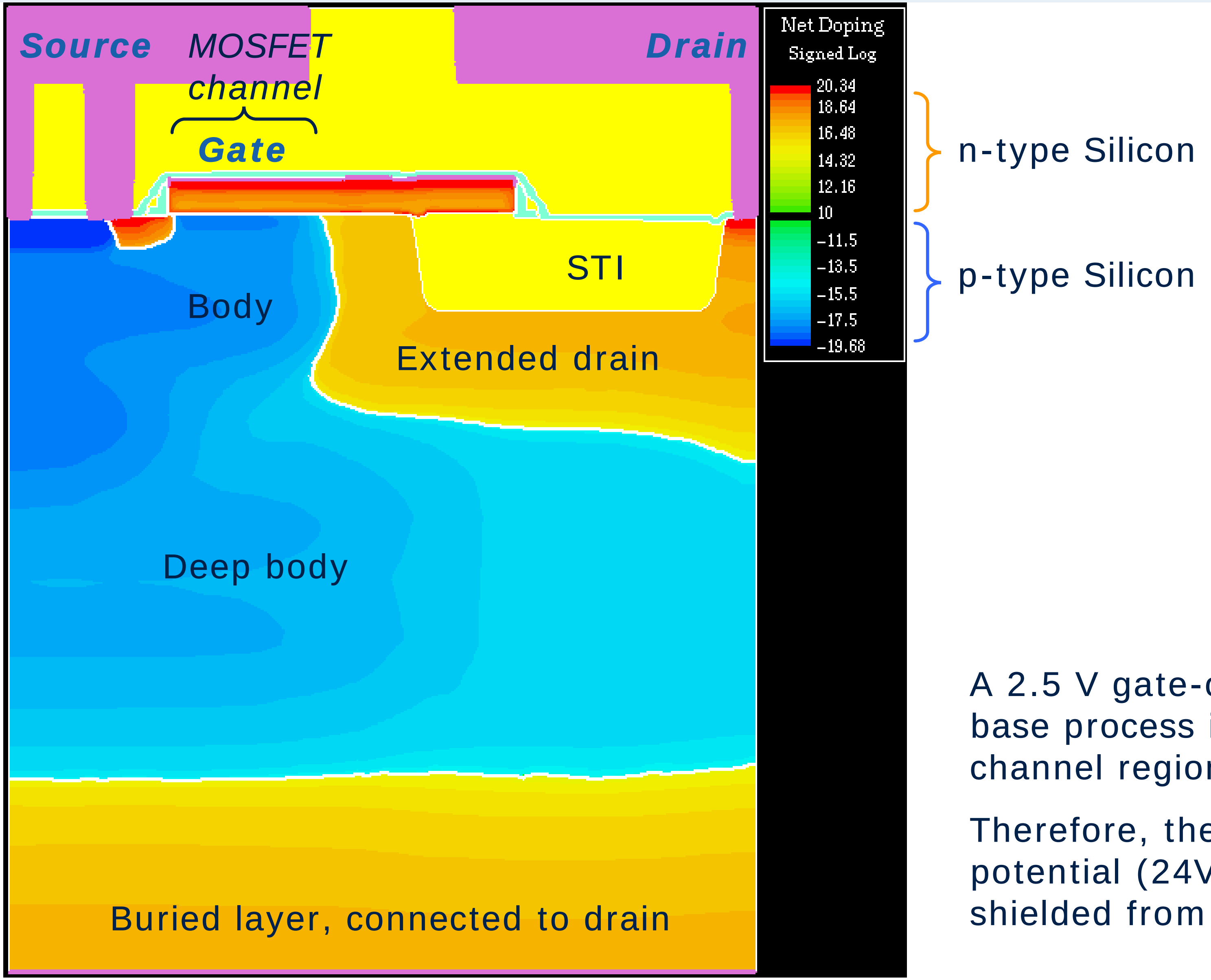
C11HV process module
p-type substrate
shallow trench isolation
HV isolation
HV devices
logic wells
gate stack (oxide and poly)
extension/halo implants
spacer
source/drain implants
silicide formation
4 levels Cu metallization
top metal and passivation

Overview High Voltage Devices

- 12V HVNMOS/PMOS Power Transistors for High-Current Applications, Rdson 4 mOhm*mm^2
- 24V HVNMOS/PMOS Power Transistors for Gate Driver Applications
- 24V HVNMOS/PMOS w separate Body for analog and level shifter applications. HVNMOS fully isolated
- 20V pnp Transistor
- HV ESD concept based on self protecting power devices, Diodes and active clamps
- passive Elements (Poly Resistors and Metal Capacitors)
- Well Isolation for floating Low Voltage circuitry

Determining the recipes for the newly introduced process modules is the main deliverable of the technology development group!

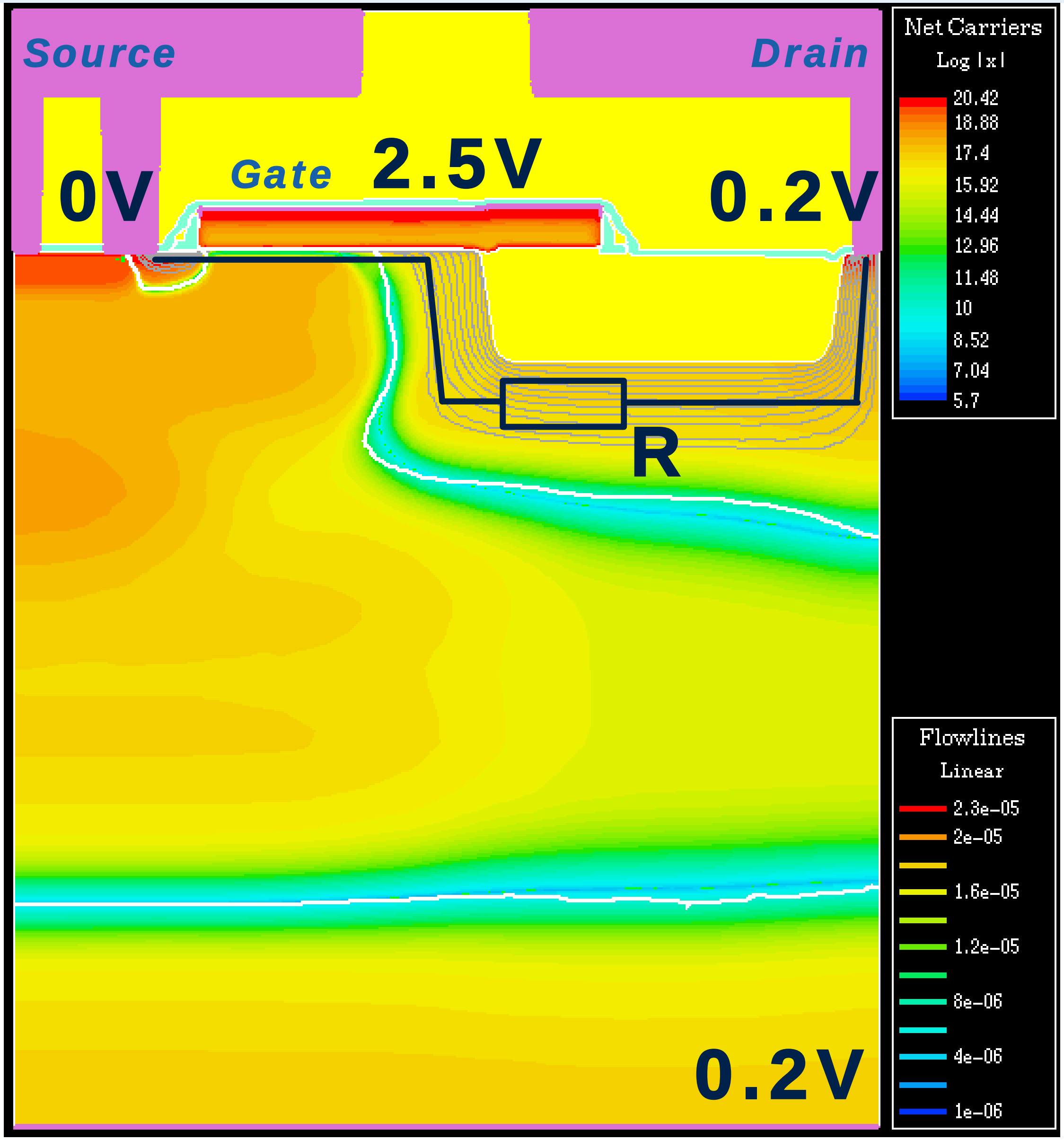
Lateral High-Voltage (HV) Device Concepts
24V Drain-Extended MOSFET



A 2.5 V gate-oxide from the base process is used for the channel region (5.2 nm).

Therefore, the high drain potential (24V) must be well shielded from the gate!

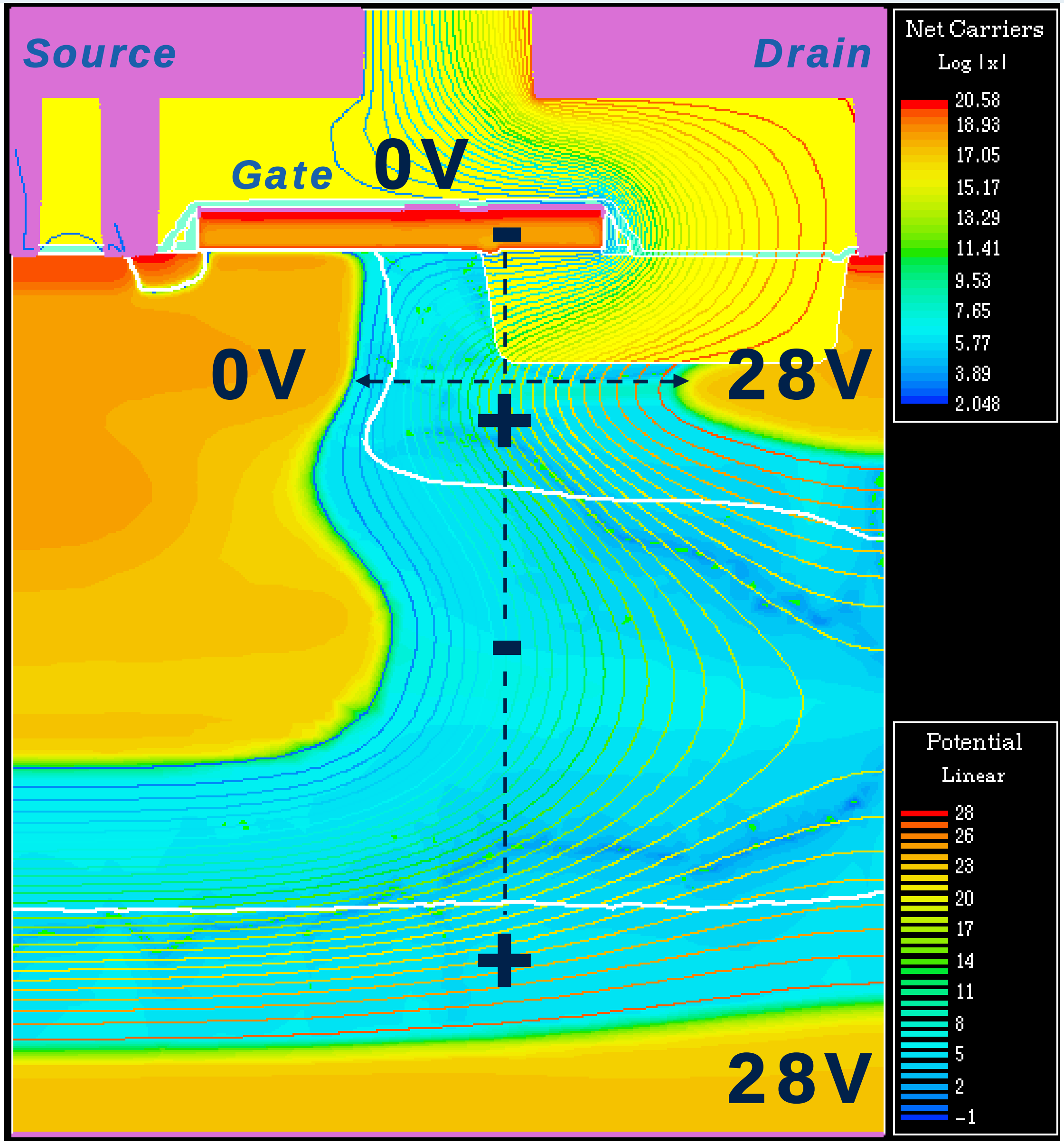
Basic HV Device Operating Conditions On-State



The on-state resistance is determined by the doping in the drain extension.

-> minimizing the on-state switching resistance requires maximum doping in the drain extension.

Basic HV Device Operating Conditions Off-State



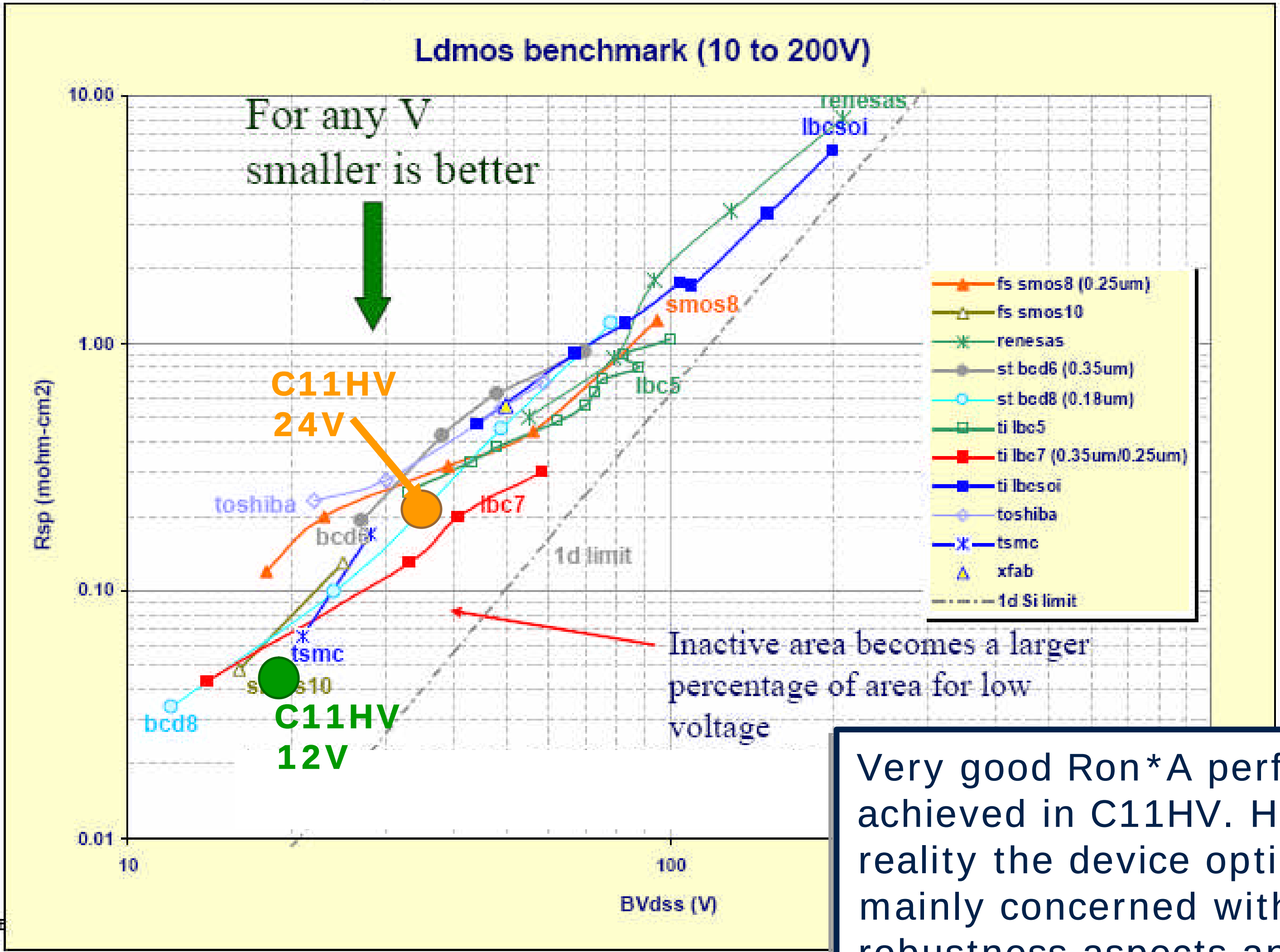
However, high doping in the drain extension limits the breakdown voltage!

Mirror space-charge principles are used to reduce the electric field strength in the drain extension region.

If charge matching is optimized the horizontal drain / body region mimics a p-i-n diode, allowing minimum lateral extent of the structure.

Drain-Extended MOSFET On-Resistance Benchmark

Integrated LDMOS Performance

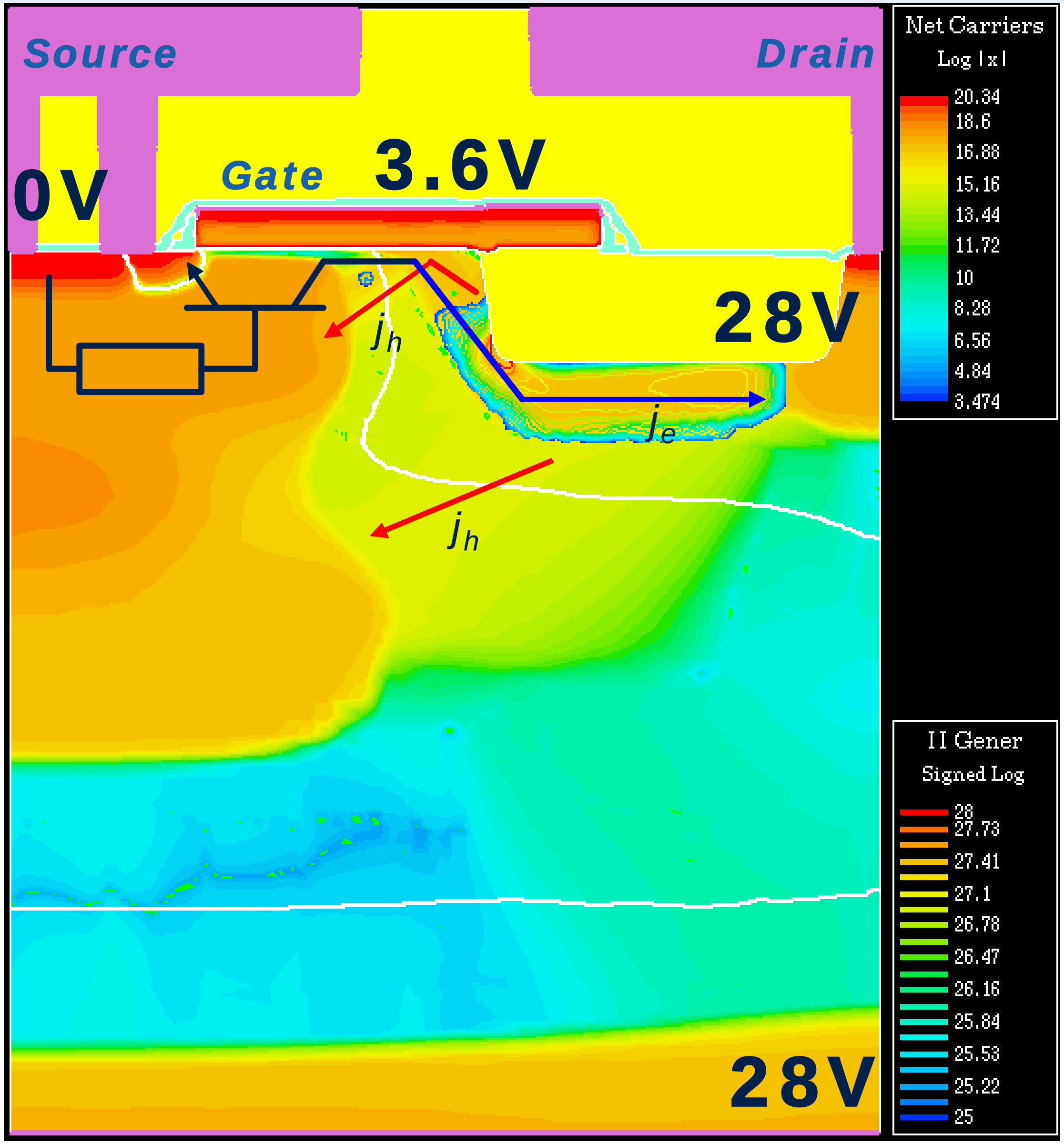


Source: T.R Efland „Trends in Power Devices“, presented at Dongbu Tech Day 10 2009

Very good Ron*A performance is achieved in C11HV. However, in reality the device optimization is mainly concerned with device robustness aspects and/or safe-operating area (SOA).

Basic HV Device Operating Conditions
Hot-switching State

$V_{ds} * I_{ds} \approx kW/mm^2$

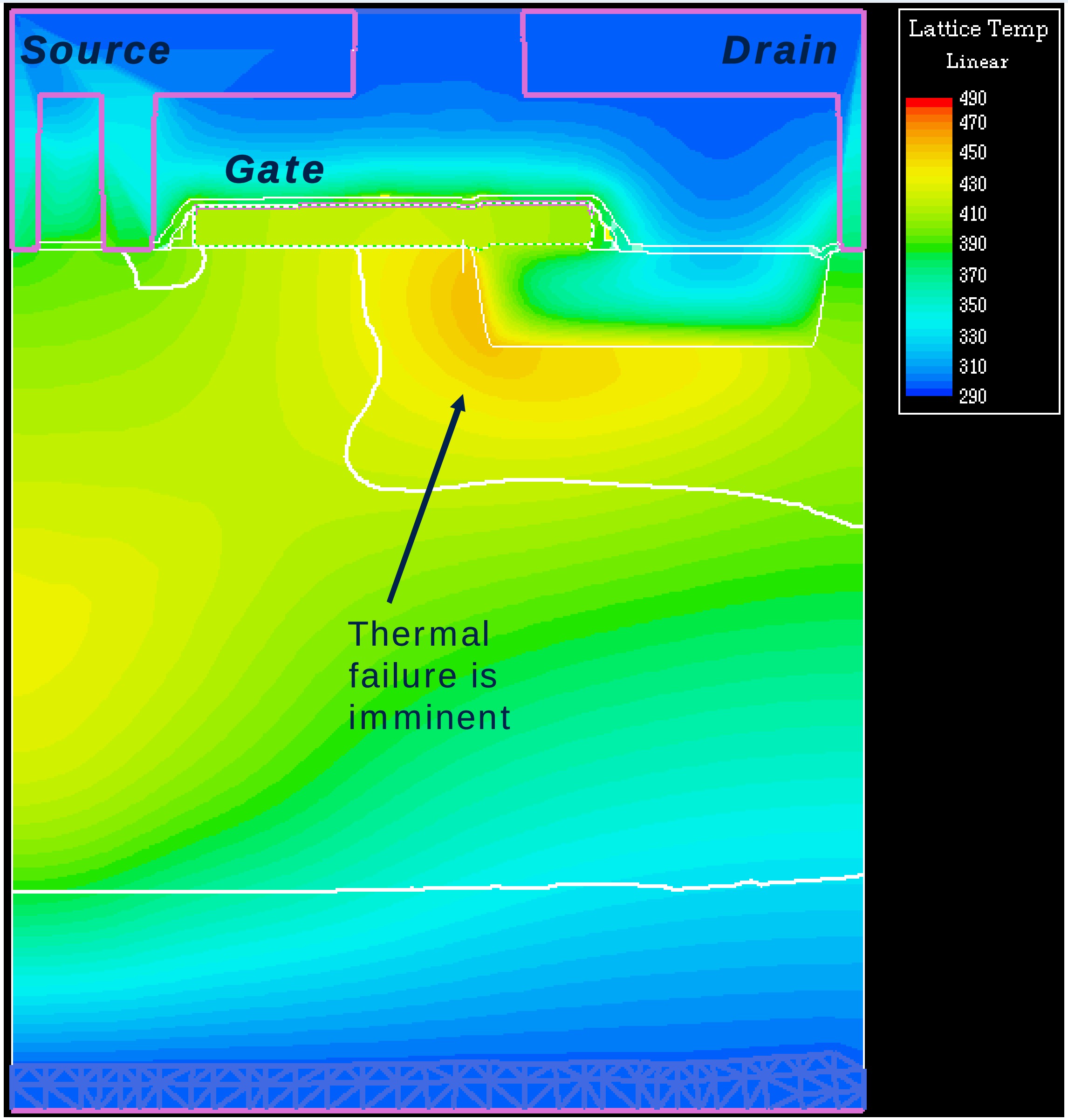


This switching state should be kept as short as possible since a lot of power is dissipated
-> poor energy efficiency
-> thermal failure

High electric fields in the drift region lead to impact-ionization (II) carrier multiplication
-> hole currents are biasing the inherent npn
-> hot-carrier effects, device parameter drift / reliability

Safe operating areas (SOA) for V_{ds} and I_{ds} can be defined based on
-> thermal failure
-> electrical npn triggering
-> reliability

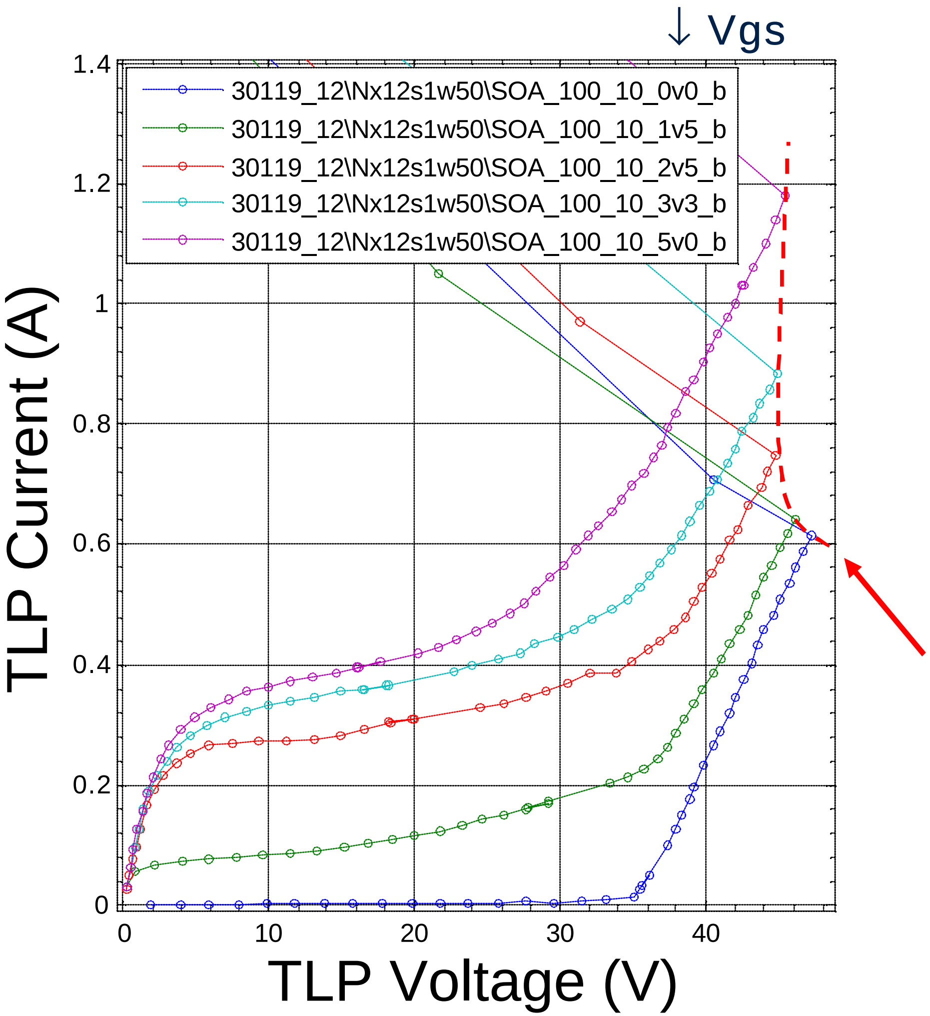
Lattice Temperature after 100 ns (Thermal SOA, medium switching times)



Electro-thermal TCAD simulations are quite helpful for optimizing the device robustness.

The metallization plays a vital role in heat conduction away from the active device region.

Transmission-Line Pulse Characterization (Electrical SOA, short switching times)



Transmission-line pulsing (TLP) is typically a 100-ns square-wave pulsed IV characterization. This is a good indication of device behavior under ESD stress.

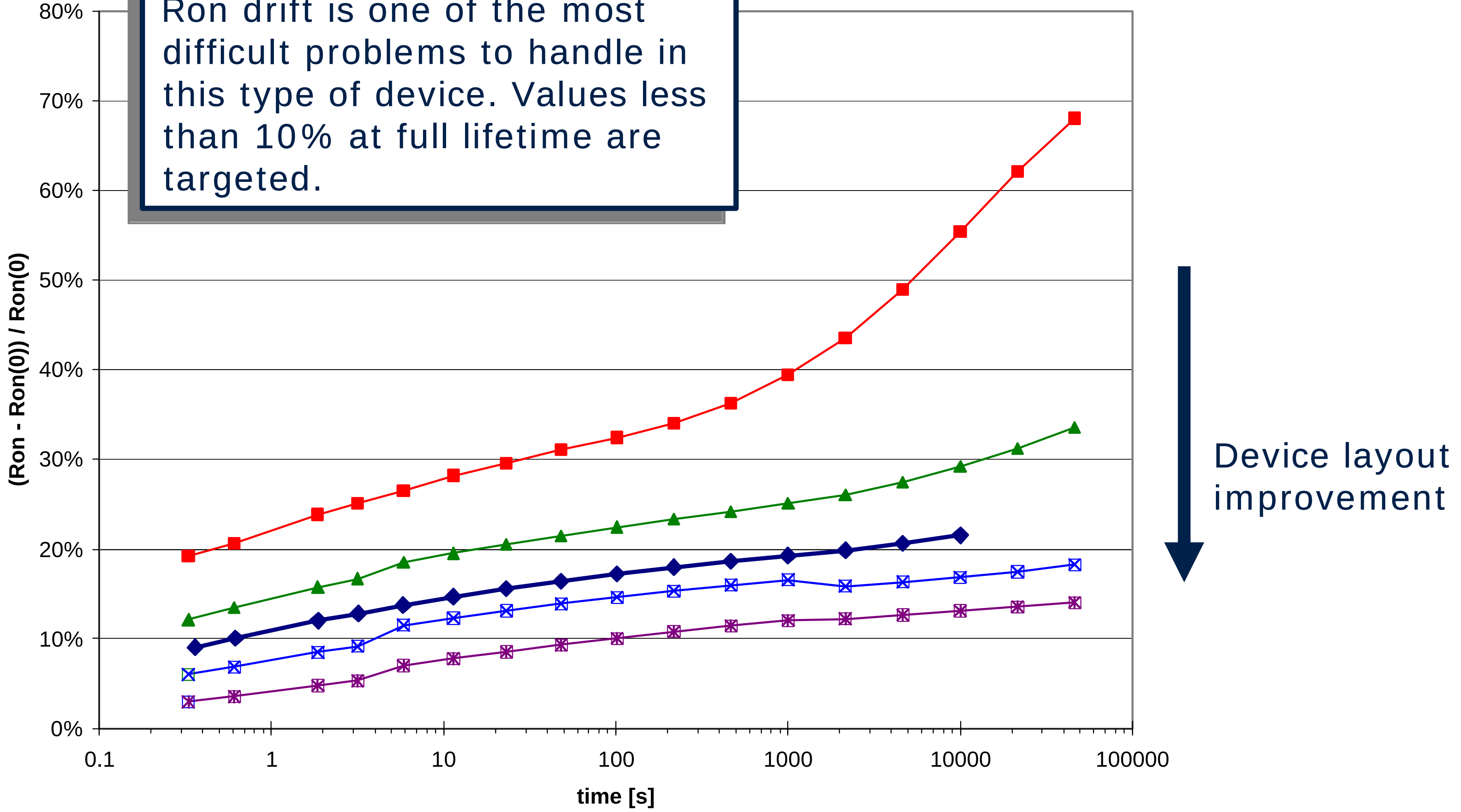
ESD qualification must be withstood at any pin of the IC (e.g. human-body model: 100 pF charged to 2 kV discharge through 1.5 kOhm).

The failure is due to electrical triggering of the parasitic npn.

Maximizing the failure current is an optimization target for output drivers.

Ron Drift
(Reliability SOA, life-integrated switch time)

Ron drift is one of the most difficult problems to handle in this type of device. Values less than 10% at full lifetime are targeted.

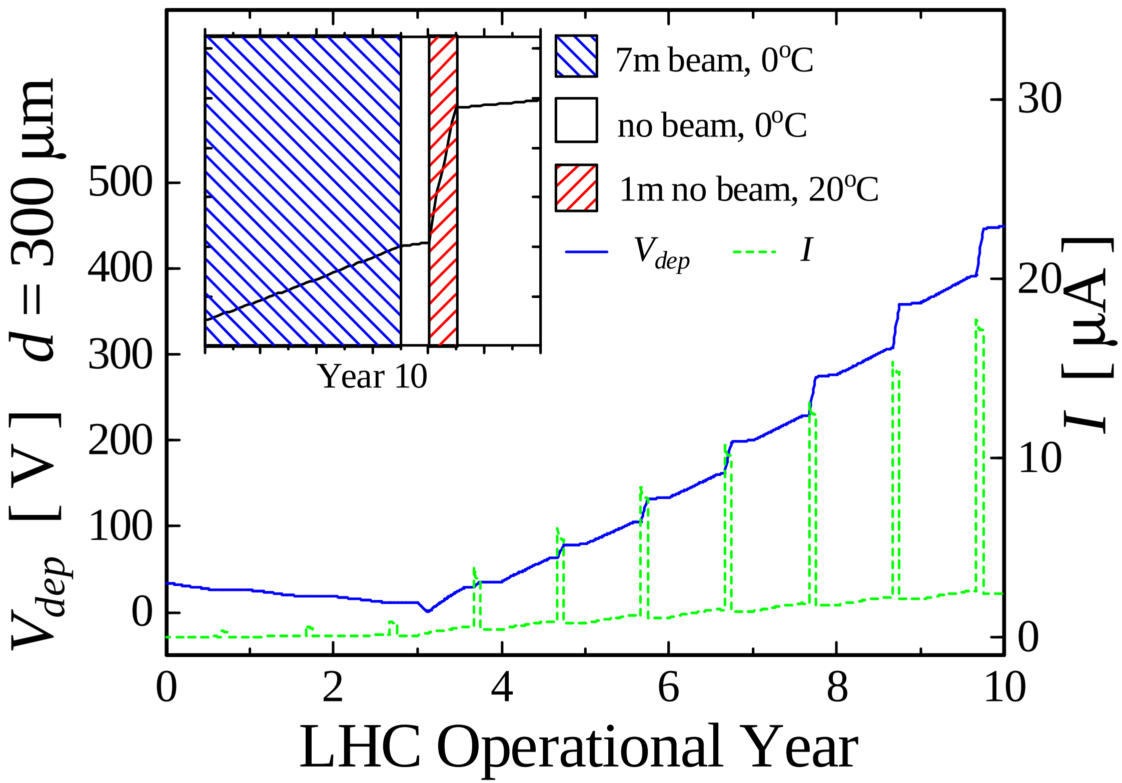


Lessons Learnt at “Nukleare Meßtechnik” Lifetime Projections, Customer Orientation

Infineon

Results for the Strip Layer at Radius 30 cm

F_{eq} = 1.7×10^{13} cm^{-2} per year at full luminosity.



Source: H. Feick, PhD thesis

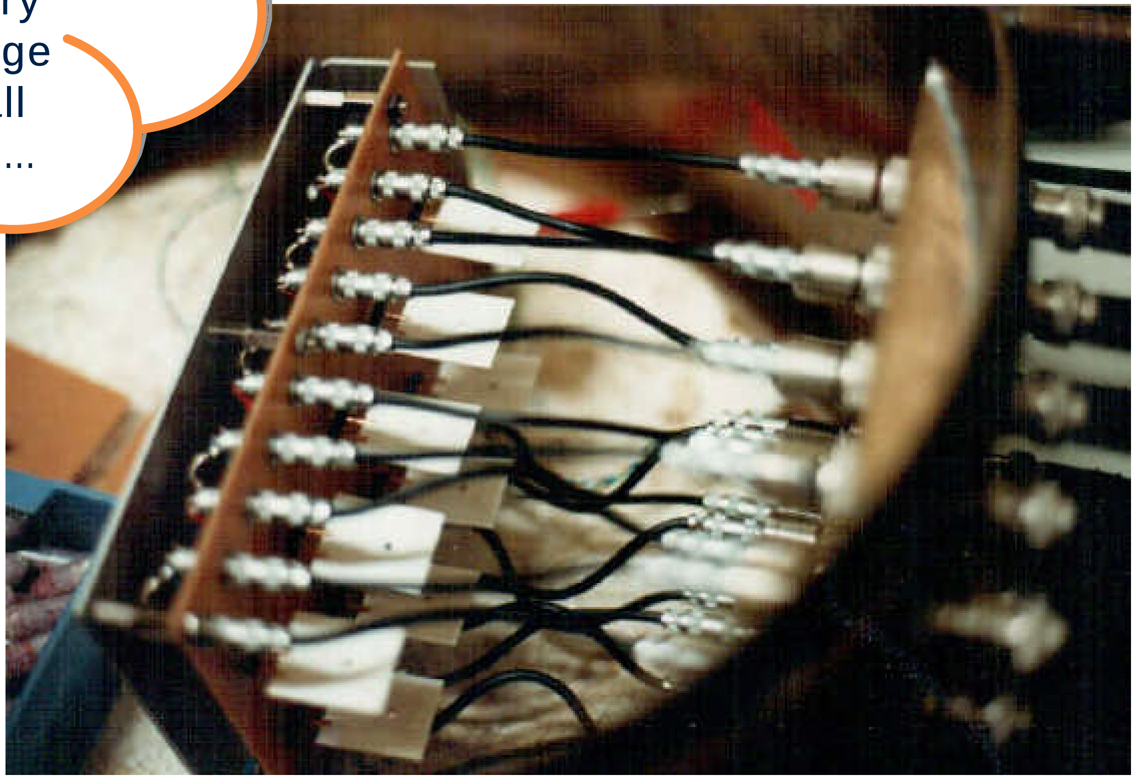
Our efforts to predict the operating lifetime of silicon detectors in the LHC experiments clearly addressed the customer’s need for a solid decision basis in planning the overall experiment.

Such type of customer orientation is also paramount for business success in the semiconductor industry.

Lessons Learnt from Gunnar: Part 1
Large Statistics Improve Prediction Quality

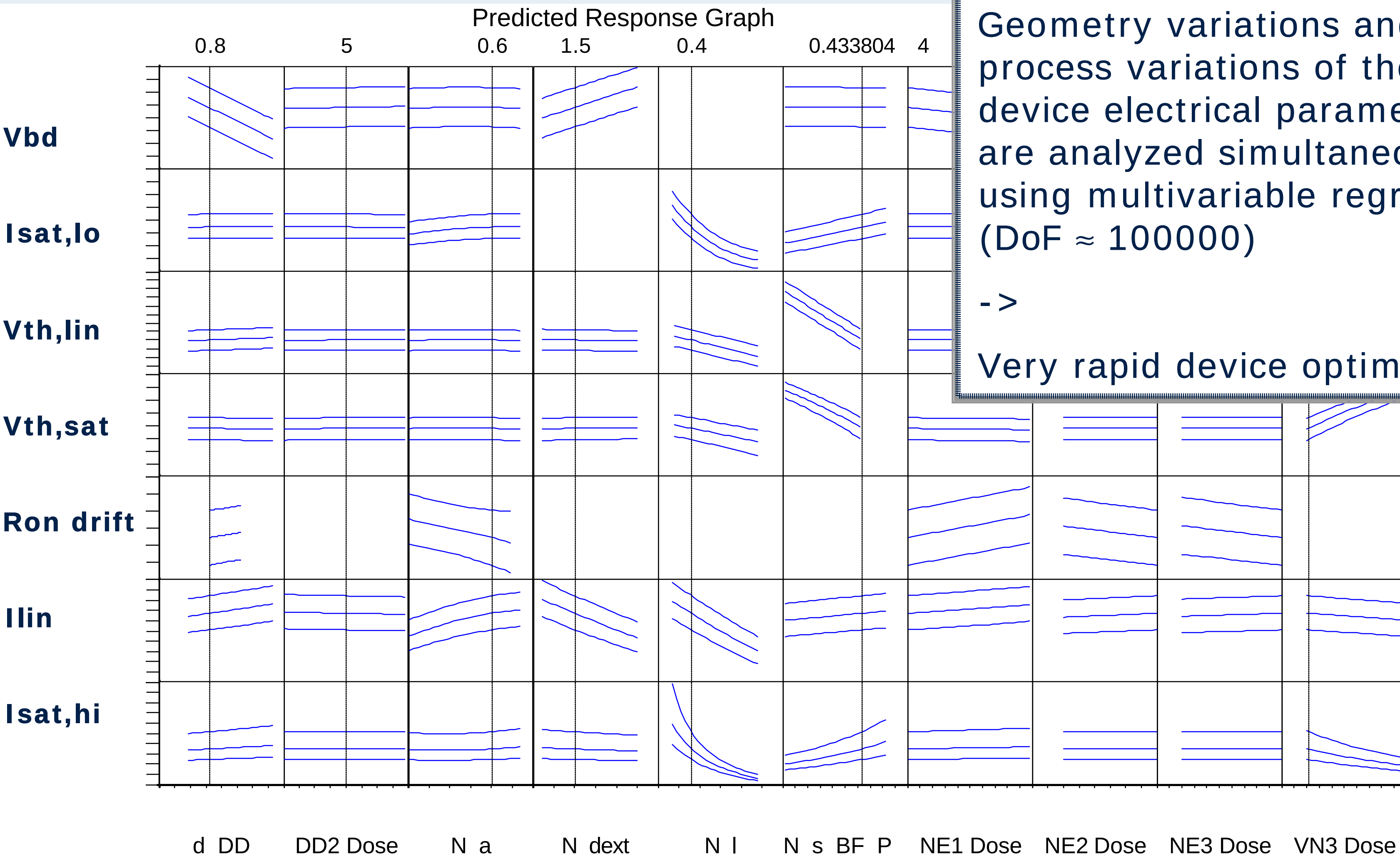
If only we had better statistics -

Those guys from industry must have incredibly large databases containing all the knowledge we seek...



This is how we tried to maximize our statistical database at „Nukleare Meßtechnik“ around 1997

Statistical Modeling and Optimization of the C11HV 24V Device



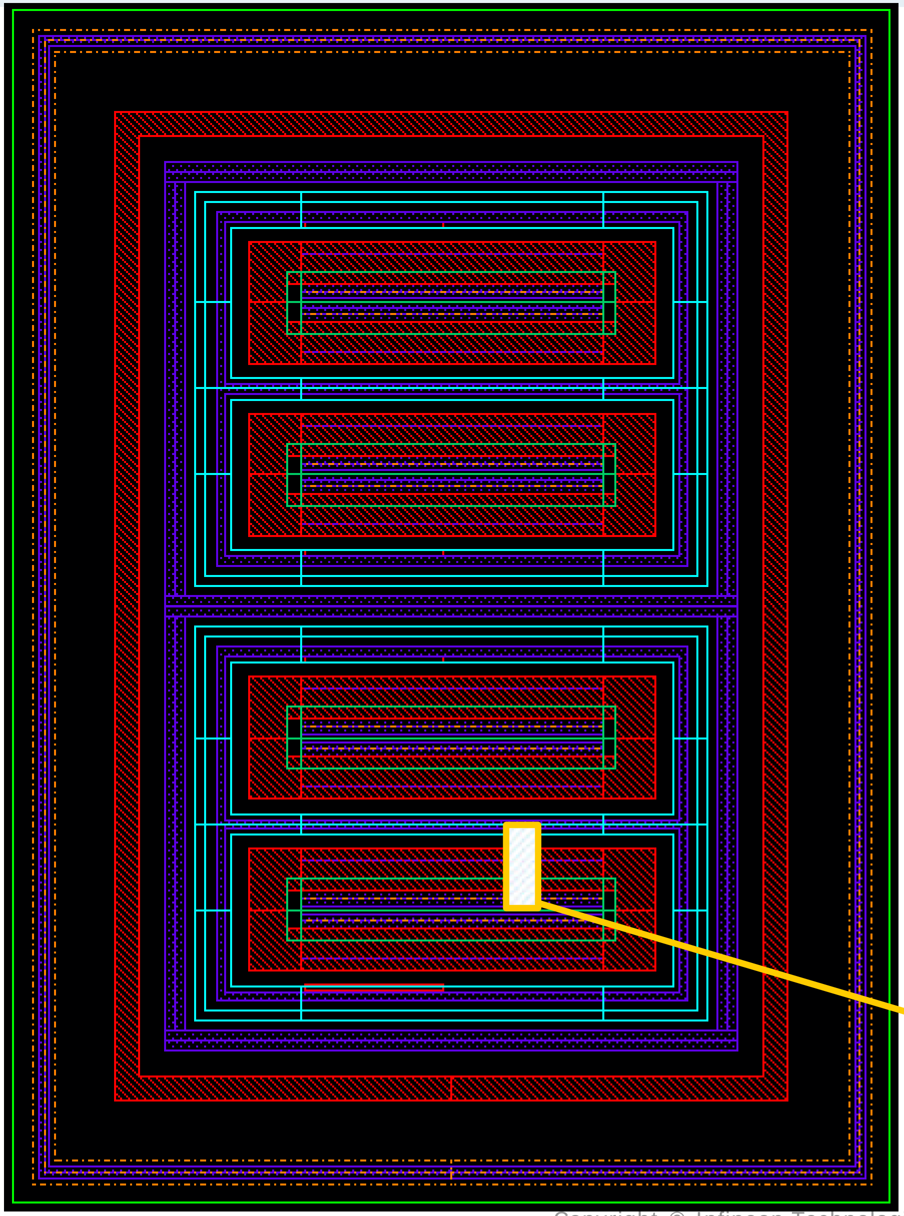
Geometry variations and process variations of the device electrical parameters are analyzed simultaneously using multivariable regression (DoF ≈ 100000)

->

Very rapid device optimization

It is true, we can generate and analyze tremendous amounts of data. Still, I am not aware of information in our databases explaining the mysterious type inversion and annealing effects in Silicon detectors.

C11HV Device Layout View

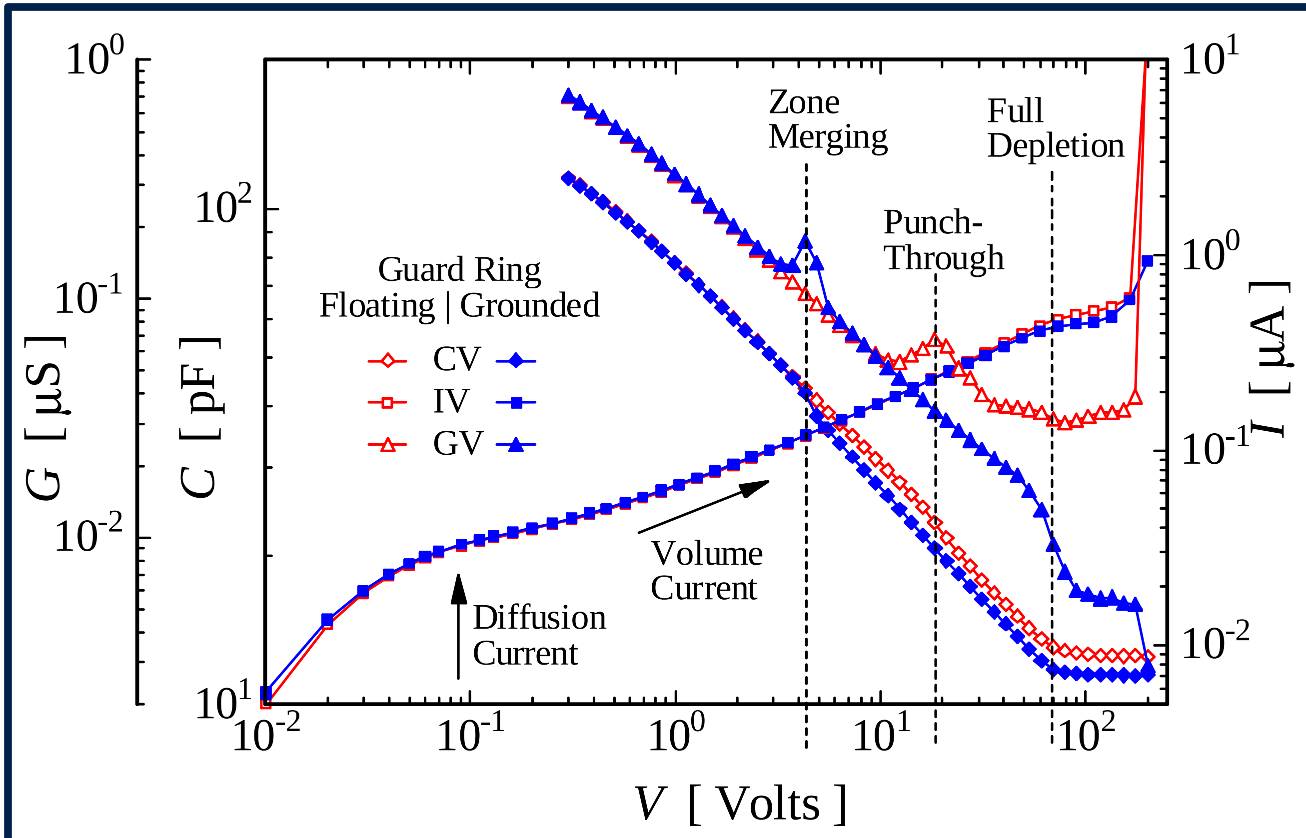


A lot of space is needed for isolating high voltages.

An area-saving technology requires careful optimization of the edge termination. This is often more difficult than the actual core device development.

Core device cross section considered in the TCAD simulations shown so far.

Edge Effects in Silicon Detectors

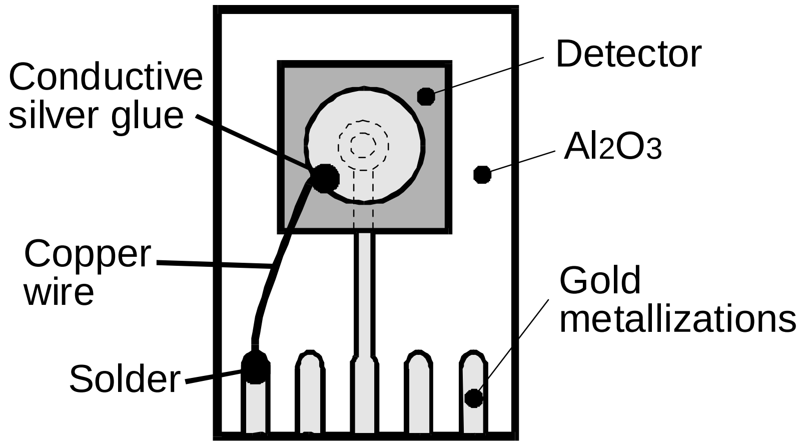


Source: H. Feick, PhD thesis

Although problems relating to diodes are rarely regarded as sufficiently appealing for a publication, mastering edge terminations and bipolar effects is considered a high art.

And Silicon detectors were my first steps in this direction.

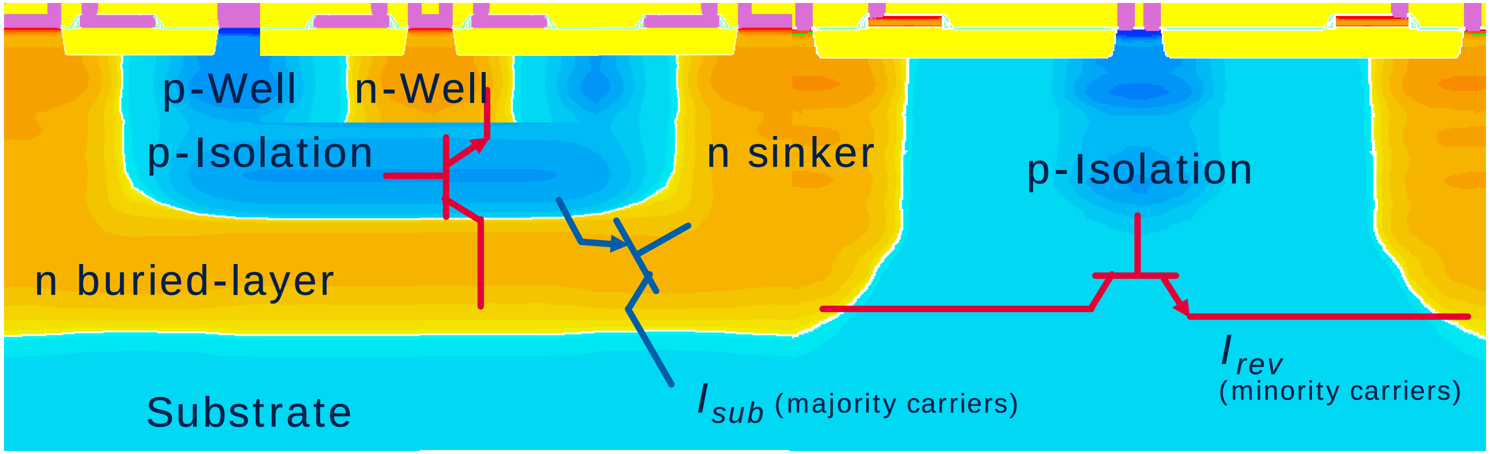
Lessons Learnt from Gunnar: Part 2
Goal Orientation and Risk Awareness



a) Reaching a goal is often much easier by copying a working solution from somebody else – this is very much true for the semiconductor industry.

b) Even barely noticeable details can endanger the entire project: Gunnar went to long ends to determine that the center line resistance to the backplane contact would be too high for high-frequency capacitance measurements. The layout was thus adjusted, the investment secured ☺.
There might be a little bit of over-engineering at work here, which is not so commonplace anymore, though.

Latch-up Risks in HV Technologies



Power switching can introduce significant substrate noise, especially if inductive loads are driven

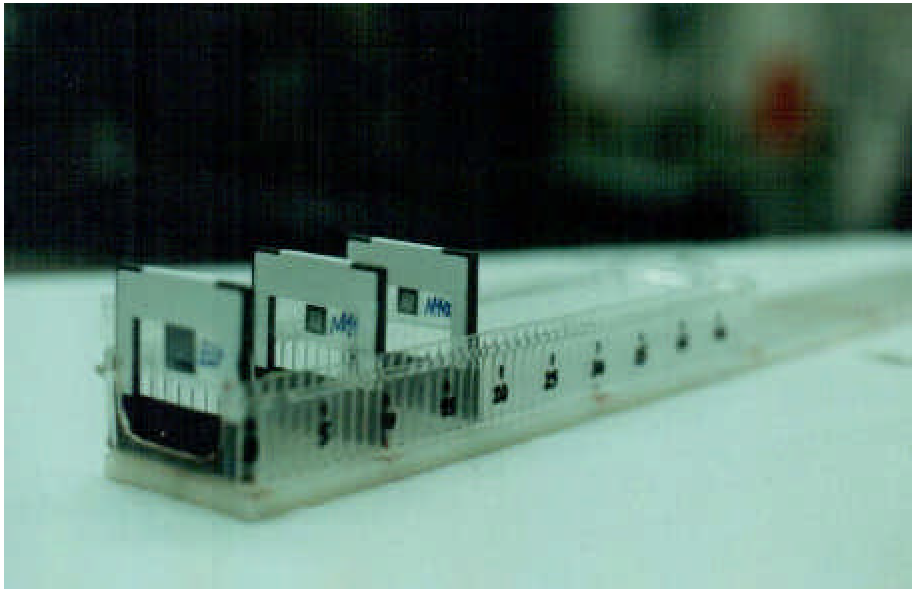
-> reverse current when minority carriers are injected (n-type region drops below substrate ground potential)

-> substrate currents when forward-biased p-n junction injects majority carriers into the substrate causing substrate potential variations

High-voltage isolation requires many parasitic bipolar paths to be minimized since they could potentially lead to latch-up problems.

Lessons Learnt from Gunnar: Part 3
Soft Skills: Dealing With Personnel

Well, well, there will be a lot of neutron scattering from this sample holder... But have it your way, for heaven's sake.



Yes, true, the neutron dose was probably a little off. But then, the radiation meter wouldn't show anywhere nearly as crazy numbers as for the old Aluminum sample holder, with all its bolts and nuts.

In order to avoid mutiny, it is always a good idea to listen and react to the wishes of your personnel – this is very much true for a company with many levels of hierarchy.

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Nuclear Instruments and Methods in Physics Research A 465 (2001) 60–69

NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A

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Developments for radiation hard silicon detectors by defect engineering—results by the CERN RD48 (ROSE) Collaboration☆

G. Lindström[a,*], M. Ahmed[b], S. Albergo[c], P. Allport[d], D. Anderson[e], L. Andricek[f], M.M. Angarano[g], V. Augelli[h], N. Bacchetta[i], P. Bartalini[g], R. Bates[j], U. Biggeri[k], G.M. Bilei[g], D. Bisello[i], D. Boemi[c], E. Borchi[k], T. Botila[l], T.J. Brodbeck[m], M. Bruzzi[k], T. Budzynski[n], P. Burger[o], F. Campabadal[p,q], G. Casse[d], E. Catacchini[k], A. Chilingarov[m], P. Ciampolini[g], V. Cindro[r], M.J. Costa[p,q], D. Creanza[h], P. Clauws[s], C. Da Via[b], G. Davies[t], W. De Boer[u], R. Dell'Orso[v], M. De Palma[h], B. Dezillie[w], V. Eremin[x], O. Evrard[o], G. Fallica[y], G. Fanourakis[z], H. Feick[aa], E. Focardi[k], L. Fonseca[p,q], E. Fretwurst[a], J. Fuster[p,q], K. Gabathuler[ab], M. Glaser[ac], P. Grabiec[n], E. Grigoriev[u], G. Hall[ad], M. Hanlon[d], F. Hauler[u], S. Heising[u], A. Holmes-Siedle[b], R. Horisberger[ab], G. Hughes[m], M. Huhtinen[ac], I. Ilyashenko[x], A. Ivanov[x], B.K. Jones[m], L. Jungermann[u], A. Kaminsky[l], Z. Kohout[ae], G. Kramberger[r], M. Kuhnke[a], S. Kwan[e], F. Lemeilleur[ac], C. Leroy[af], M. Letheren[ac], Z. Li[w], T. Ligonzo[h], V. Linhart[ae], P. Litovchenko[ag], D. Loukas[z], M. Lozano[p,q], Z. Luczynski[ah], G. Lutz[f], B. MacEvoy[ad], S. Manolopoulos[j], A. Markou[z], C. Martinez[p,q], A. Messineo[v], M. Mikuž[r], M. Moll[ac], E. Nossarzewska[ah], G. Ottaviani[ai], V. Oshea[j], G. Parrini[k], D. Passeri[g], D. Petre[l], A. Pickford[j], I. Pintilie[l], L. Pintilie[l], S. Pospisil[ae], R. Potenza[c], V. Radicci[h], C. Raine[j], J.M. Rafi[p,q], P.N. Ratoff[m], R.H. Richter[f], P. Riedler[ac], S. Roe[ac], P. Roy[af], A. Ruzin[aj], A.I. Ryazanov[ak], A. Santocchia[ad], L. Schiavulli[h], P. Sicho[al], I. Siotis[z], T. Sloan[m], W. Slysz[n], K. Smith[j], M. Solanky[b], B. Sopko[ae], K. Stolze[am], B. Sundby Avset[an], B. Svensson[ao], C. Tivarus[l], G. Tonelli[v], A. Tricomi[c], S. Tzamarias[z], G. Valvo[y], A. Vasilescu[ap], A. Vayaki[z], E. Verbitskaya[x], P. Verdini[v], V. Vrba[al], S. Watts[b], E.R. Weber[aa], M. Wegrzecki[n], I. Wegrzecka[n], P. Weilhammer[ac], R. Wheadon[v], C. Wilburn[aq], I. Wilhelm[ar], R. Wunstorf[as], J. Wüstenfeld[as], J. Wyss[i], K. Zankel[ac], P. Zabierowski[ah], D. Zontar[q]

☆Presented at the LEB workshop Cracow, September 2000, see CERN report CERN 2000-010 CERN/LHCC/2000-041.

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Lessons Learnt from Gunnar: Part 4 Leadership

Forming coalitions, joining forces, motivating people, and taking the leading role is key to a successful career.

And Gunnar has always been a true master at this.

Thank you.

Infineon Dresden

Quality meets Innovation.

- Broad Technology Base
- Prime Security Standards
- Fast Customer Samples
- Advanced Automation
- Customer Embedded
- High Flexibility
- Rapid Ramps
- Zero Defect
- Top Experts
- Open Mindset
- More than Moore
- World Class Yields
- Short Cycle Times

Infineon

Never stop thinking

ENERGY EFFICIENCY MOBILITY SECURITY

Innovative semiconductor solutions for energy efficiency, mobility and security.