- Vertex Detectors at the LHC and LHC Upgrade
- The LHCb Upgrade and the VELO
- From Timepix to VELOpix
- VELO Upgrade outline
- The Timepix particle tracking telescope
- First results and future plans

Paula Collins On behalf of the LHCb VELO Upgrade group





Pixels and strips

- For the central detectors pixels are mandatory for the inner layers to keep the occupancy numbers reasonable
- ALICE pixel inner layer: max. occupancy for central
- Pb-Pb 2.1% (max. 8000 tracks/|η| at mid-rapidity)
- Silicon strips can be used at larger radii or (in the case of LHCb) to minimise material





Huge variation in silicon parameters;

From the tiny







LHC had a bright startup in 2010

250 bunches with ca. 2.6 10^{13} ppb Luminosity > 10^{32} cm⁻² s⁻¹ → Emittance in collision < 3 µm



Potential to achieve > 5 fb-1 in 2 years

Plan to run at 7 TeV for 2011 and 2012 $\,$

18 month shutdown in 2013-2014 to repair splices

Decision also driven by equally bright start for experiments – many channels and searches overtaking Tevatron after just 36 pb⁻¹ of data

Elle ⊻iew <u>S</u> ettings <u>A</u> udio ⊻ideo <u>N</u> avigation <u>H</u> elp ▲ II II II III III → → → → III III IIII →	VLC	media player		
14-Oct-2010 03:39:29 Fi	II #: 1418 Enei	rgy: 3500 GeV	I(B1): 2.62e+13	I(B2): 2.61e+13
Experiment Status Instantaneous Lumi (ub.s)^-1 BRAN Luminosity (ub.s)^-1 Fill Luminosity (nb)^-1 BKGD 1 BKGD 2	ATLAS PHYSICS 101.346 103.804 4.2 0.047 288.000	ALICE STANDBY 0.187 0.184 0.143 0.452	CMS NOT_READY 101.073 97.665 3.5 17.689 0.002	LHCb 93.180 81.519 3.4 0.432 1.315
BKGD 3	17.000	0.016	2.246	0.374
Performance over the last 24 Hrs 25613 2113 1013 5013 0500 0500 0500 0500	11:00 14:	00 17:00	20:00 23:00	Update:: 0333:21
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			Day in 2	2011
				3/25/11

First phase of upgrades: 2010-2020

- This decade will see the initial operation of the LHC and the increase of energy and luminosity towards the design luminosities.
- Goal of extended running in the second half of the decade to collect ~100s/fb
 - 80% of this luminosity in the last three years of this decade
 - About half the luminosity would be delivered at luminosities above the original LHC design luminosity
- Motivation for upgrades during this phase
 - may be based on required performance for higher luminosity, better physics performance, better reliability of operation

2010-2012 Ramping up to fewx10³³ @ 7TeV Up to 5 fb-1 delievered

Long shutdown Splice repairs

2015-2016/7 Ramping up to 10³⁴ Up to 100 fb-1 delievered

Injector and LHC Phase I upgrades

2018-2020/1 Ramping up to 10³⁴ Up to 100 fb-1 delievered per year

> Towards High Luminosity LHC 3/25/11



3/25/11

CMS Snapshot





- Innermost layer with reduced radius
- Additional outermost layer at 160 mm
- ~2x radial acceptance
- ~65% more pixels
- CO2 cooling
- Reduced material for more layers!



ATLAS Snapshot

Insertable B-layer (IBL)

- Addition to current B-layer inside the current ones
- × New FE-I4 ASIC in 130nm
 - 4 * area of FE-I3
 - 27k 50x250um pixels
 - 8b/10b on chip
- Prototype successful promising testbeam and irradiation results, irradiation of hybrid packages underway
- Install in Phase o (Success driven)
- Schedule recently accelerated by LHC timetable
- Move services to area with lower radiation
- Flat staves, and active/slim edges
- Replace entire inner detector in Phase II (1-2 10¹⁶ regime for innermost layer)







3/25/11

20 25 Cluster Charge (TOT)









Cooling system : evaporative CO₂

3/25/11

Module support and cabling to vacuum wall

Detector box & RF foil

 Detectors are entirely contained within a secondary vacuum (~10⁻⁷ mbar) seperated from the primary beam vacuum

(<10⁻⁹ mbar)

 RF pick-up from the passing beam is guarded against with a ~300µm-thick aluminium foil.

And the VELO moves ...

 At all times other than "STABLE BEAMS", the VELO sits back ~3 cm from beam-line.

 Beam's eye view of the open VELO

Vertexing performance:

- 2 key 'figures of merit' :
 - Primary vertex resolution: depends on the number of tracks in the event.

For 25 tracks (typical) : 13 um (X and Y), 77 um (Z)

- Impact parameter resolution:
 - Depends on the transverse momentum p_T of the track.

~13 um + 26 um/p_T in x,y

~16 um + 30 um/p_T in 3d

• The VELO is the main tracking and vertexing detector both for the online software trigger (HLT1) and the offline event reconstruction.

'Other applications' of excellent vertexing.

- Imaging of the beam bunches, by reconstructing proton - residual gas collisions.
 - Used for luminosity measurement. Unique to LHCb. Continuous and non disruptive.
 - 'SMOG' experiment will inject Xenon gas to enhance this effect.

• 'Radiography' or self- imaging of the VELO by reconstructing interactions in material :

LHCb physics programme well underway

- In 2010 LHCb accumulated 37 pb⁻¹ with luminosity close to design, but significantly higher pileup
- Excellent trigger and reconstruction performance
- Confidence in LHCb physics programme
- $B_{s}^{-} > \mu^{+}\mu^{-} < 1.2 \text{ x } 10^{-8} 95\% \text{ C.L.}$
- Clean ∆m_s measurement at Tevatron precision and with 2x smaller systematic error
- Production cross sections in beauty and charm
- Ingredients in place for core CPV programme

LHCb Upgrade Objectives

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- Pursue core physics objectives with
 - Order of magnitude increase in integrated luminosity
 - Flexible software trigger able to focus on NP channels hinted at or measured in first phase – by LHCb or the GPDs

LHCb upgrade also accesses

- Lepton flavour physics, flavour violating t decays
- Charm physics
- Electroweak physics and exotics

	B_s ->J/ $\psi\phi$	Determination of γ	$\mathbf{B}_{s} \rightarrow \mu^{+}\mu^{-}$	$B_0^->K^*\mu^+\mu^-$
NOW	Find, or exclude large deviations from SM	Measure with 4º uncertainty	Measure SM value or large deviations	Measure zero crossing point of asymmetry
UPGRADE	Precise phase measurement	Achieve <1º precision and match (future) Lattice QCD	Make precision measurement and extend to B`->µ ⁺ µ ⁻	Measure full kinematic distributions

LHCb – upgrade

- Can confidently expect to run at nominal luminosity 2 x 10³² from 2011, after which time to double statistics is too low
- Aim of upgrade is to increase the event yield by a factor 10-20 by
 - Increasing luminosity by a factor 5 in the first phase and ultimately by a factor 10
 - Increasing the trigger efficiency in hadronic channels by a factor 2
- This can be done without serious increases in occupancies, so basic detector layout can remain
- Current experiment has bottle neck with reduction to 1 MHz imposed at the first level trigger, built into FE electronics of experiment

Solution: Execute trigger algorithms on ALL data in software -> more sophisticated trigger

A new **DAQ** system must transfer all, zero-suppressed front-end data straight into a large computer farm, through a huge optical network & router. VELO to be completely replaced

VELO Upgrade radiation challenge

At 7 mm from beam we accumulate 370 MRad or 8 x 10^{15} n_{eq}/cm².

Distance from silicon tip to thermal connection too great

Recent RD50 studies have shown that silicon irradiated at these levels still delivers a **signal** of ~ 8ke⁻ / MIP

Efficient heat removal mandatory to avoid thermal runaway!

Diamond cooling substrate candidate solution Electronics must be of sufficiently low noise to cope with reduced signal

VELO upgrade data rate challenge

- Electronics has to digitise, zero suppress and transmit event data at 40 MHz
- By pixel standards the occupancy of the VELO is miniscule, but the data rate is HUGE
- 1 chip has to transmit 10-20 Gbit / second
- Our current granularity, occupancies = ok but FE electronics and DAQ are not

The Medipix – from HEP to Medicine and back again

Medipix2 (2002) – Photon Counting

Each hit in the sensor is converted into a count in the 14 bit counter

Noise and below threshold events are not counted at all

1000 electron noise floor

The shutter closes and the data are shifted out

Charge deposition studies with various Isotopes Space Dosimetry

Courtesy L. Pinsky, Univ. Houston 3/25/11

LiF (50 µm) used for thermal neutrons detection

Al (50 and 100 μm) used to stop low energy electrons and photons

Uncovered accepts all particles low sensibility to neutrons

PE (1.3 mm) used for fast neutrons detection

PE + Al used for fast neutrons detection removing low energy electron photons contributions

¹J. Jakubek, S. Pospisil, M. Suk, D. Turecek Paula Collizs Vykydal and the Group at Prague CTU

Low Energy Electron Microscopy

Images of Graphene Flakes presented to the Medipix2 collaboration by I. Sikharulidze, Leiden

'Medipix2 applied to low energy electron microscopy', Ultramicroscopy 110 (2009) 33 - 35

Timepix -> VELOPix (via Timepix2)

Why the Timepix decision

• Square Pixel size (55µm x 55 µm)gives equal spatial precision in both directions, removing the need for double sided modules and saving a factor 2 in material

- IBM 130 nm CMOS process
- Low occupancy is suited to ToT measurement, with no loss from 1 us deadtime

Changes needed

- Replace shutter based readout/acquisition scheme by continuous, deadtimeless operation
- Sustained readout of pixels with maximum flux 5 particles /cm²/25 ns
- Reduced ToT range and resolution
- Add bunchtime identification good within 25 ns

Timepix Evolution

- Timepix2 is an important step towards Velopix
 - Similar front end
 - Fast column bus
 - Data Driven readout
 - Simultaneous Time Over Threshold and Time of Arrival measurements
- Timepix2 by end 2011
- Aim to have first Velopix by 2012

VELOPix: analog front-end requirements.

- Reduce timewalk: <25 ns @ 1ke⁻ threshold.
 - × Faster preamplifier and discriminator of Timepix2 covers and exceeds this requirement
- I_{krum} range 5 ...40nA
 - \Rightarrow sensitivity 750 ... 6000 e⁻/25ns.
 - × ⇔ 20 ke⁻ signal returns to baseline in 660 ... 83 ns
- Reduced non-linearity near threshold.
- Analog power consumption <10 uW/ pixel.
- Higher preamplifier gain (~50mV/ke⁻).
 - × reduced ENC, lower detectable charge (~500 e⁻)
 - reduced linear range (30 ke⁻) : better suited to Si -tracking
- Design by X.Llopart(CERN) and V.Gromov (NIKHEF) very advanced.

Fit to Surrogate function at threshold ~ 1500 electrons, ikrum 5

VELOPix:

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- Digital :
 - Simultaneous 4 bit Time-over-threshold and time identification (12 bit).
 - Data loss must be kept < 0.5% in worst conditions (6kHz pixel hit-rate).
 - × Limit ToT < 400ns.
 - × Adequate buffering & bus speeds.
 - Data driven readout.
 - SEU protection of logic & registers.
 - o multi-Gbit/s output links : 4 x 3.2Gb/s#
 - Design of superpixel, column bus and EOC logic very advanced (Tuomas Poikela).
- Total power budget <3W full chip.
- Radiation hardness TID 400Mrad.

Data rates

- Numbers at highest occupancies:
 - average particle rate per 'hottest' asic ~ 5 particles/25ns = 200MHz
 - average pixel cluster size ~2: (pessimistic assumption, 200um Si)

• Information bits per hit pixel : 32

- 4 bit : Time over Threshold value.
- 12 bit : bunch identification
- 16 bit : pixel address.
- => Single asic data rate can reach 13 Gbit/s !

• 30% data reduction can be achieved by 'clustering' data:

- share the bunch id (12bit) and address bits between neighbor pixels.
- × must be done before column readout, i.e. inside pixel array !
- most efficiently done in units of 4x4 pixels = "Super pixel"

Average #particles/event

1.3	1.0	0.6
5.3	2.6	1.0
*	5.3	1.3
	2.6	1.0
	1.0	0.6

Super pixel

• Super pixel layout: group digital logic in a common area.

- × Advantages:
 - Space saving : some functional blocks can be shared (time-multiplexed).
 - More efficient routing of power rails and global signals.
 - Better analog/digital isolation.
 - Digital column logic is synthesized with standar library. Ease, reliability, yield ...
- × Disadvantages:
 - bump pads on top of digital circuit:
 - => digital feedback in analog frontend. Shielding ?
 - Non-uniform analog input capacitance:
 - => Only small effect
- Status:
 - □ The verilog code for superpixel and digital column exists and has been laid out (Tuomas Poikela). Final simulations are done. Worst-case power estimate is ~840 mW, including clock distribution.
 - □ Use of a 'lower speed/lower power' library for IBM 130nm gives savings in space and power!

220 um

и —	colu	mn 0			column 1		S	c	olumn 63		_
A A A	A A dig A pix	4 gital kels	A A A A A A A A	A A A A A A A A A A A A A A A A A A A	4x4 digital pixels	A A A A A A A A	er pixel	A A A A A A A A A A A A A A A A A A A	4x4 digital pixels	A A A A A A A A A A A A A A A A A A A	row 63
A A A	A A A A A A A A A A A A A A A A A A A	4 gital kels	A A A A A A	A A A A A A A A A A A A A A A A A A A	4x4 digital pixels	A A A A A A A A	x4 supe	A A A A A A A A A A A A A A A A A A A	4x4 digital pixels		row 62
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	4x 55 um	(4 pixels)					9				

VELOPix. Address encoding

- Address encoding in 4x4 super pixel :
 - Super pixel address : 12 bit.
 - "Row hit indicator" : indicate which rows have hits (4 bit, always present).
 - O to 4 "row hit patterns" : indicate which pixels in row are hit (4bit).
 - Examples:

Gain compared to individual pixel address
Overall 20% data reduction

ddress	encoding
6 bit	20 bit
2 bit	24 bit
8 bit	28 bit
4 bit	32 bit
	ddress 5 bit 2 bit 3 bit 4 bit

ASIC design. Data reduction

- Sharing across super pixel boundaries :
 - Only in 1 direction (column)
 - Results in additional 10% data reduction.

Hit X1 will be transferred to super pixel n+1

• Reject large multiplicity event :

- If hit > N then no readout. (N is configurable and can be de-activated).
- Packet format:

Pixel matrix readout architecture.

- Pixel matrix readout architecture
 - Internal bus speeds:
 - Column bus : 8bit@40MHz=320 Mbit/sToken ring arbitration.
 - × Output bus : 16bit@320MHz=5 Gbit/s
 - Total ASIC output : ~12.8 Gb/s.
 - Buffering in :
 - × Super pixel : 2 clusters.
 - × Super pixel group FIFO : 3 clusters.
 - × Output FIFO: multi kbyte
- Simulation shows losses< 0.5% in highest occupancy conditions.
- Periphery & output links are under study.

VELO Pixel module.

- Sensor tiles: made of 3 readout ASIC's on a single sensor, with a guard ring of 500 um.
- 2 sensor tiles are mounted on opposite sides of the substrate.
- Substrate choices:
 - Diamond : excellent mechanical and thermal properties: => low mass
 - Carbon fiber/TPG or Al/ TPG.

Sensor R&D

• Planar silicon

- Thin sensors seem well suited to the high fluences
- R&D focussing on guard rings
- Several wafers in the pipeline with various manufacturers
- Irradiation of planar silicon + Medipix3 assemblies starts in May

Diamond

- Exciting option for removing thermal runaway headache
- Very radiation hard
- Double act: sensor and thermal path

3d sensors

- Potentially Super radiation hard
- Many Medipix/Timepix assemblies available

LHCb VELO meeting 24/09/10 Paula Collins

VELO Detector layout.

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- The full detector is composed of 26 planes.
- The modules on either side of the beam are staggered to create overlap regions.
- This layout has been simulated to be fully efficient (4 hit per track) in the LHCb acceptance 250 x 300 mrad.

Strip Option

- In case the material budget/power consumption of the pixel option falls beyond specifications or time limits, a backup strip option is being prototyped.
- Key points:
 - Optimisation of strip capacitance to bring down noise
 - Possible move to "spider web"
 - Increase in number of strips and better layout – expected occupancy at upgrade will be 0.5% for first phase
 - New chip also needed (synergy with IT)
 - IP resolution superior to pixels

Timepix Telescope Arm Prototype early 2010

USB2 readout – 700 tracks per second

6 pixel telescope planes angled in 2 dimensions to optimise resolution

Device Under Test moved and rotated via remote controlled stepper motor Fine pitch strip detector with fast electronics readout

Angled Planes to Boost Resolution

Hits that only affect one pixel have limited resolution (30um region in 55um pixel)

Tilting the sensor means all tracks charge share and use the ToT information in centroid, CoG calculations

Indicative Timepix events

Timepix Telescope Arm Prototype late 2010

- RELAXD readout from NIKHEF
- 55 frames per second over gigabit Ethernet
- 5,000k tracks per second readout

50,000,000 tracks recorded in 2 weeks

Eight different DUTs analysed

Added Time Tagging Capability to ~1ns

- Asynchronous SPS beam not suited to LHC systems designed for 25ns bunch structure
- Implemented a TDC which with Timepix ToA mode gives us ~1ns per track time stamping
- Able to provide and record synchronised triggers to 40MHz readout systems (TELL1)

Timepix Arm Performance Summary

- 1.5µm spatial resolution at DUT
- 1ns timing resolution
- Up to 5kHz track rate

Links to AIDA Project

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- Timepix Telescope arm is a AIDA Deliverable
- We have many exciting common areas of development
- Trigger Logic Unit: Currently we use 2 NIM crates and a VME TDC to perform timing tasks
 - Controlling the Shutter eg selecting X particles per frame
 - Providing triggers to external systems
 - Measuring the phase between synchronised and unsynchronised triggers
 - Santiago University in collaboration with the AIDA team are developing a portable based TLU replacement
- Other areas of overlap under investigation

Timepix data analysis

- Calibration of chip under excellent control
- Many lessons learned for Timepix2 design and necessary useful features for calibrating final chip
- 1st paper submitted: http://arxiv.org/abs/1103.2739

Scanning the pixel cells

Very precise tracking allows us to probe all kinds of details within the pixel cells, allowing us to to

- Identify delta rays
- Investigate threshold effects
- •Measure pixel diagonal resolution
- Measure timewalk
- •Measure efficiency etc. etc.

Example Frame from 2010 Testbeam

A few highlighted results:

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Resolution as a function of angle Resolution [micron] 10V resolution 16 100V resolution (reference) 14 12 10 8 6 10 15 20 Track Angle [degrees] -20 -15 -10 -5 0 5

10V data (close to depletion)100V data (overdepleted)There is an enormous gain at lower voltagePossible advantage for VELO underinvestigation

Resolution as a function of # bits

Resolution as a function of number of bits (shown for three different angles) Input to Timepix2/Velopix design 4 bits and above are safe 3 bits is close to resolution degradation

R&D on pvCVD diamond sensors Strasbourg telescope

Charge Collected (ADC)

Goal: produce 400 μm sensors and compare their performance with 150 μm Si at different level of irradiation

First step: laboratory and test bench studies of 750 µm sensors in a test beam (CERN RD42 test beam with Strasbourg telescope)

Conclusions

- The VELO upgrade is on course for 2017/2018 installation
- The VELOPix ASIC is an ambitious and performant chip on course to deliver the needed specifications for the VELO modules
- The LHCb physics programme is on course to deliver full results with the first phase of operation and looks forward to a great, upgraded future
- Hope I've been able to give you a "flavour" of what we are doing Thanks for listening

Moving to Full Telescope Arms

- Major hardware work remaining is to make the system easier to set up and use
- Very strong overlap with proposed AIDA work

ALICE Inner Tracking System - ITS

ITS consists of 6 concentric barrels of silicon detectors (pixels, drift, double sided strips)

- Radial coverage from 3.9 cm to 43 cm)
- D devices (pixels and drift)
- PID with drift and strips
- □ Total material budget ITS <8% X_o, pixels 1.14 % X_o per layer
- Pixel trigger: each pixel chip creates FastOr signal which is contributing via dedicated trigger system to the Lo trigger decision (bg-noise rejection in p-p, event selection in HI)

Event from first HI collisions in 2010

Medipix2 Applications

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- The most commercialized of the current chips and being sold by PANalytical (NL) in X-Ray Diffractometers
- Also active applications in
 - Material Analysis
 - Medical Imaging
 - Synchrotron Light Source Instrumentation
 - Micro CT material analysis
 - Proton Beam Monitoring (at the SPS)
 - Electron microscopy
 - Mass spectrometry
 - Neutron Imaging
 - Charged Particle Dosimitry

