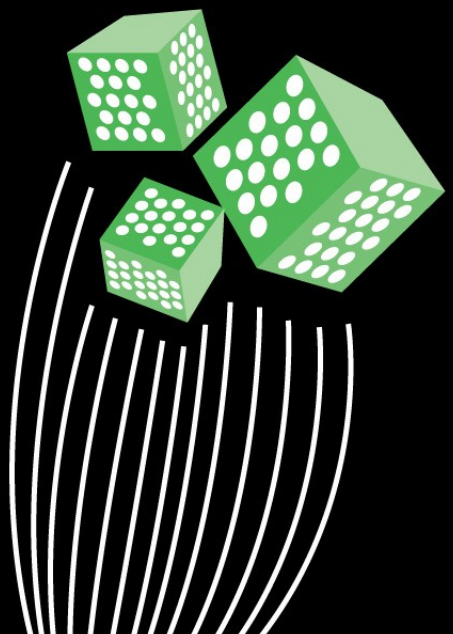
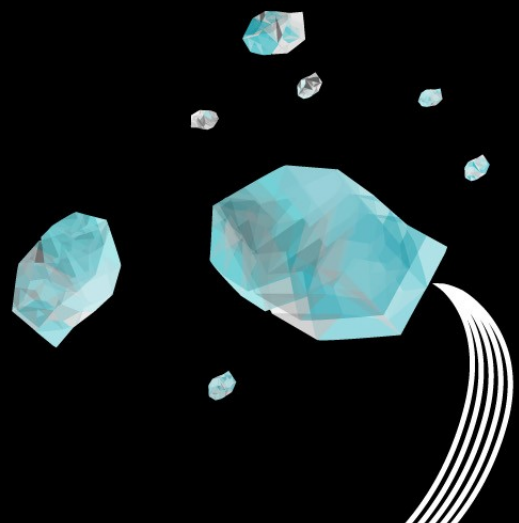
UNIVERSITY OF TWENTE.

Chip Post-processing for Particle Detectors

Jurriaan Schmitz

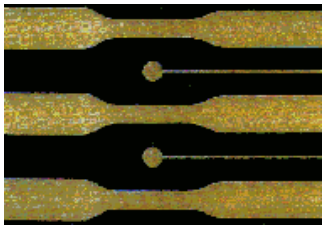




About Jurriaan Schmitz

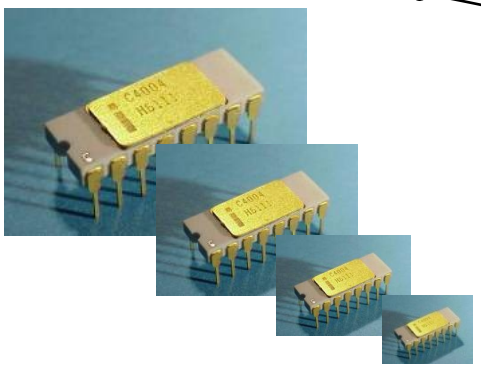
Ph.D. experimental physics 1994

Universiteit van Amsterdam/NIKHEF



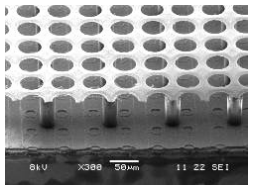
Senior Scientist at Philips Research

1994-2002



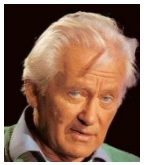
Full professor at University of Twente

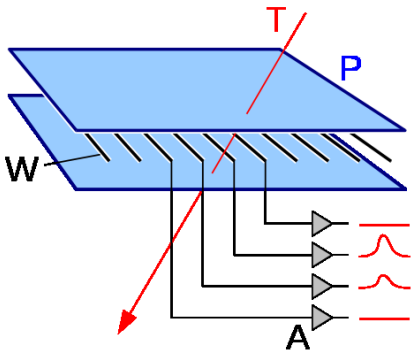
2002-present

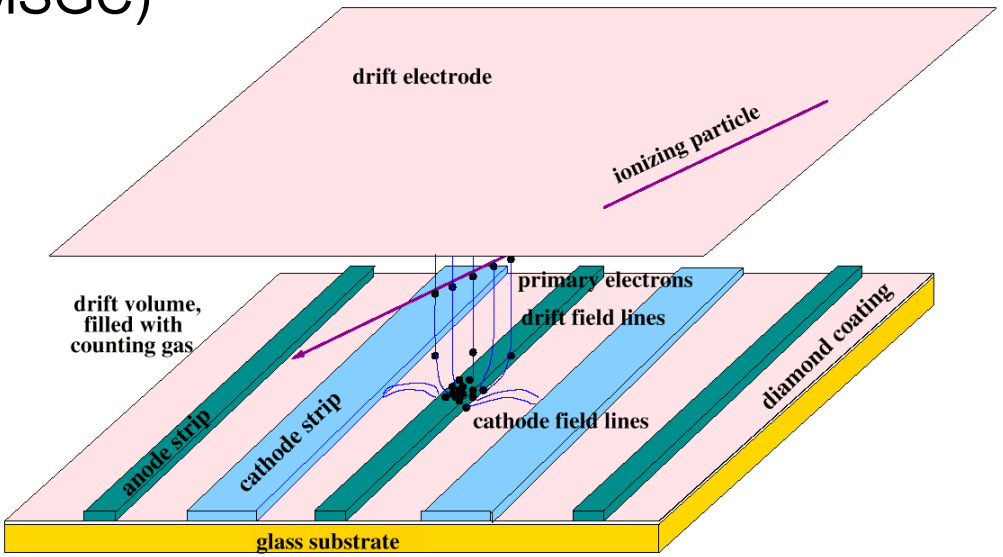


My Ph.D. work at NIKHEF 1990-1994

- Detector Research and Development
- Micro Strip Gas Counter (MSGC)







Key results:

- DME/CO_2 gas mixture
- MC simulation of detector response
- Invention of the M**T**GC
- Study of preamplifier optimization
- Study of application in LHC experiments (…)

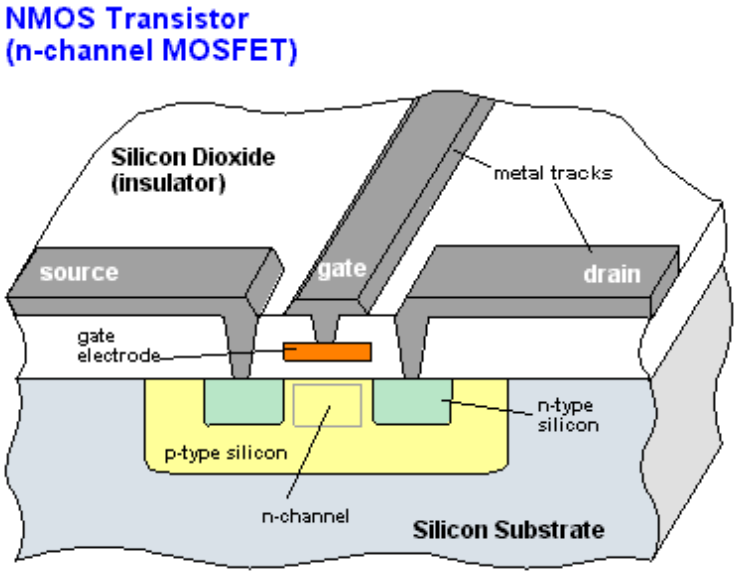
My work at Philips Research 1994-2002

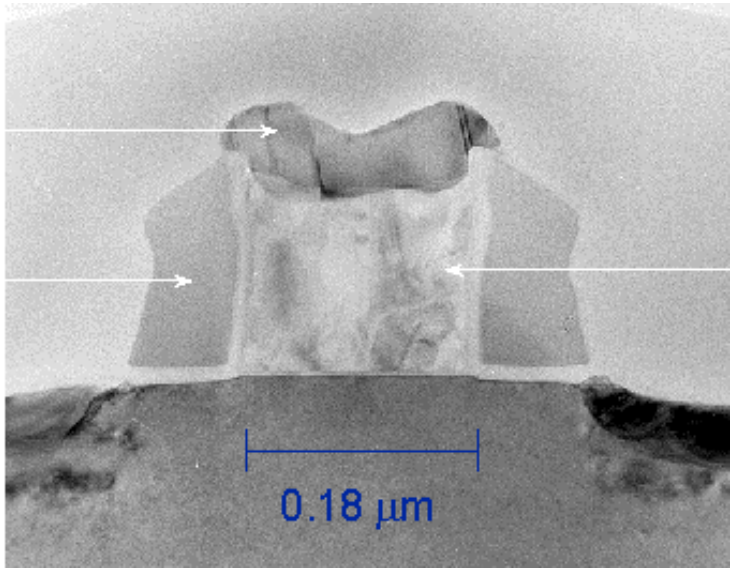
CMOS transistor downscaling:

- How to improve the fabrication process to make a smaller MOS transistor

Key results:

- 15 US patents
- Many IEEE related activities (conference organization etc.)
- EU projects
- Work experience at IMEC (BE)
- Job offer from the UT





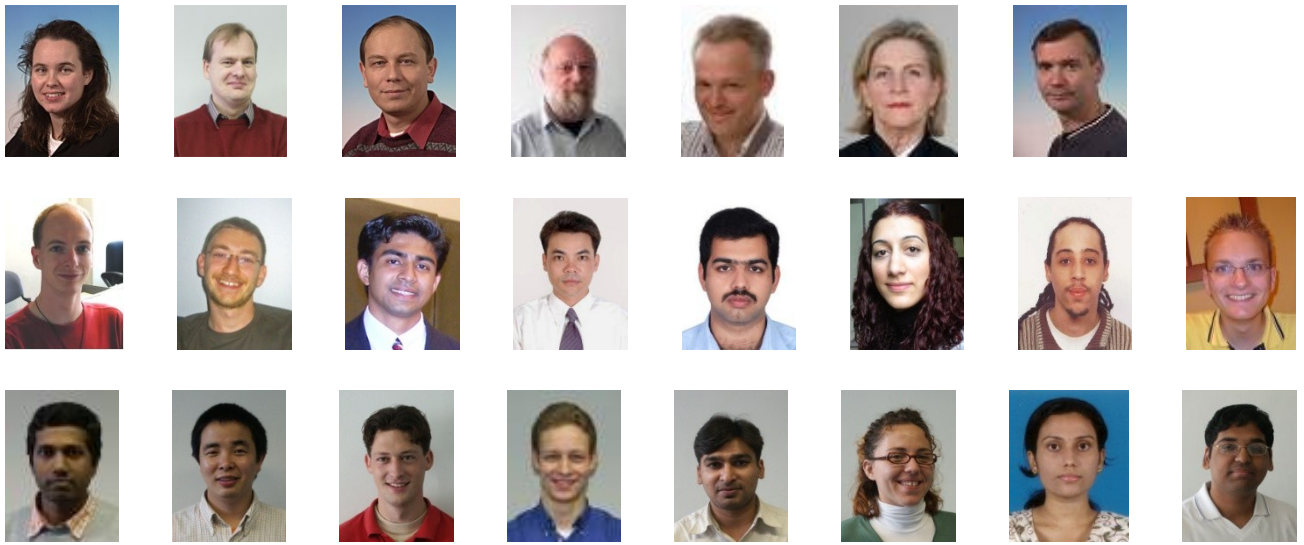
My work since 2002

Full professor of Semiconductor Components

- Research on microtechnology
- Make new types of microchips
- Use the Pizza technology approach

+ teaching

+ leading a group of ~25 researchers



Outline

Part I: the technology foundation

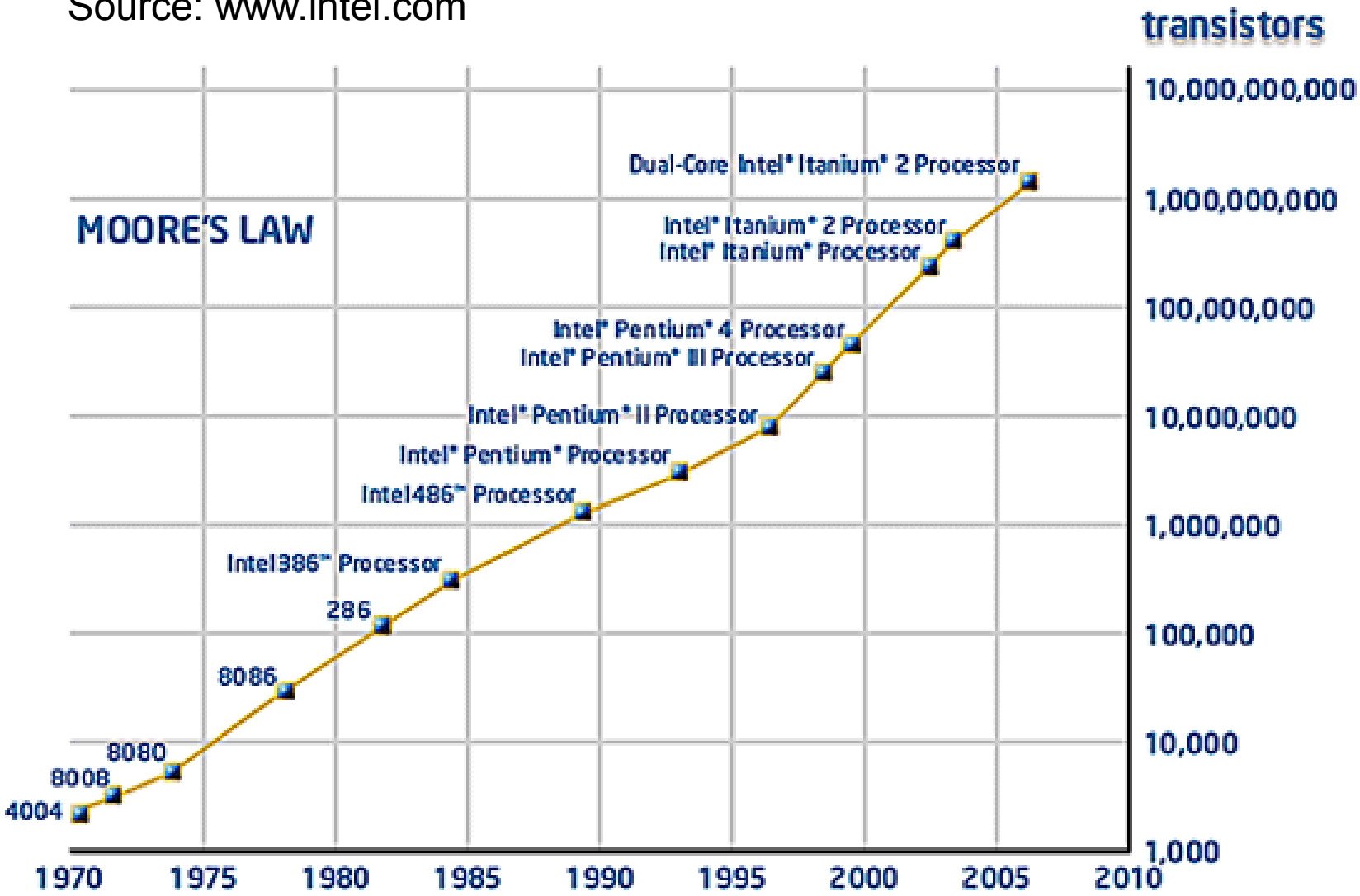
- The making of CMOS microchips
- Integration of CMOS with sensors / MEMS
- The success of pizza-technology
- Recent results

Part II: radiation imaging

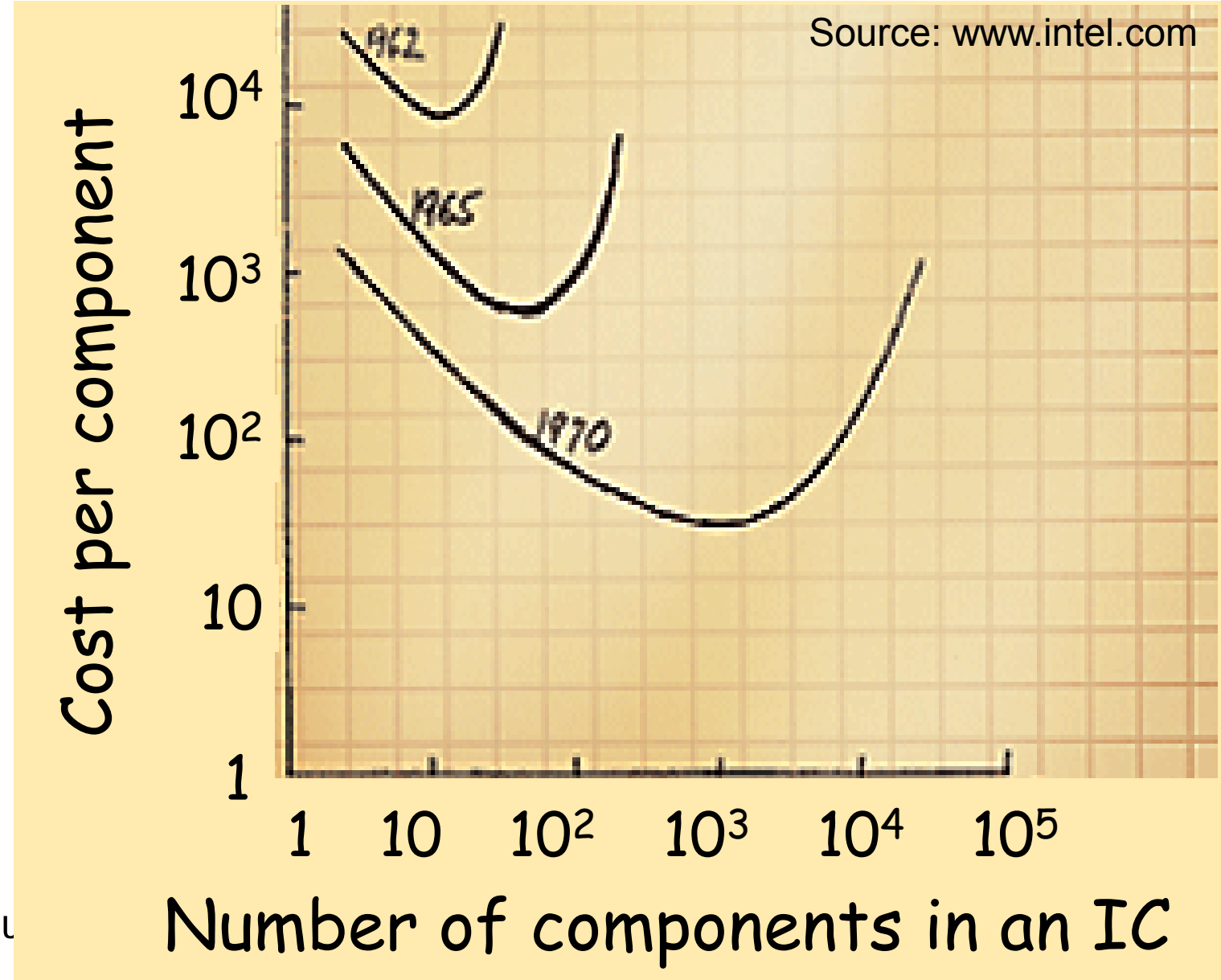
- InGrid detector fabrication
- Results with InGrid detectors
- Perspective

Moore's ~~Law~~ *Trend*

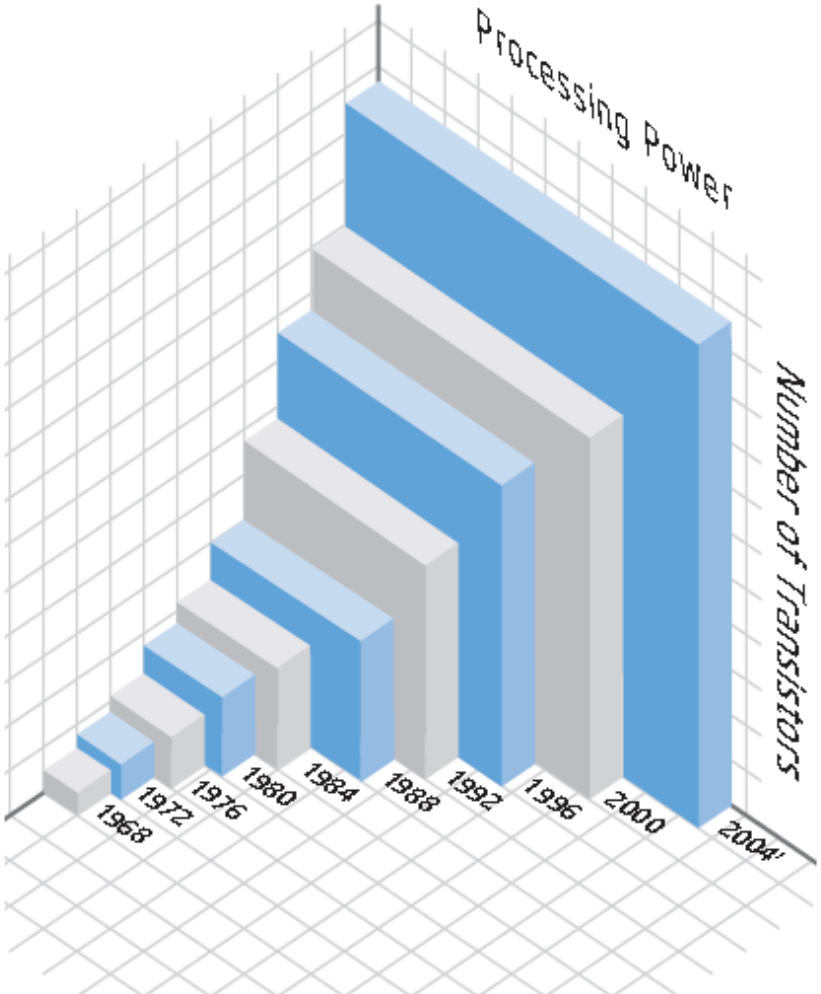
Source: www.intel.com

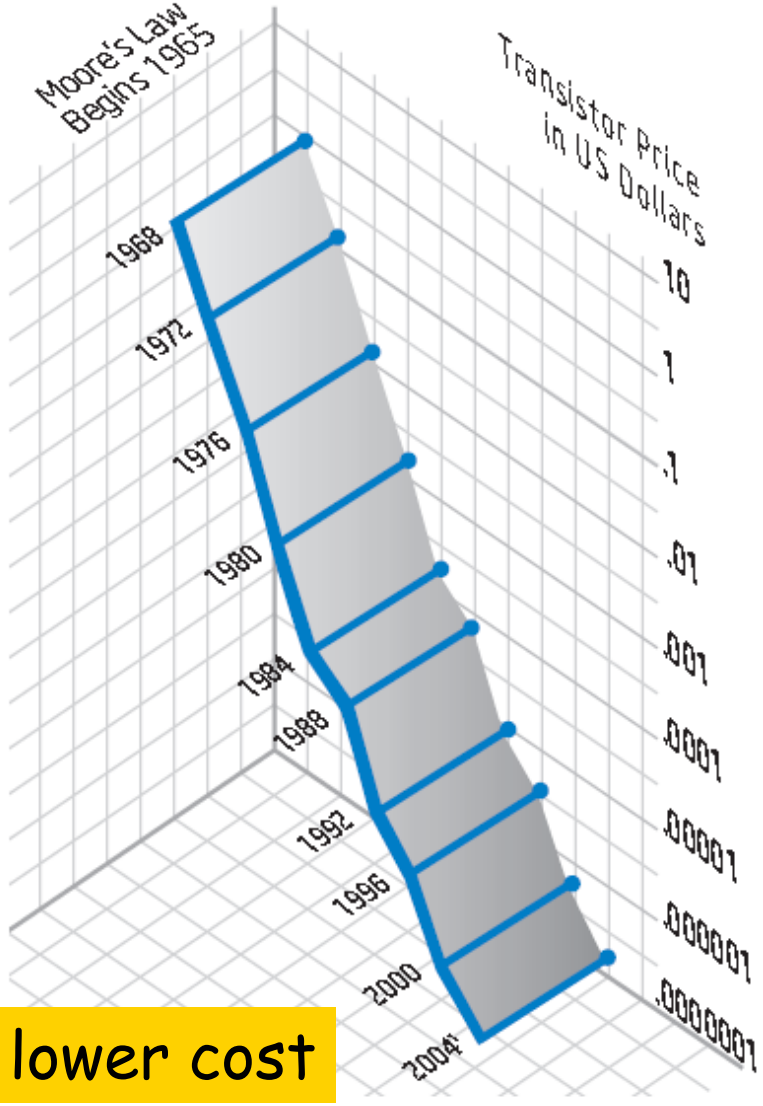


Moore's Trend explained



Source: www.intel.com

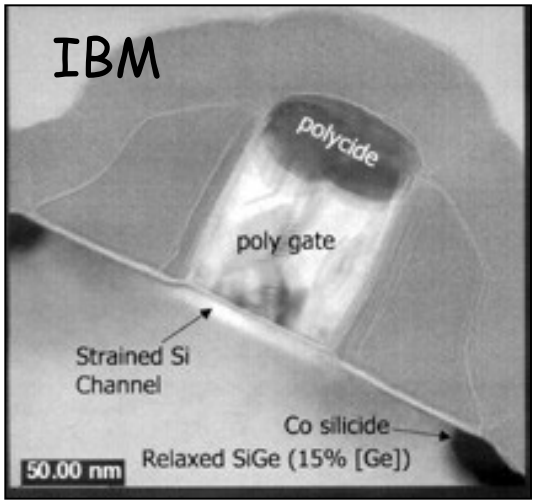


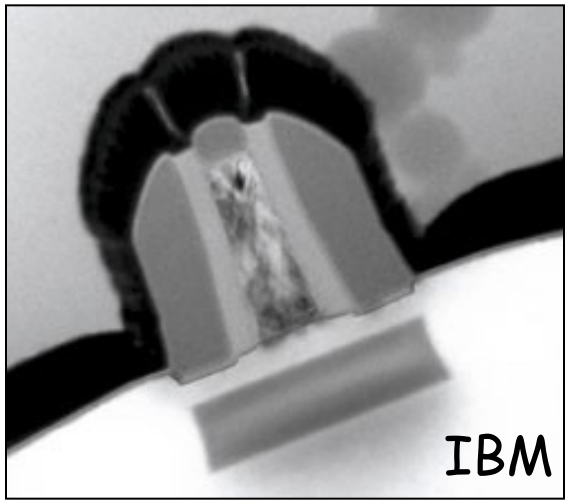


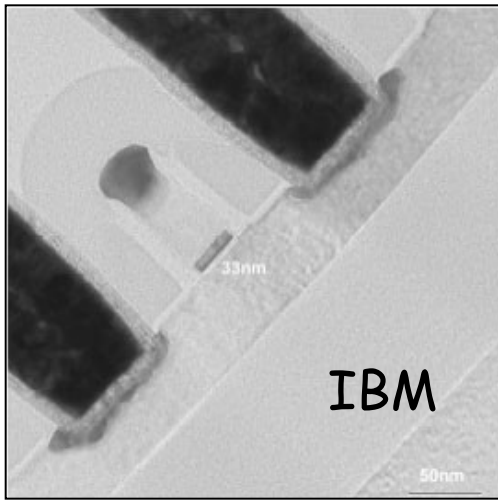
More performance…

… at lower cost

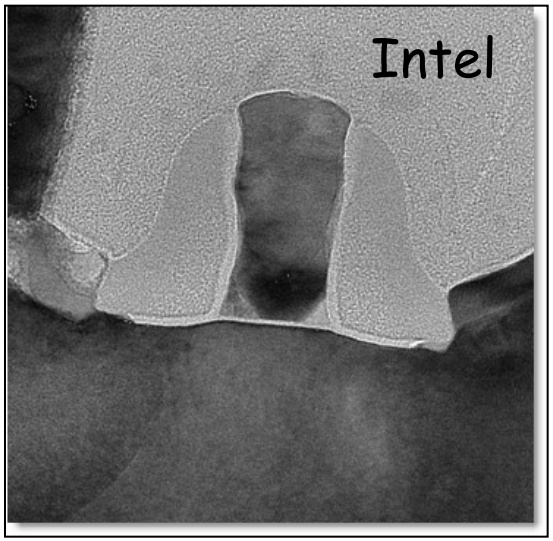
The state of the art (1): CMOS



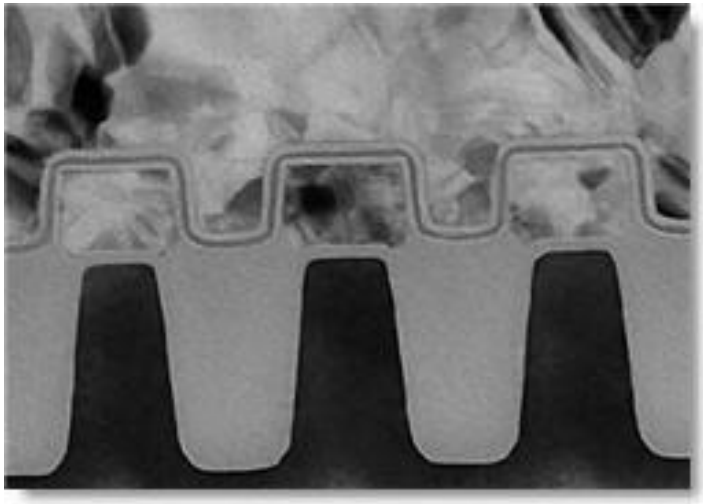


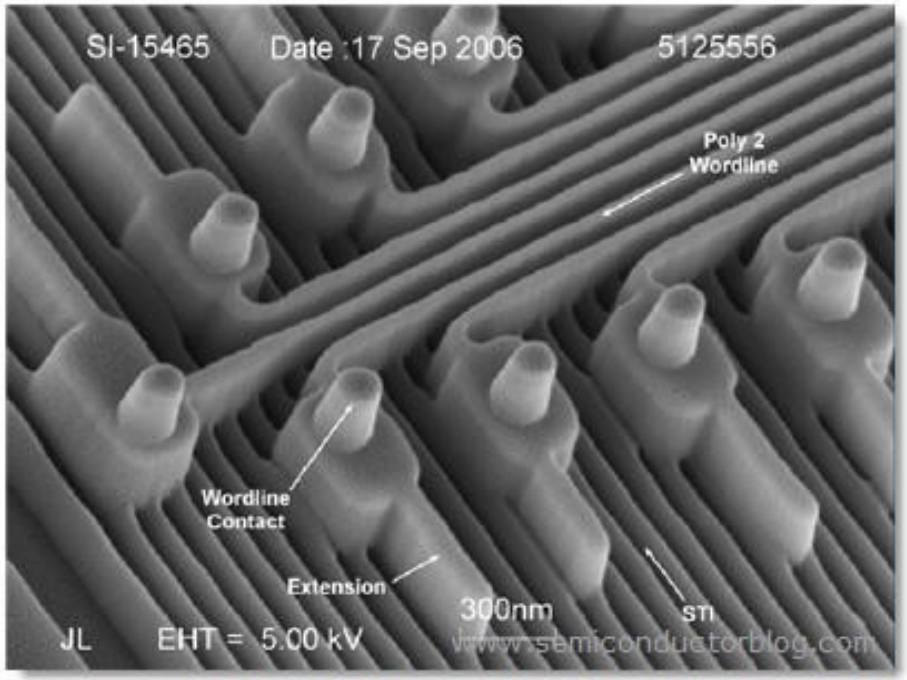


- Nanometer precision
- Sub-ppm materials purity



The state of the art (2): FLASH

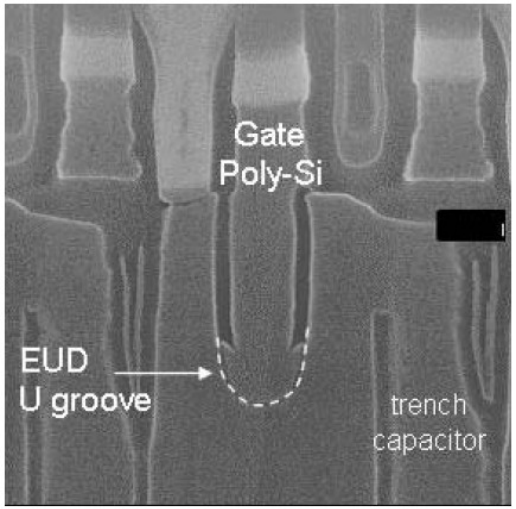


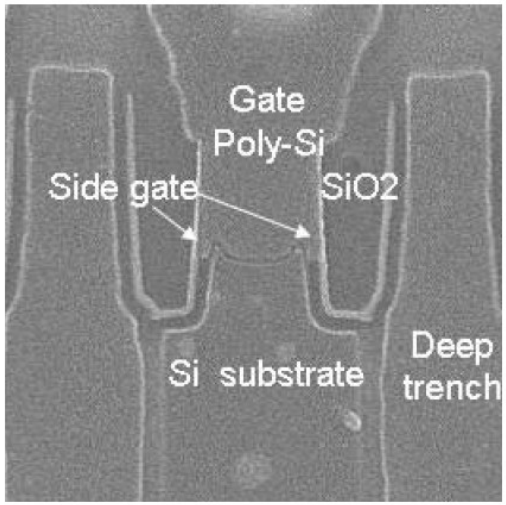


High magnification SEM image of IM Flash Technologies (IMFT) 4G 50nm NAND Flash (source: Semiconductor Insights)

- Nanometer precision
- Sub-ppm materials purity

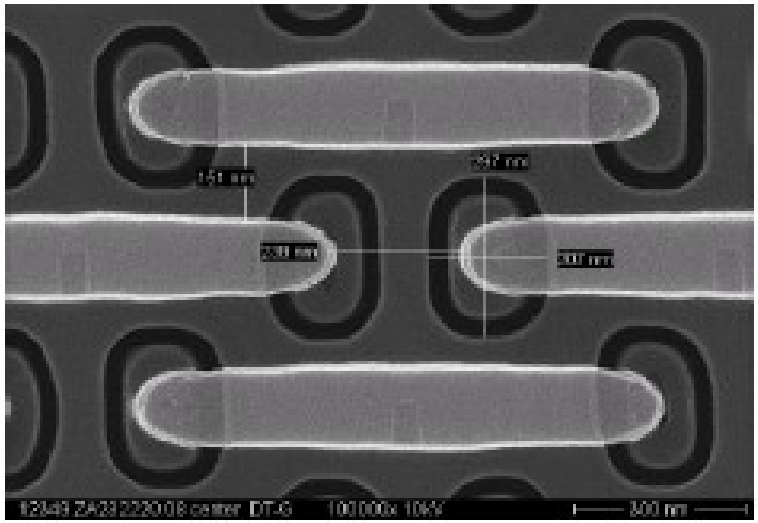
The state of the art (3): DRAM





Qimonda

SAMSUNG



- Nanometer precision
- Sub-ppm materials purity

The manufacturing of a microchip

Process steps:

- Oxidation
- Photolithography
- Etching
- Diffusion
- Implantation
- Deposition
- Cleaning
- Polishing (CMP)

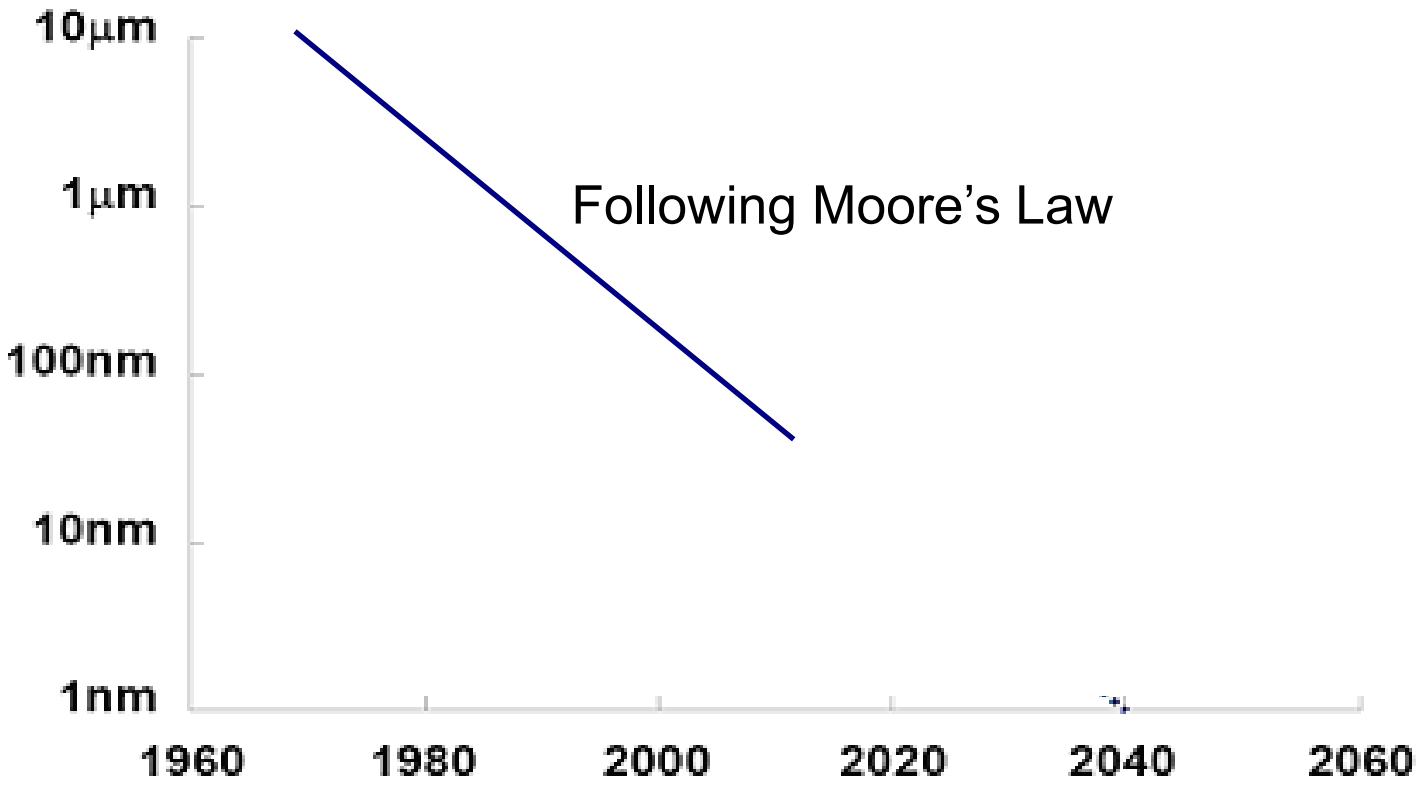
Complete process:

300 - 500 process steps

20 - 50 lithography steps

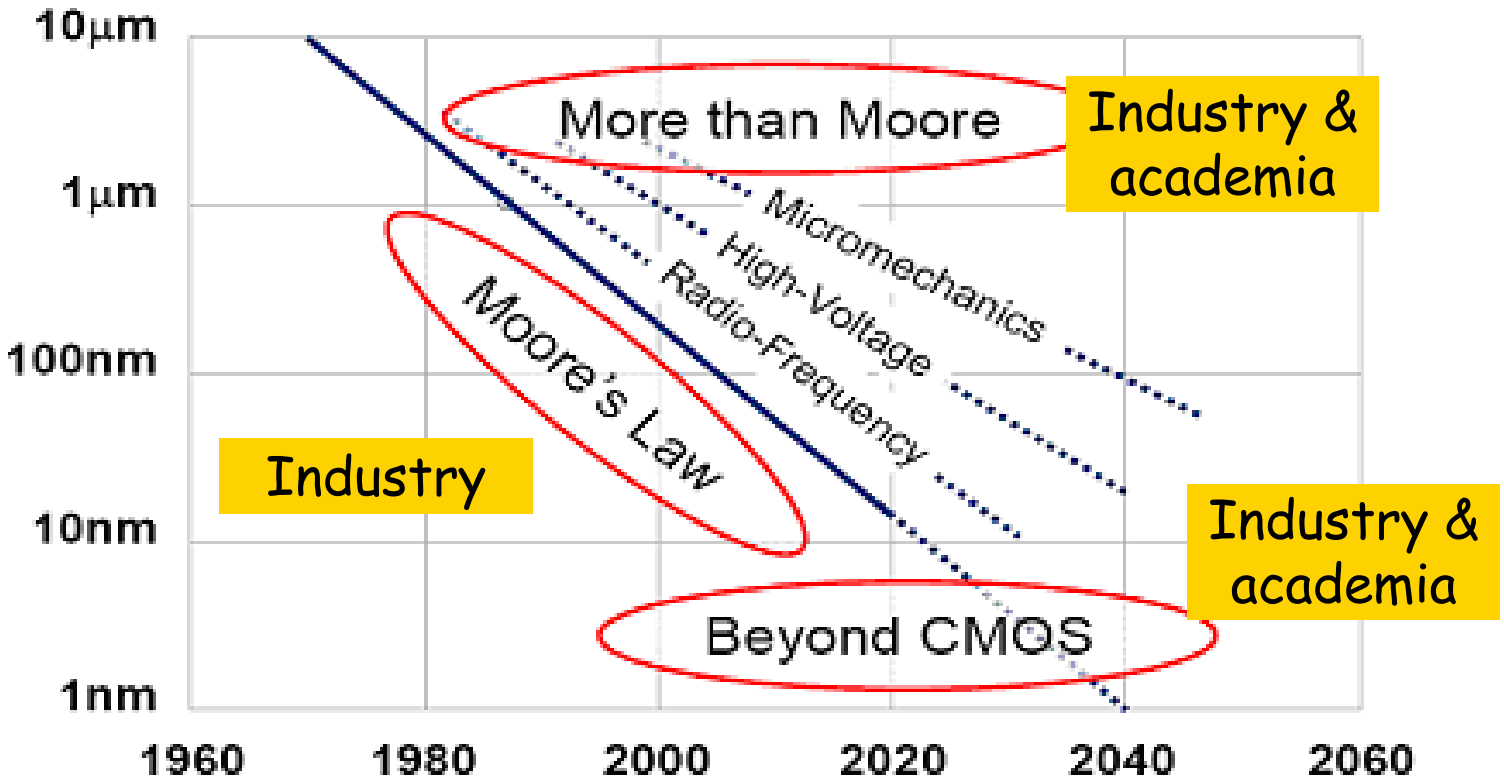
Repeated application of process steps

The More than Moore domain of microtechnology



The More than Moore domain of microtechnology

Source: ENIAC



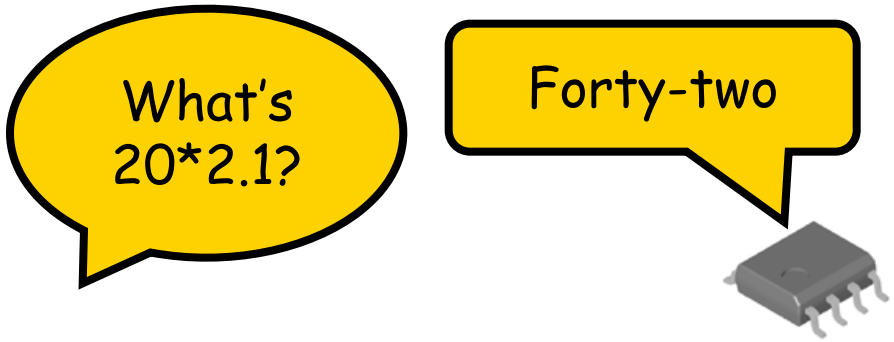
More than Moore: new functions

Traditional IC:

- Computing
- Data Storage
- Electrical Communication

Possible extensions:

- High quality passives
- Wireless communication
- Optical communication
- Sensing and Actuating

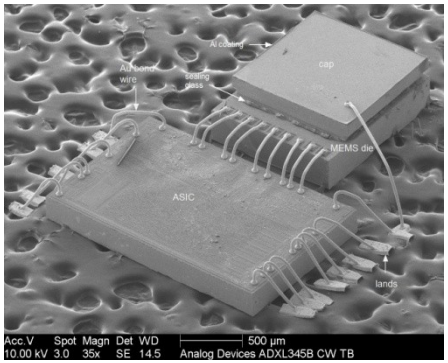


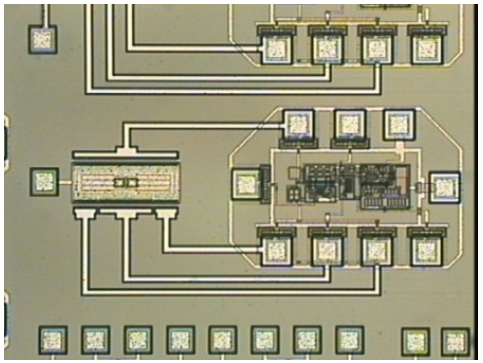
Integration: "ubiquitous computing" demands it microtechnology can deliver it

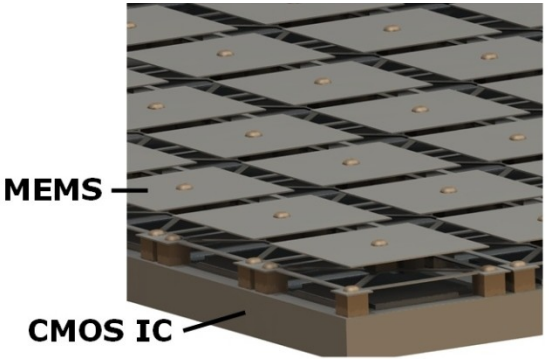
The fabrication challenge

How to combine electronics with sensors, actuators, optics, …?

- Hybrid (solder/bump the components together)
- Pre-CMOS: Make component, then make CMOS on the same wafer
- Intermediate: Mix the component and CMOS processes
- … or post-CMOS: add components on top of a finished CMOS chip



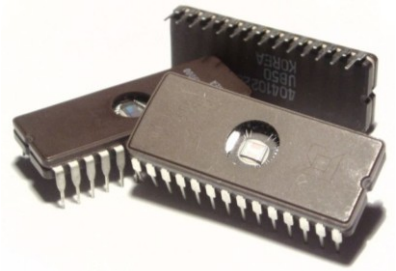


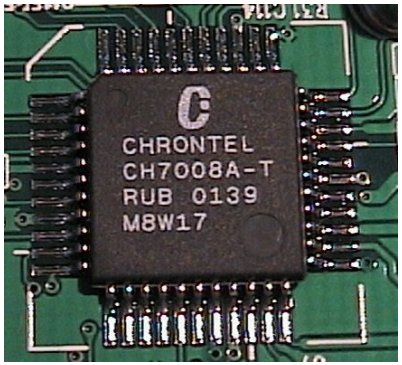


My definition of “a chip”

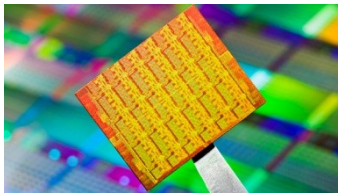
- Not this

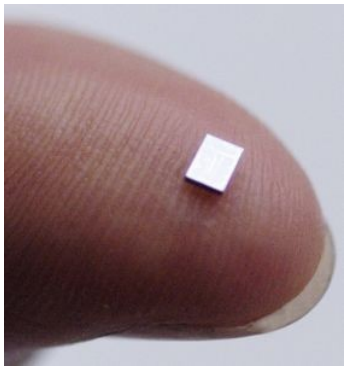
- Not even this





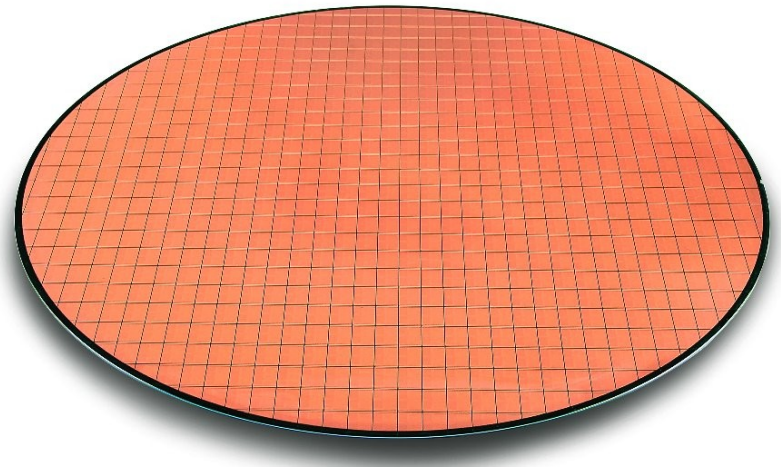
- But this





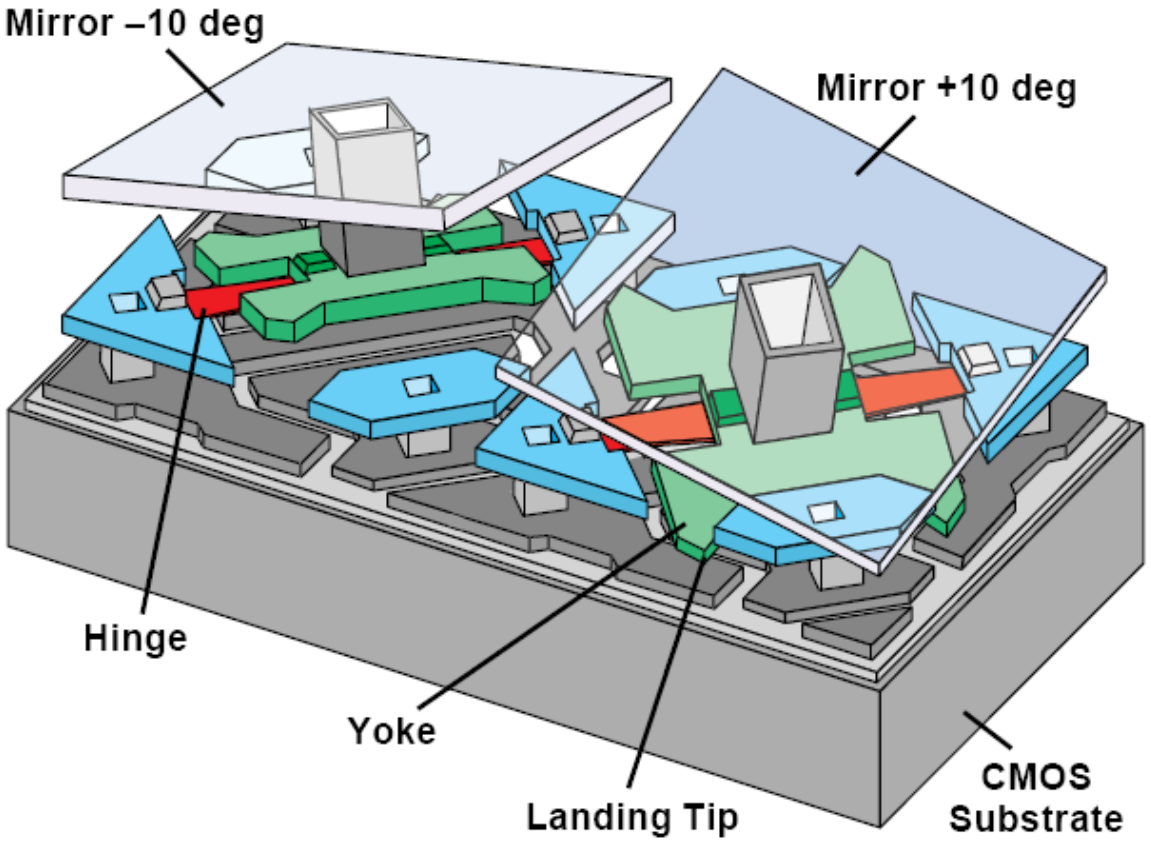
CMOS post-processing: “pizza technology”

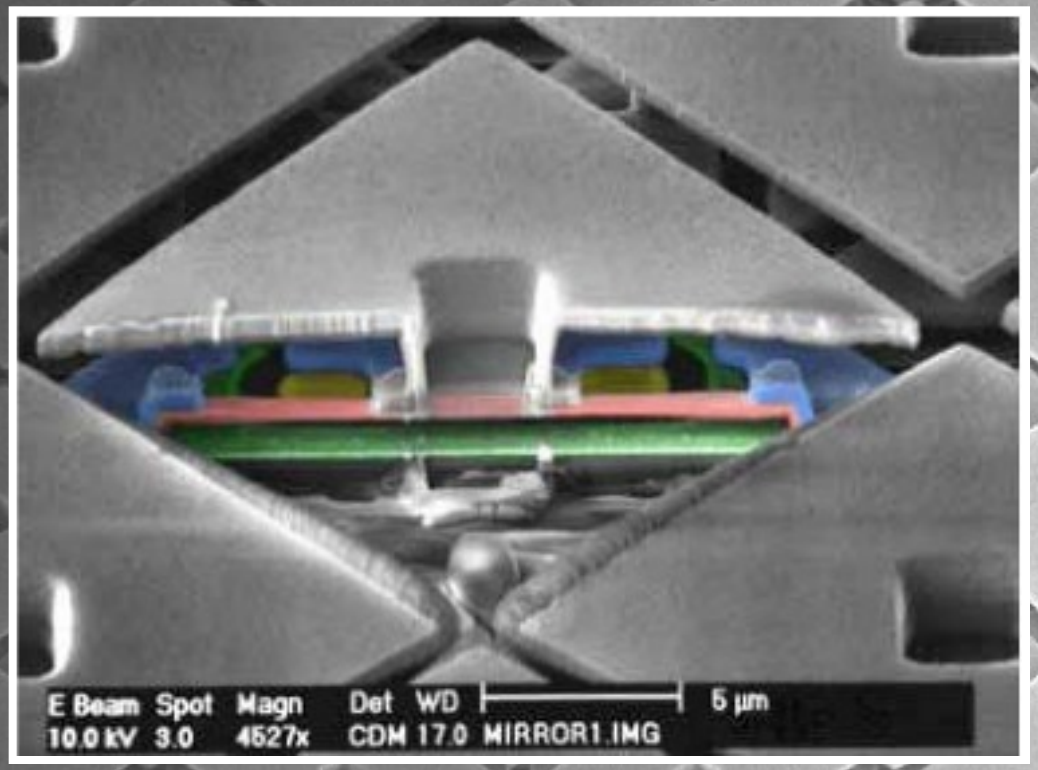
- Use CMOS wafers as a base
- Stack other things on top
- ... Creating a new microsystem with added functionality
- Also known as: Above-IC



Pizza #1: the Digital Micromirror

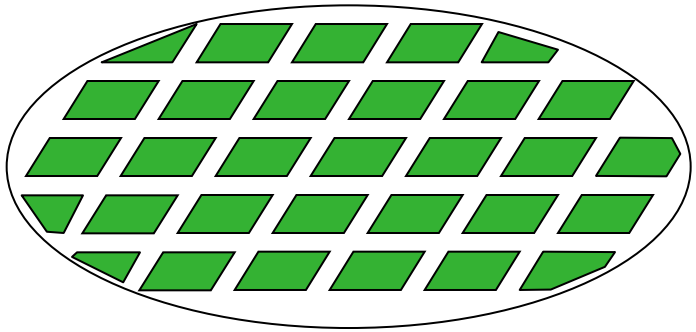
Digital Micromirror: Texas Instruments, 1980's
www.dlp.com



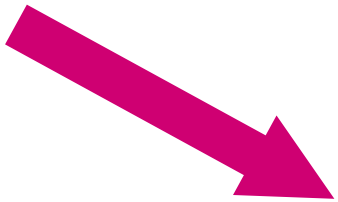


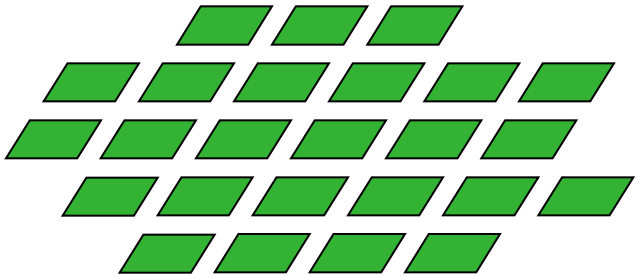
E Beam Spot Magn Det WD 20 µm
8.00 kV 3.0 2563x TLD 4.9 44003 00 04004

Wafer post-processing



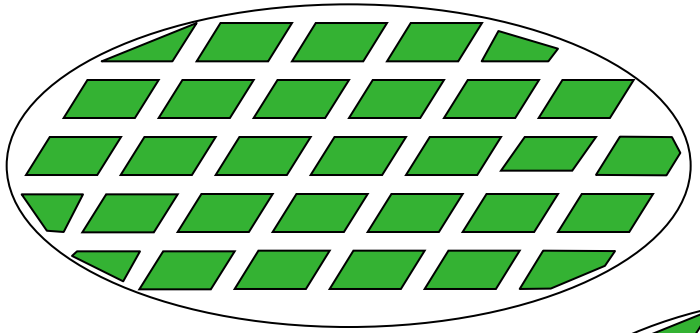
a. Chip fabrication



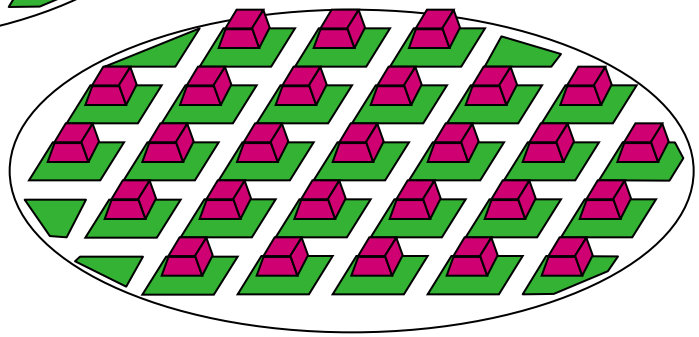


b. Wafer dicing

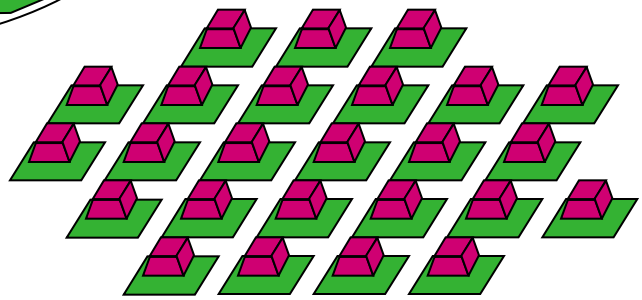
Wafer post-processing



a. Chip fabrication

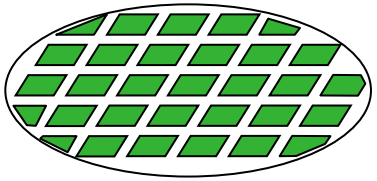


b. Post-processing

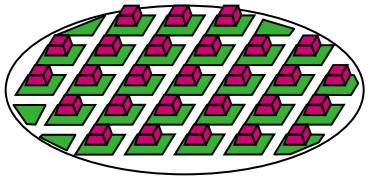


c. Wafer dicing

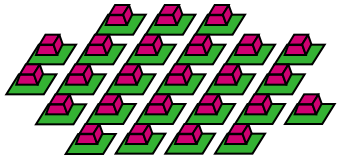
Logistics



a. Chip fabrication



b. Post-processing

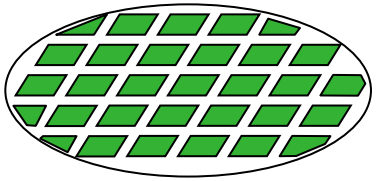


c. Wafer dicing

- Chip fabrication: standard, at any regular (CMOS) fab

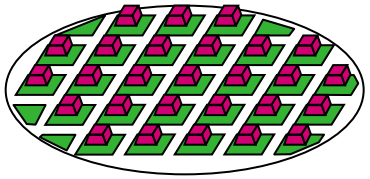
- Wafer dicing, packaging: specialized work like MEMS packaging, e.g. Amkor, Boschman

Pros and cons



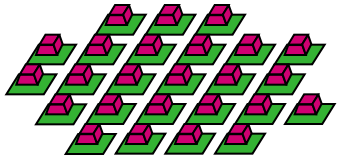
a. Chip fabrication

- We do not interfere with the (CMOS) fabrication process
- We can buy good quality chips



b. Post-processing

- We can use any lab for this
- Excellent alignment and galvanic contacts
- We must keep the CMOS intact



c. Wafer dicing

- We have to think the final stages through very carefully! (Standard solutions may fail)

CMOS post-processing: game rules

Careful treatment of the underlying CMOS:

- Temperature ≤ 450 C
- Mild (or no) plasmas
- Maintain the H balance in the MOSFET
- Limited mechanical stress

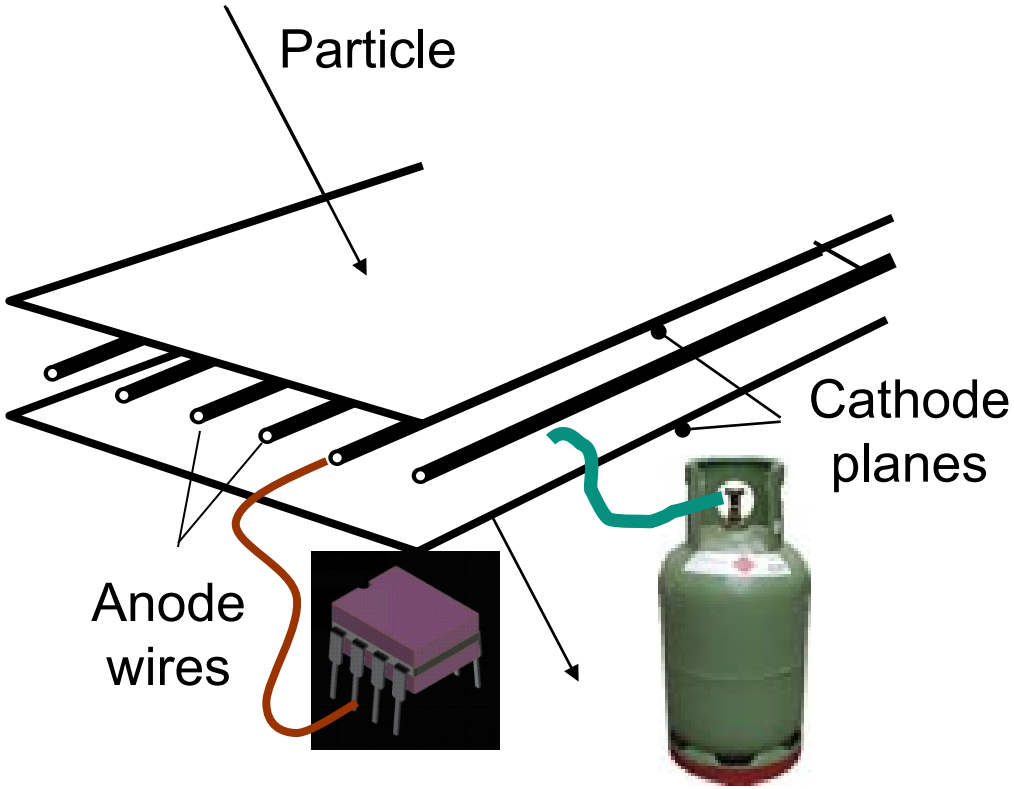
Choose your materials for good adhesion and durability

The CMOS properties must remain unchanged:
only then the standard infrastructure can be used.

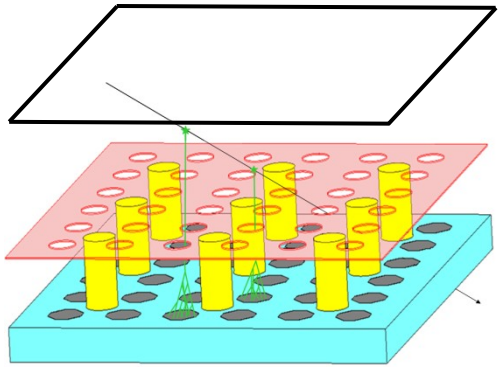
Further reading:
Jurriaan Schmitz, Nucl. Instr. Meth. A 576 (2007) 142.

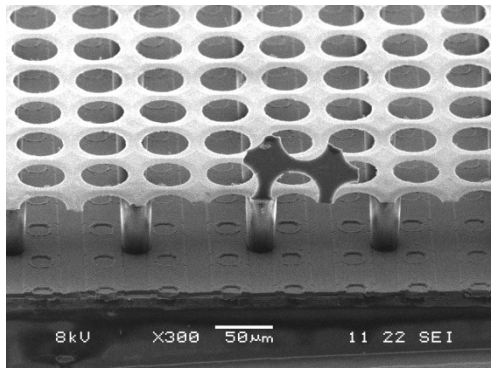
Pizza-based radiation imaging

Traditional MWPC



InGrid

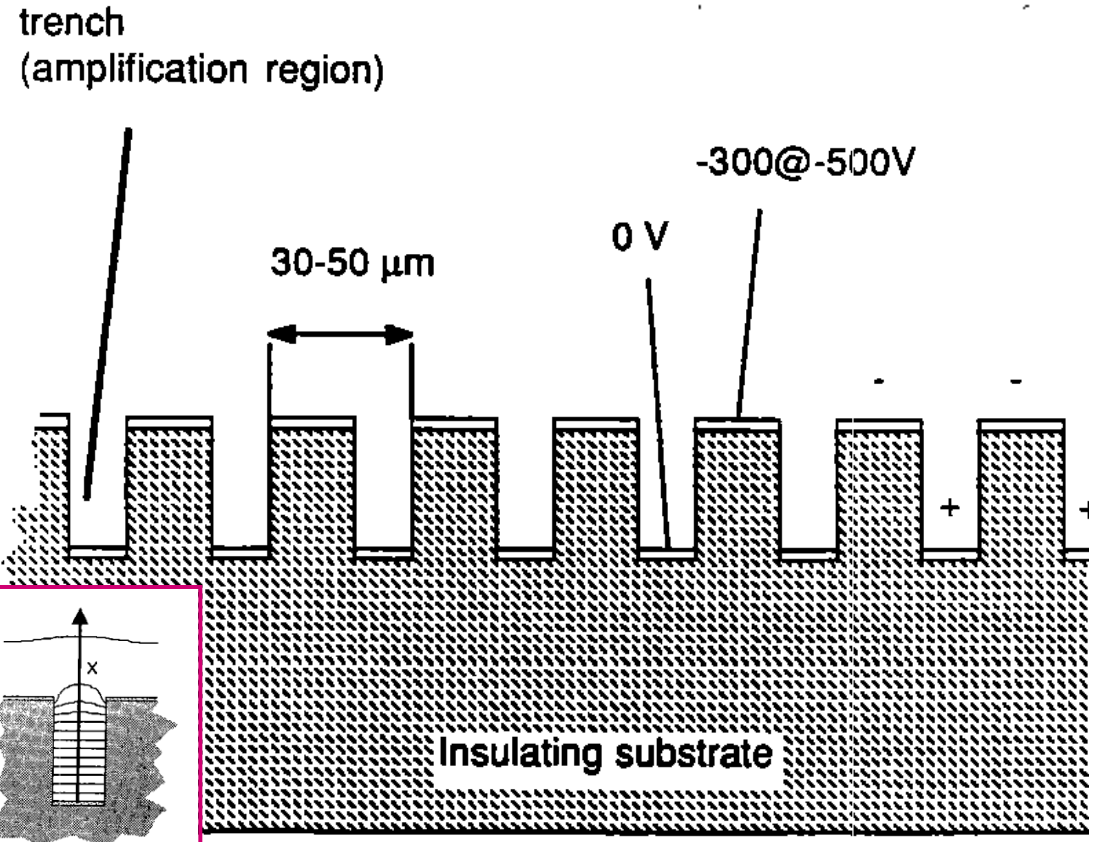




Based on an old idea…

NIKHEF-H/91-14

July 1991



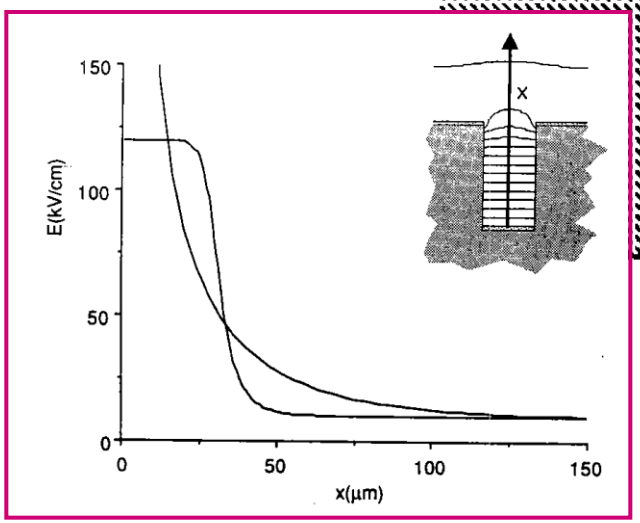
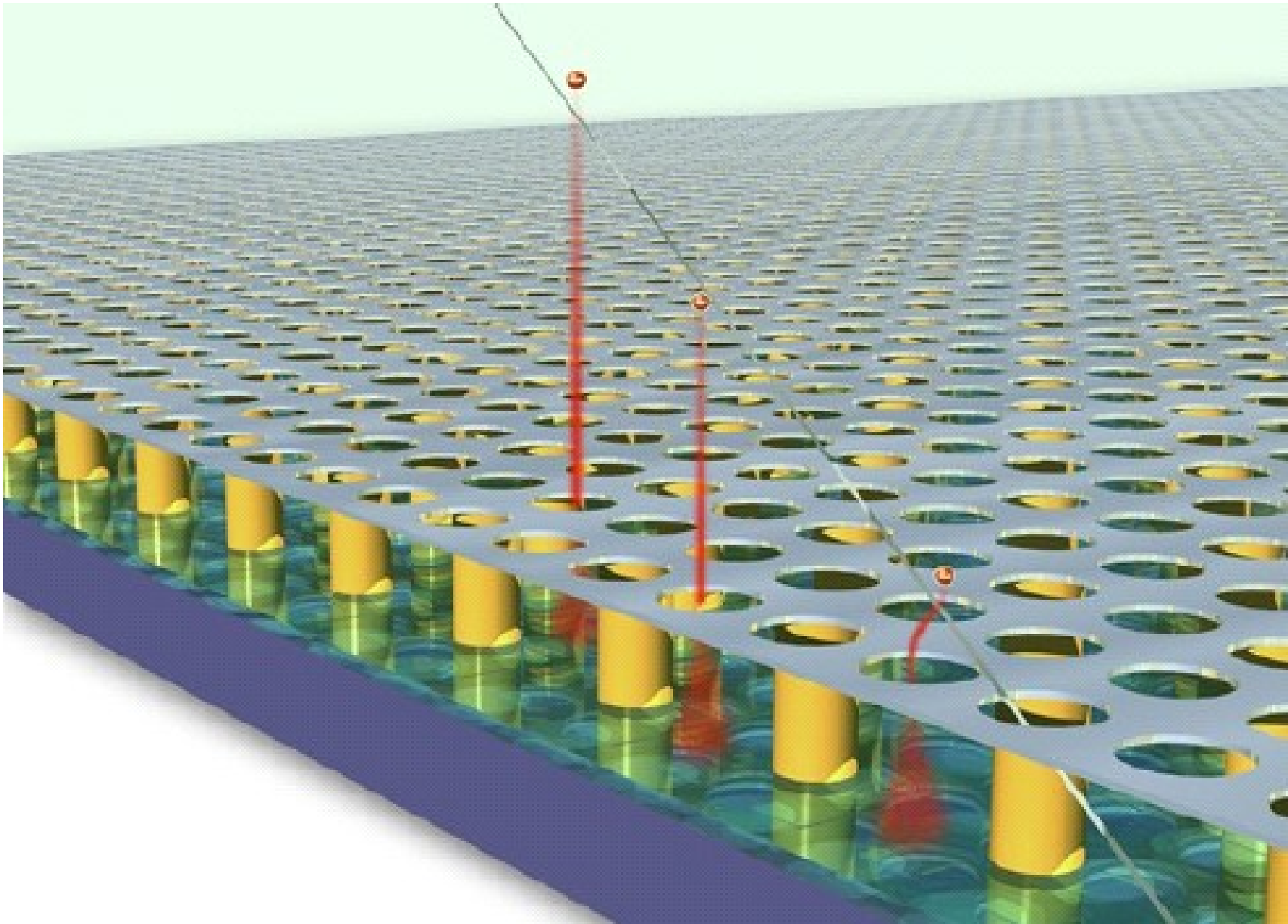
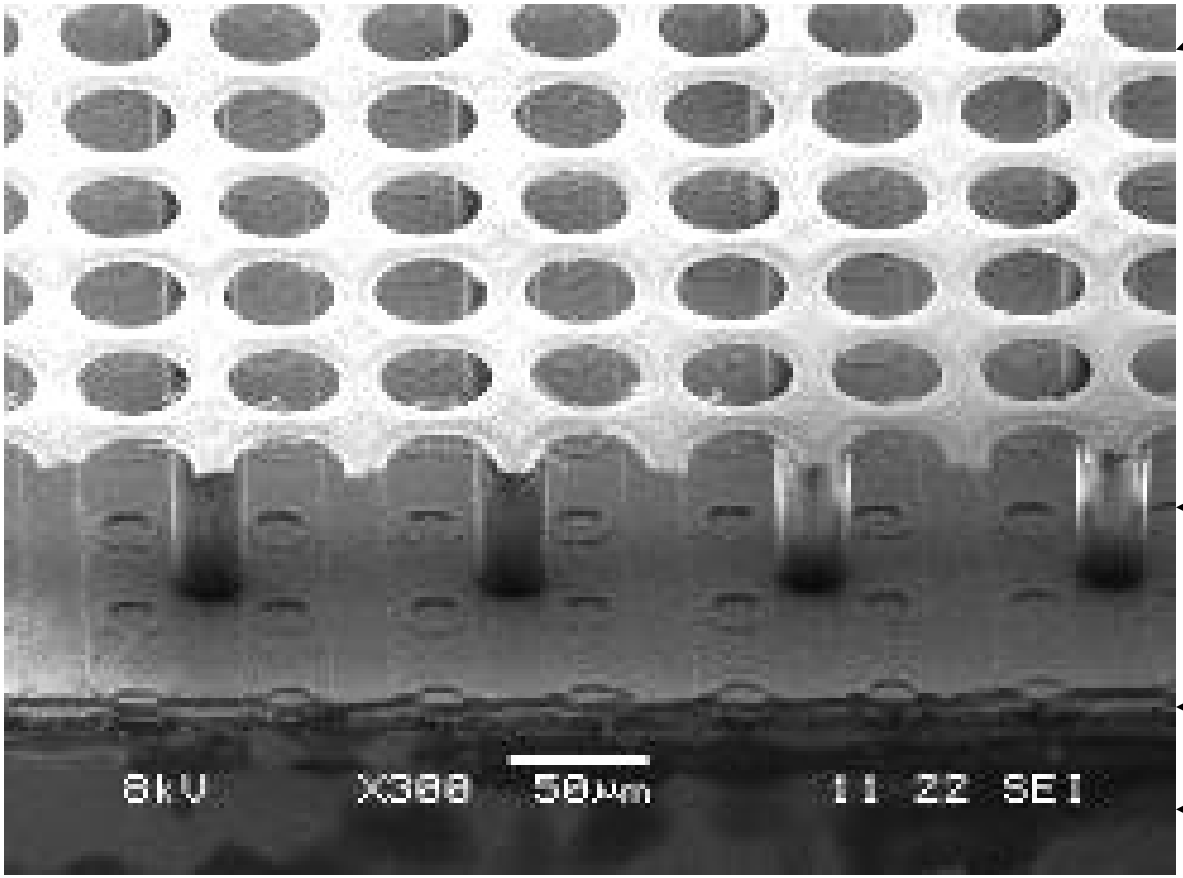


fig. 2: layout of a Micro Trench Gas Counter.

InGrid: a radiation imaging detector



Choice of materials



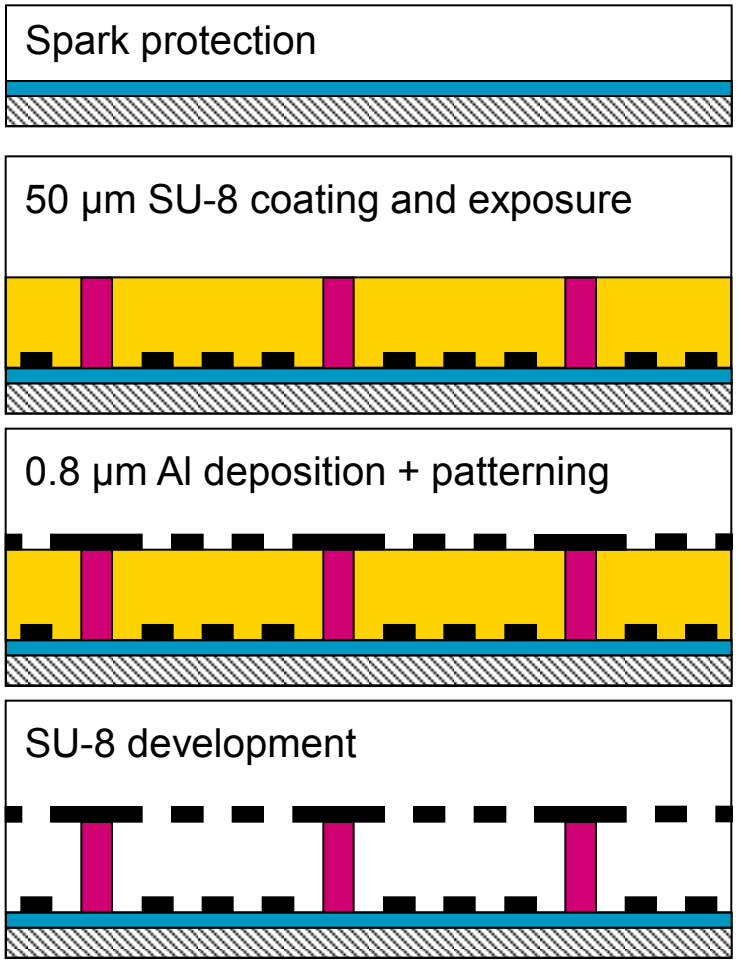
Al membrane
(-400-450 V)

SU-8 pillar
(50 µm high)

a-Si protection

Readout chip:
Medipix2,
Timepix, …

Process flow – suspended membrane

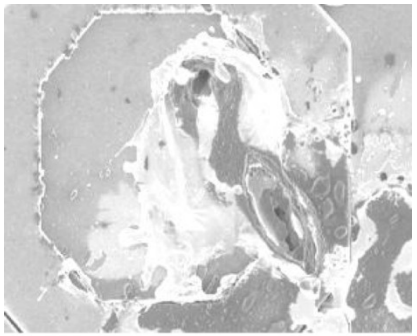


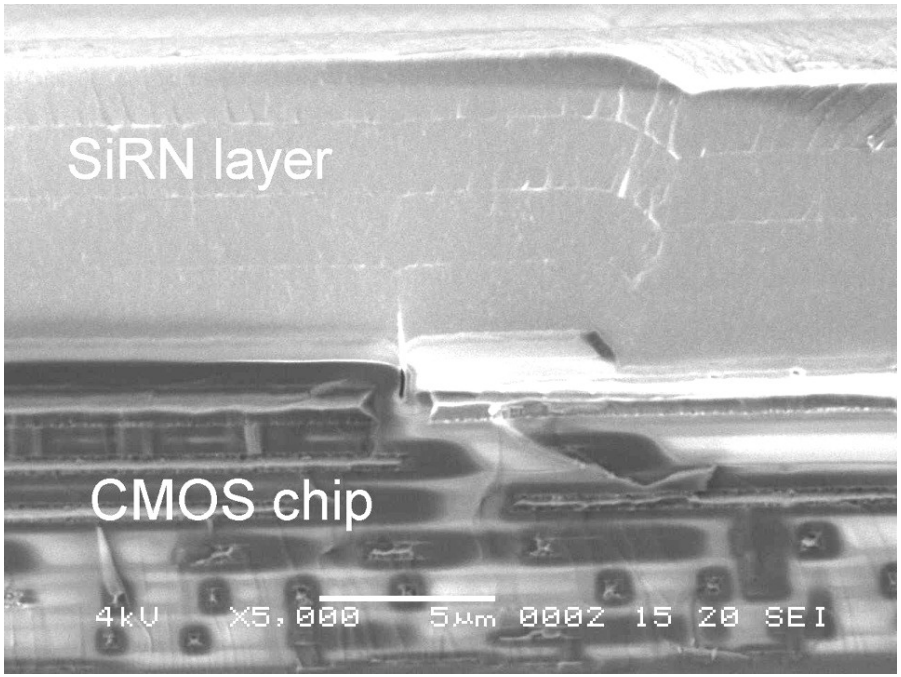
- Deposit spark protection film: a-Si or Silicon-rich nitride
- SU-8 photoresist for pillars
- Al deposition is critical: unexposed SU-8 (yellow) should not crosslink
- Al patterning also critical: lithography at room temperature to protect SU-8
- Membrane release at end, after wafer dicing (fragility)

Silicon-rich nitride: anti-spark material

- Sparks cause permanent damage
- Originally a-Si:H, now Si-rich Nitride
- Si_3N_4 typical anti-scratch layer on CMOS
- SiRN, excess of Si to tune resistivity and mechanical stress
- Deposited by PECVD at 300 °C or lower

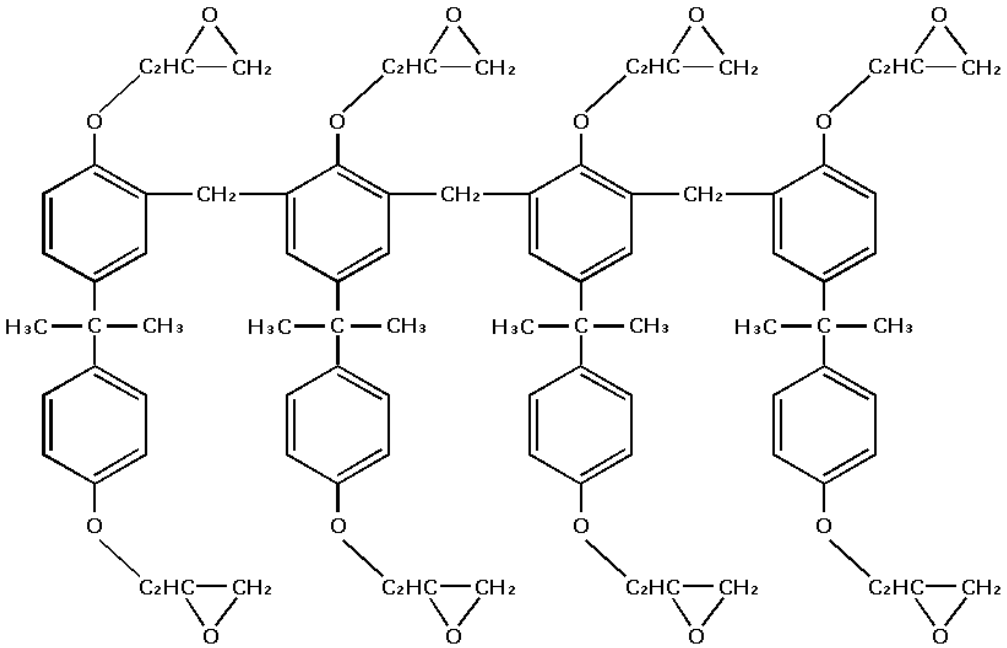
NIM-A, in press



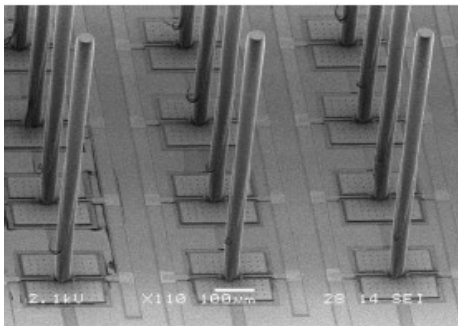


SU-8 material

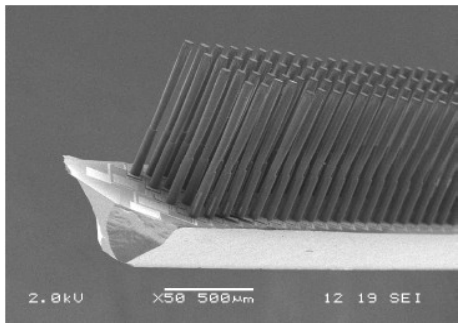
- Negative tone photoresist (developed by IBM Research)
- Polymer based (EPON SU-8 from Shell Chemical)
- Available in many viscosities
- Thickness ranges from 1 to 1000 µm
- Processing similar to normal UV lithography



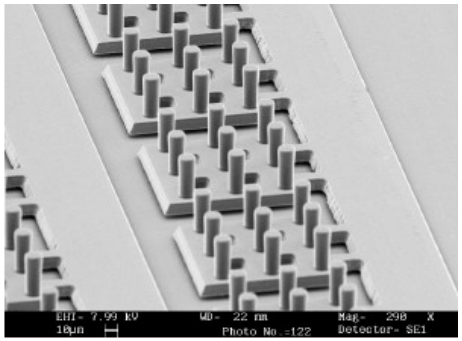
Examples of SU-8 use



Krijnen *et al.*, MESA+, UT



Krijnen *et al.*, MESA+, UT

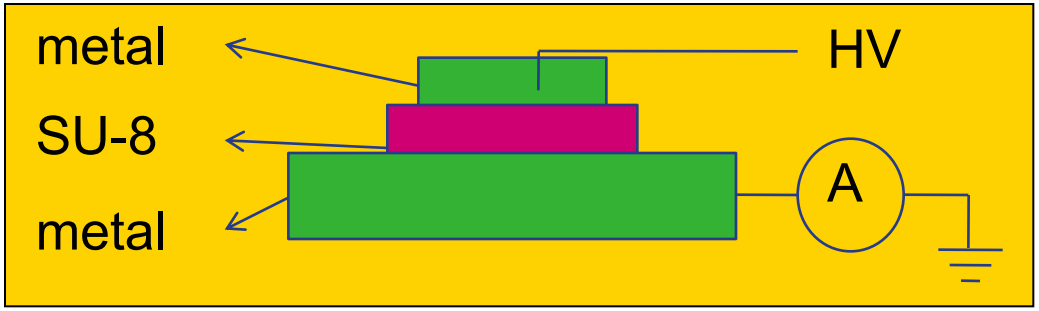


Conradie *et al.*, Cambridge

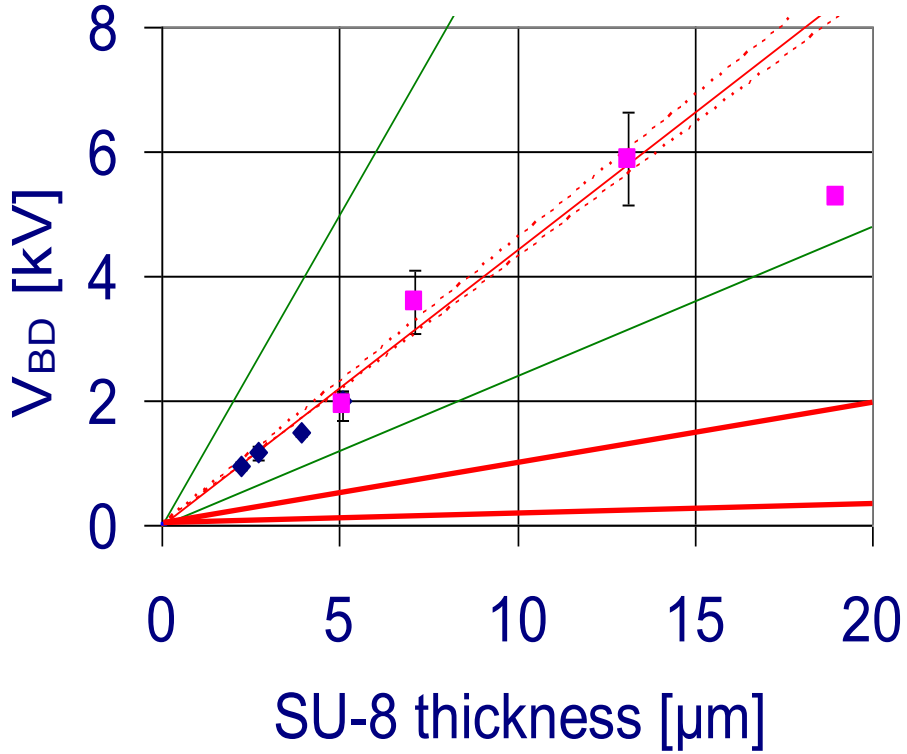
Also applicable in proportional chambers?

- Radiation hardness: Key, Cindro, Lozano 2004
- Dielectric strength?
- Outgassing?

Dielectric strength of SU-8



SiO_2:
0.8–1 kV/μm



SU-8: 443 16 V/μm

Kapton-N: 270 V/μm

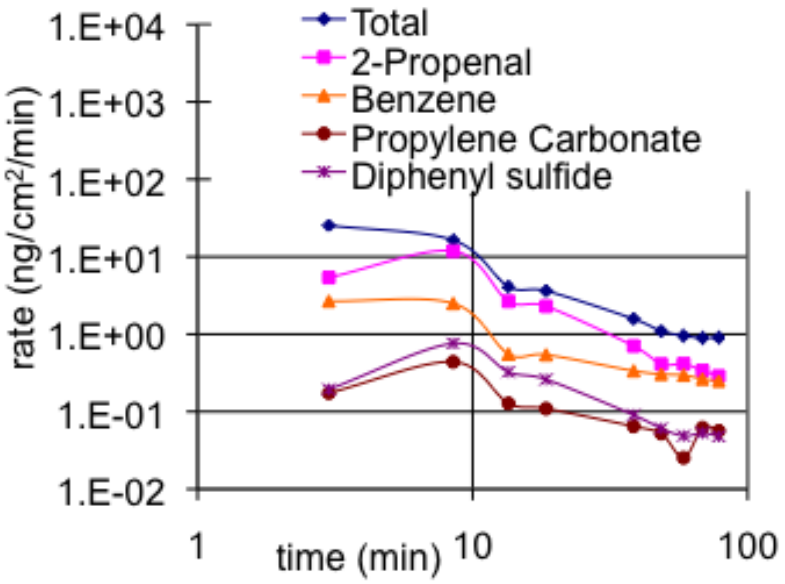
MCP: ≤ 100 V/μm

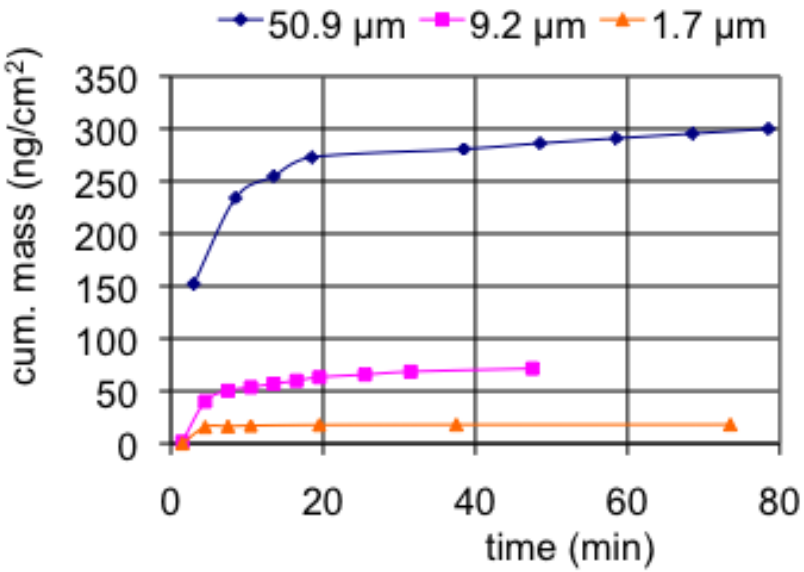
MPGD: ≤ 10–20 V/μm

J. Melai et al.,
J. Micromech. Microeng. 19 (2009) 065012

Outgassing from SU-8

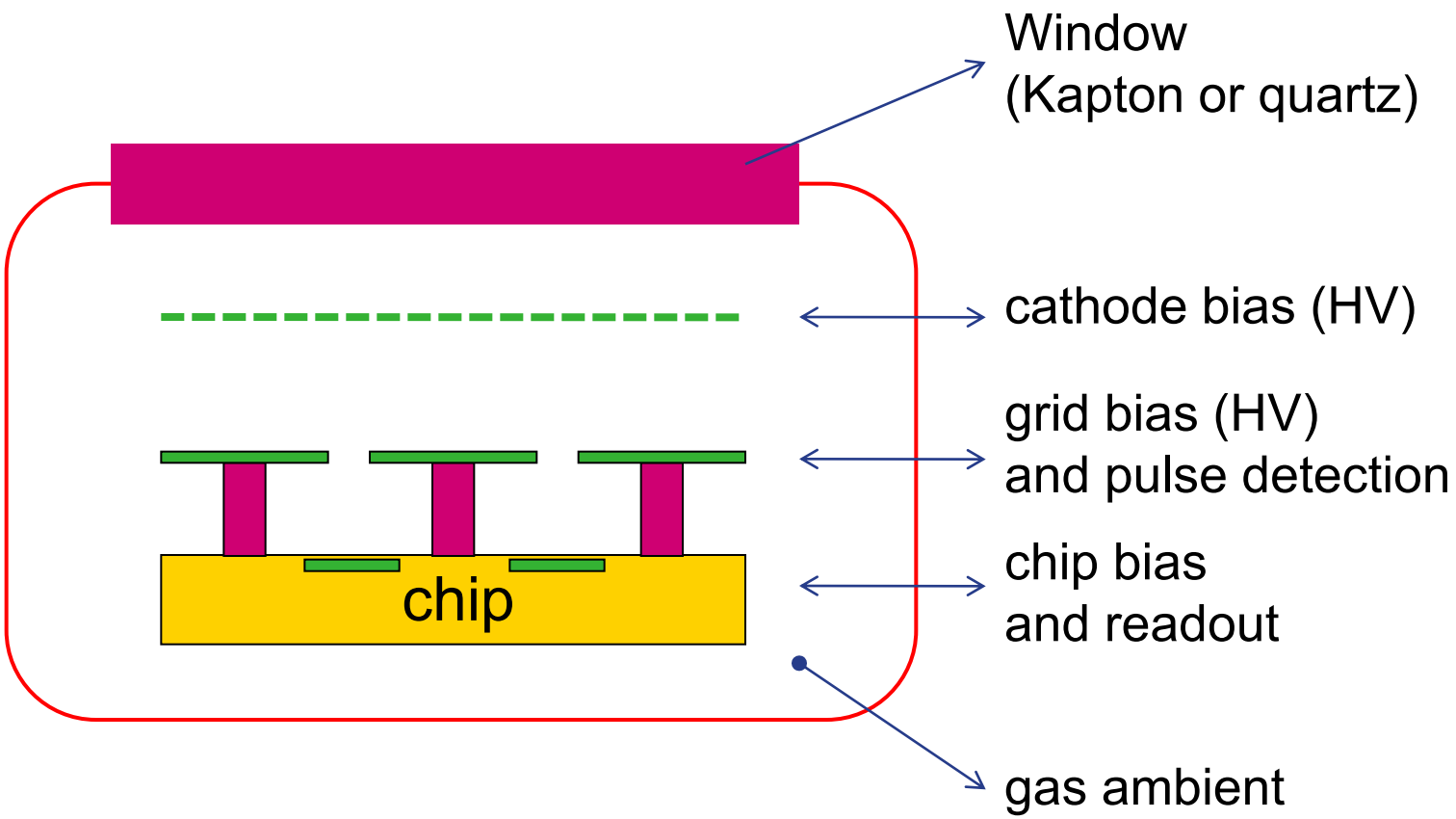
- Outgassing rate comparable to Kapton
- 20–30 min Hard-Bake → efficient pre-conditioning
- Components directly linked to resist formulation





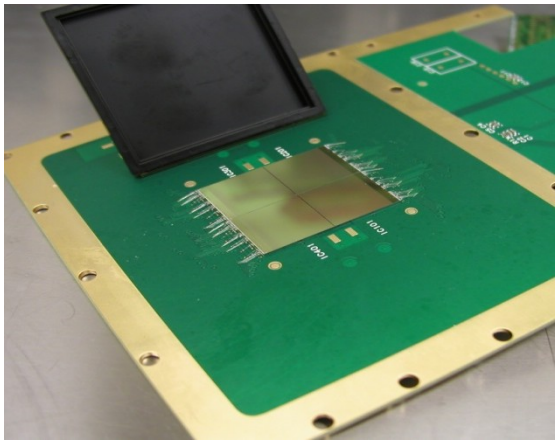
J. Melai et al.,
Microelectronic Engineering 86 (2009) 761–764

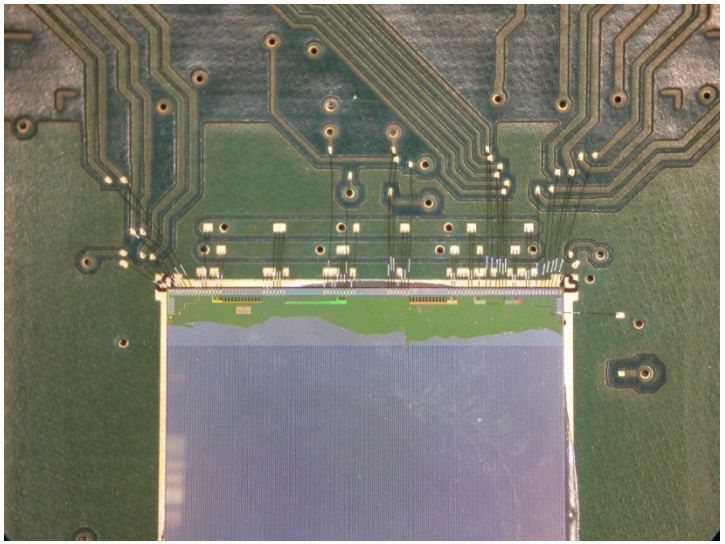
Testing of the InGrid chips

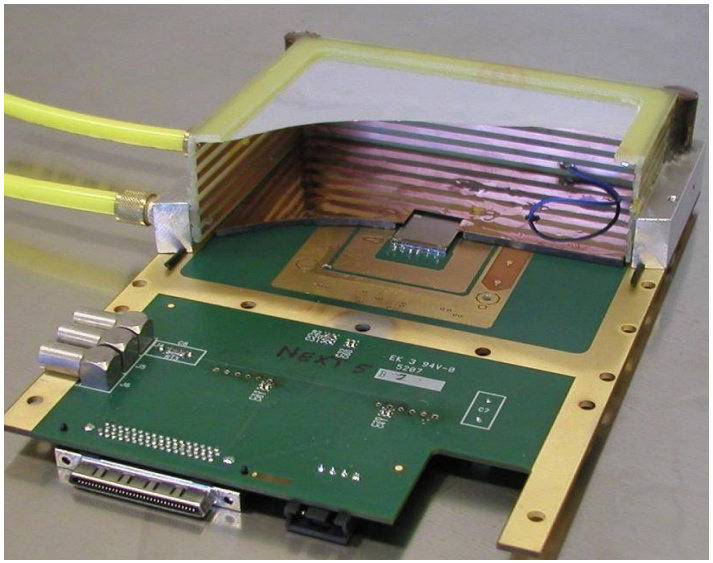


Chip bonding

- Finish post-processing
- Attach chip (w/ InGrid) to board
- Wirebonding of connections
- Mount chamber onto board

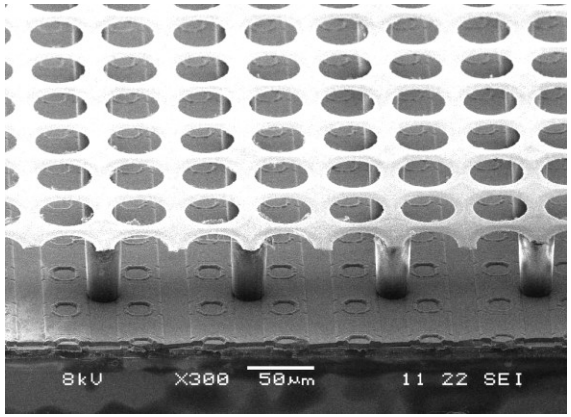


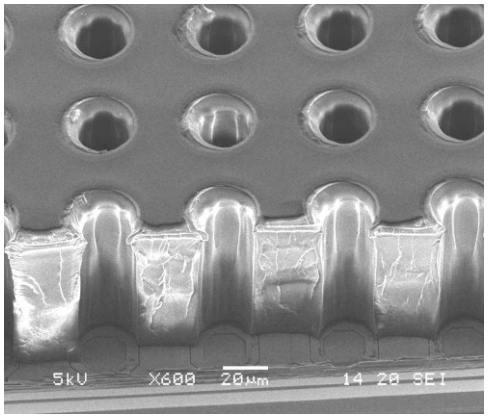


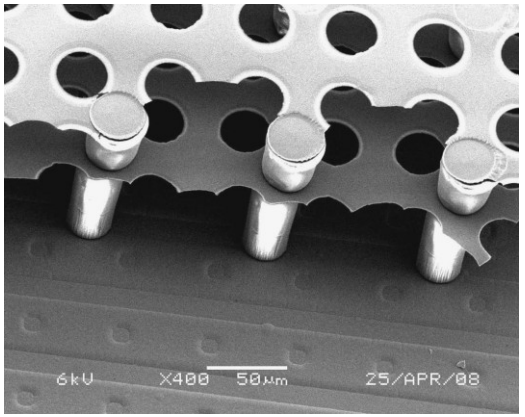


InGrid performance

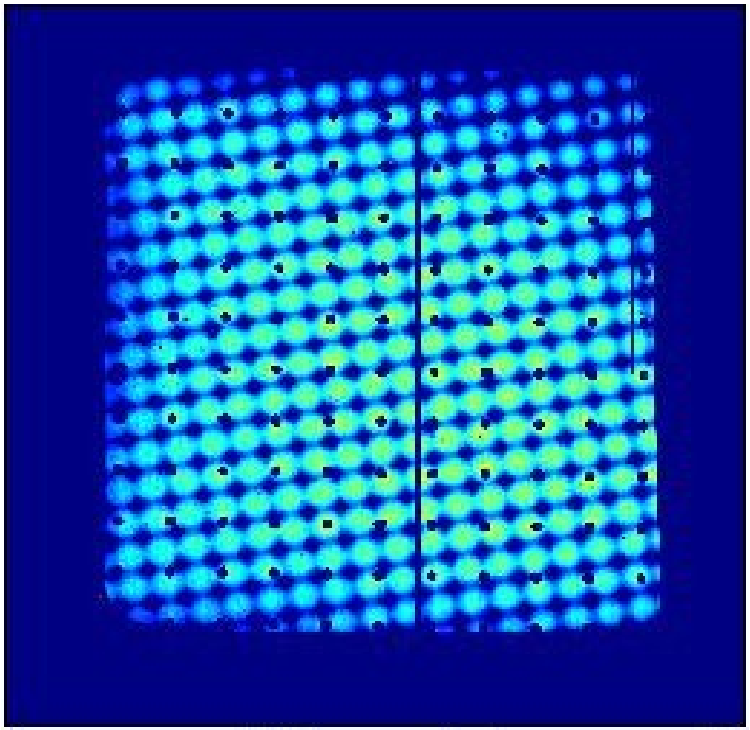
- High single e^- collection efficiency (> 90% at 10^4 gain)
- Good energy resolution (11.7% FWHM for ^{55}Fe in Ar/CH_4)
- 2D and 3D tracking of MIPs etc – 20 µm position resolution!
- Various device designs:
  Micromegas, GEM, multiple electrodes



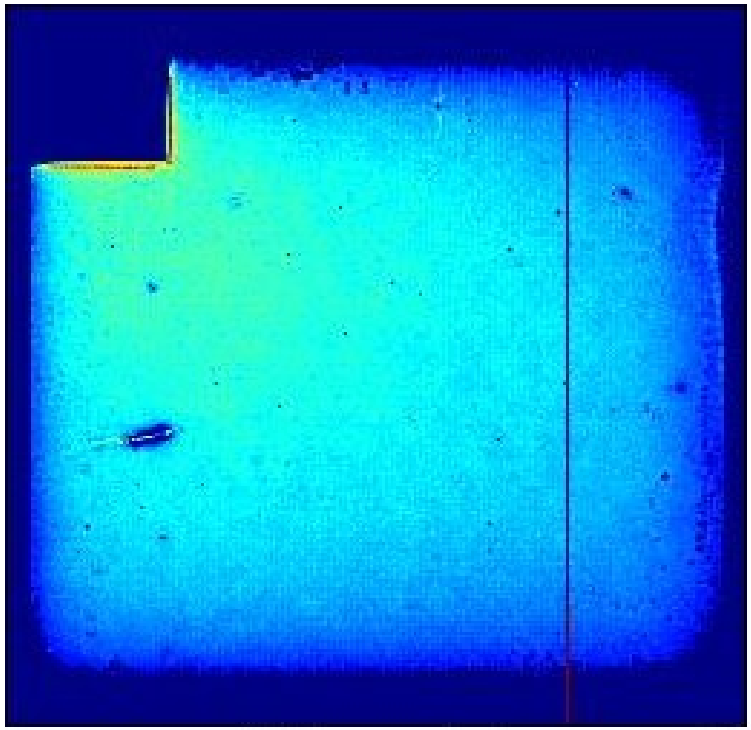




Homogeneous response



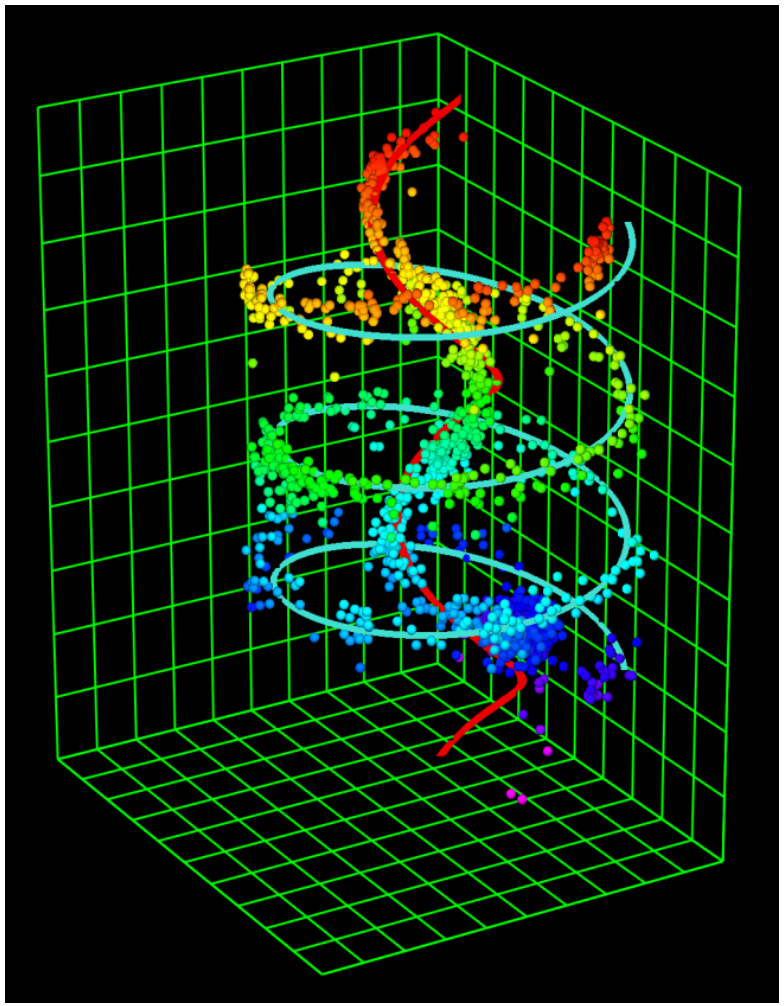
Seperately mounted Micromegas



Post-processed InGrid

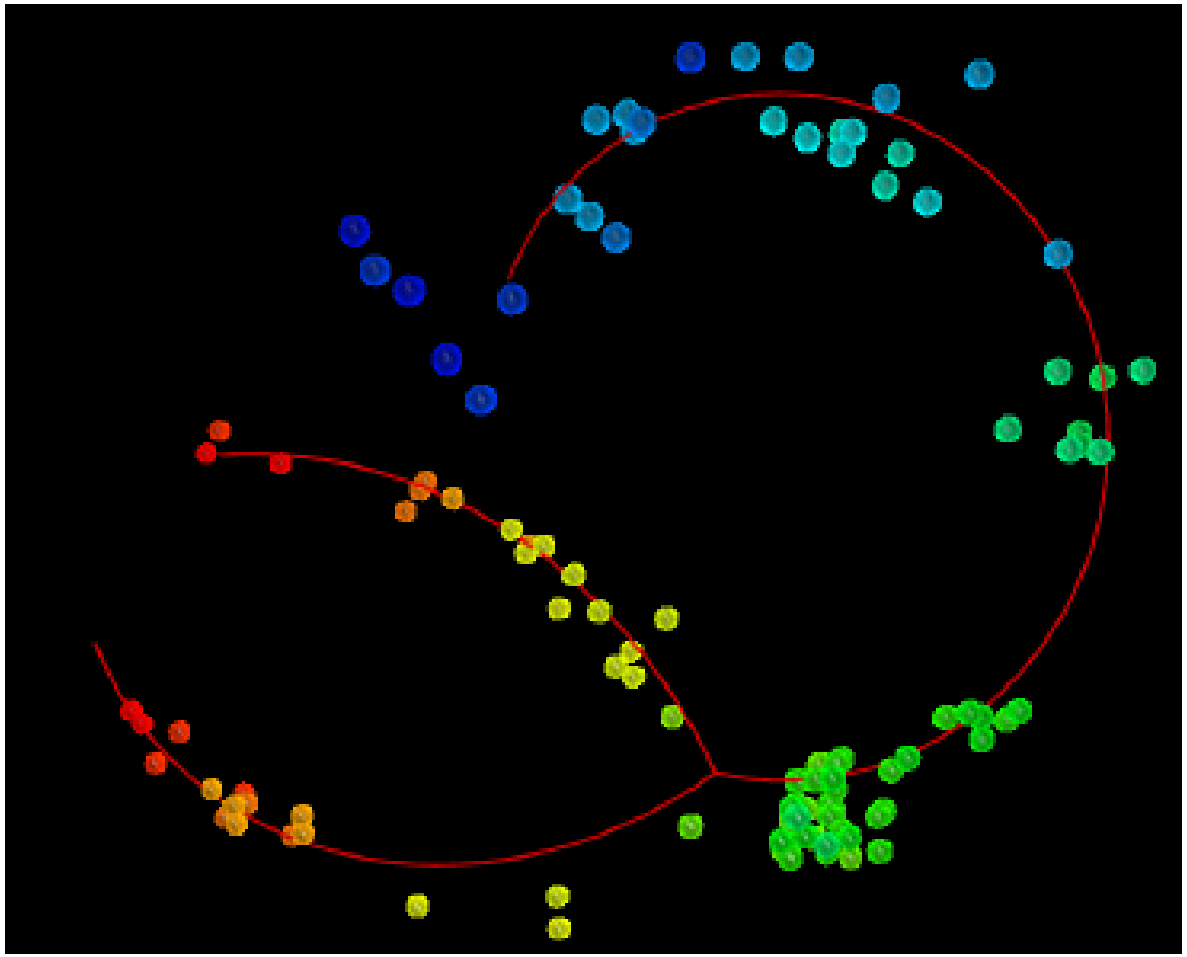
Microlithography → alignment tolerance (few μm)
→ alignment between pixels and grid (55 μm pitch)
→ no more Moiré patterns

^{90}Sr tracks recorded with a 3 cm Timepix TPC



Courtesy: Martin Fransen and Lucie de Nooij, NIKHEF

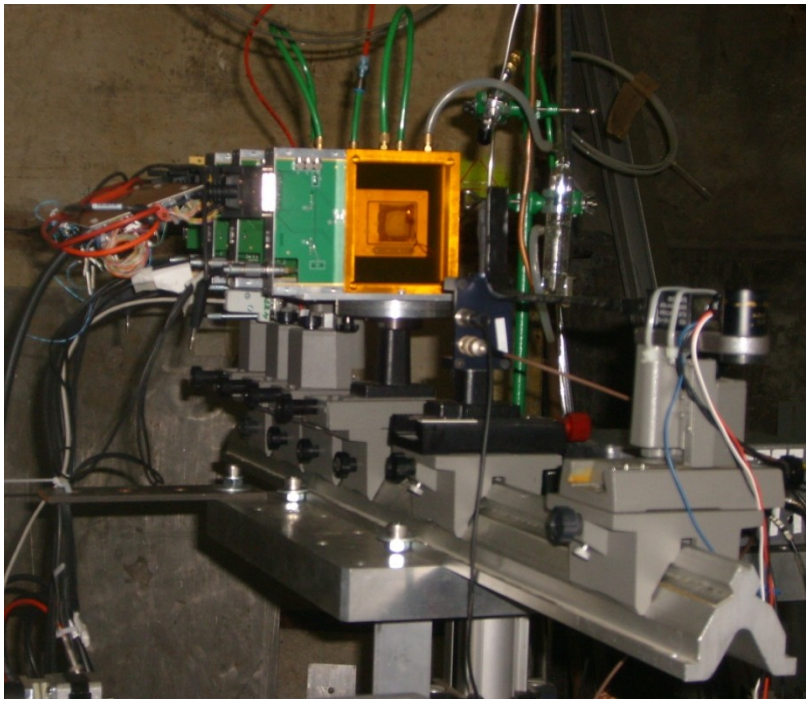
^{24}Na decay



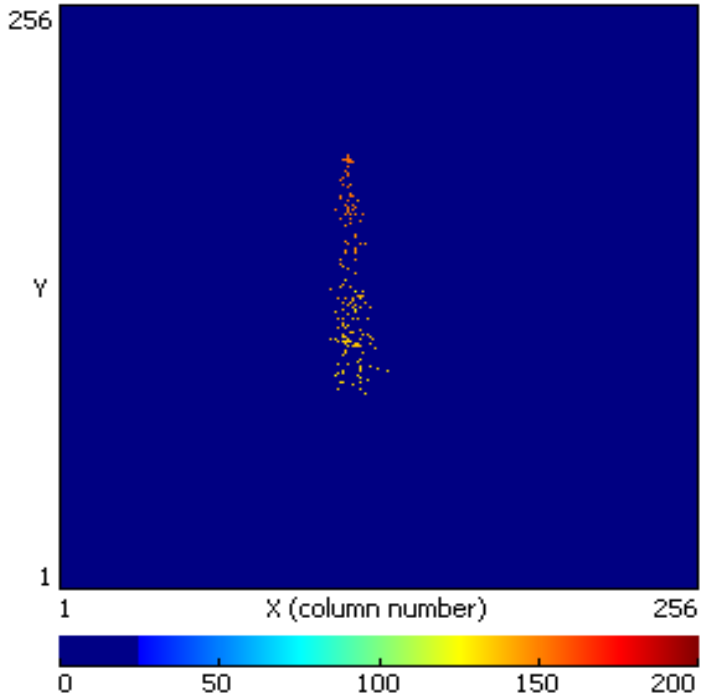
Courtesy: Harry van der Graaf, NIKHEF

Beam tests – preliminary findings

Several PS beams at CERN
Ar/Iso 80/20 and DME/CO_2 50/50

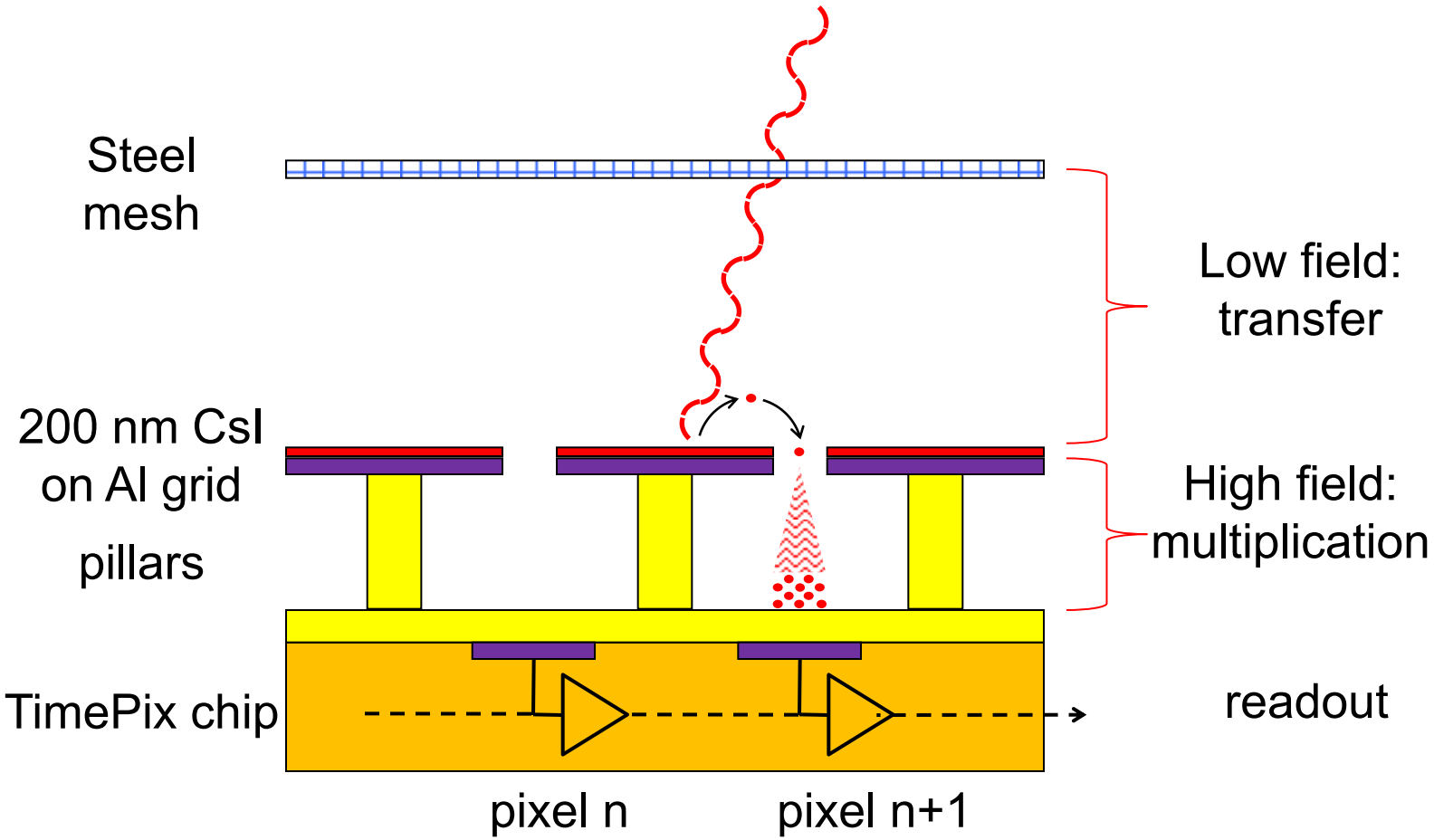


Few-GeV e^- at DESY
11.5 mm high TPC, Ar/Iso 80/20

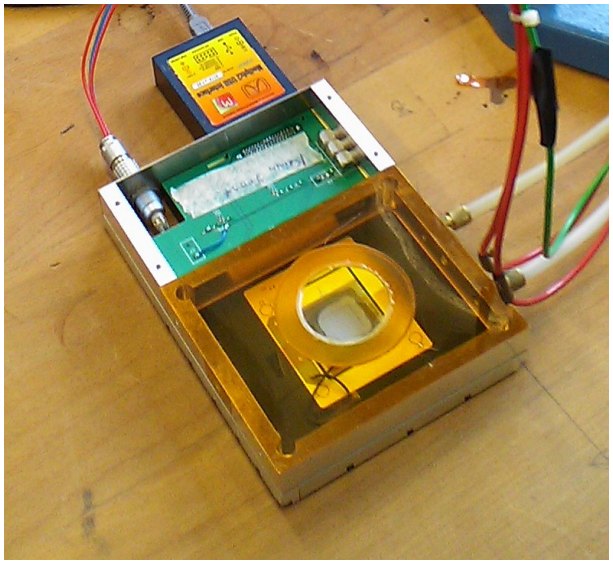


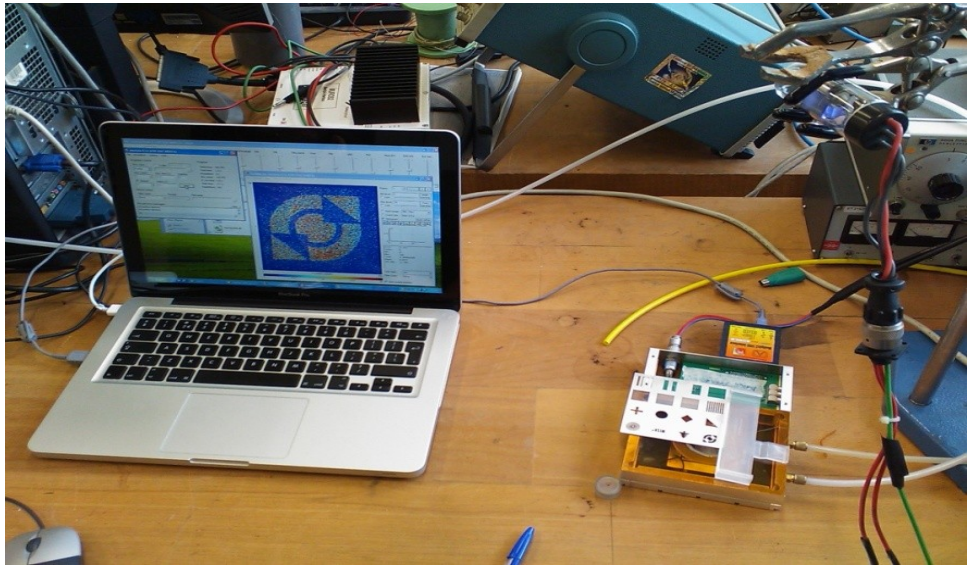
Position resolution better than 20 μm in XY plane
Decent operation, but sudden deaths observed

Making InGrid single-photon sensitive



Set-up for photon detection

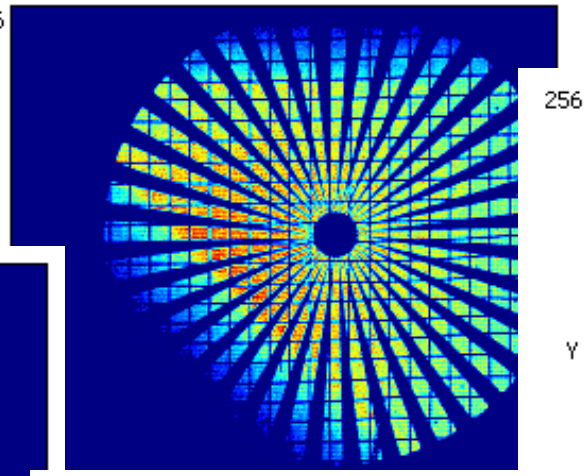




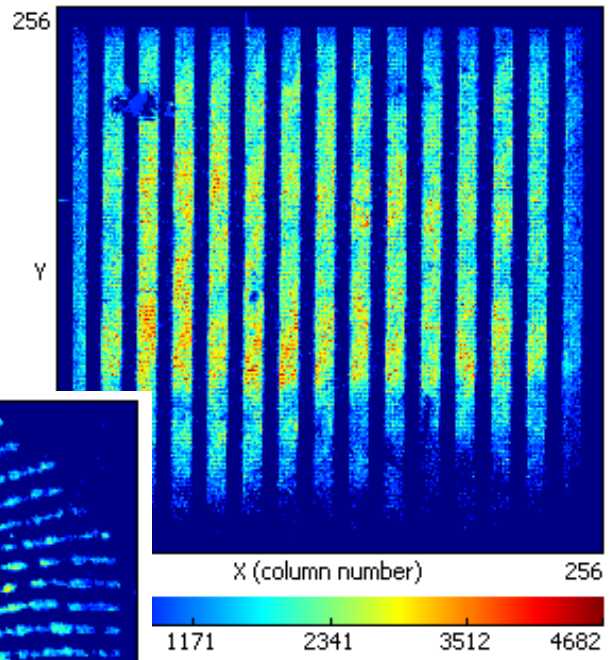
- Typical InGrid on a Timepix chip
- GOSSIP/NEXT chamber (Nikhef), USB readout
- Thermal evaporation of CsI (Weizmann)
- Tested using UV source, filters, shadow mask

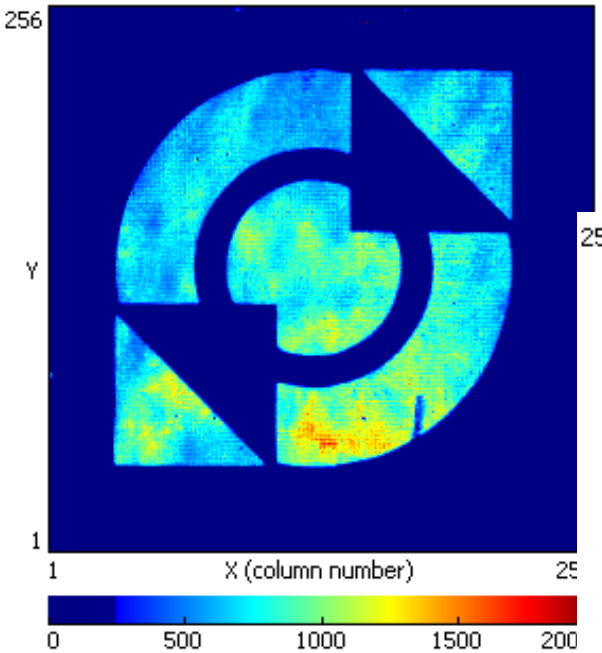
InGrid images under UV irradiation

Siemens star

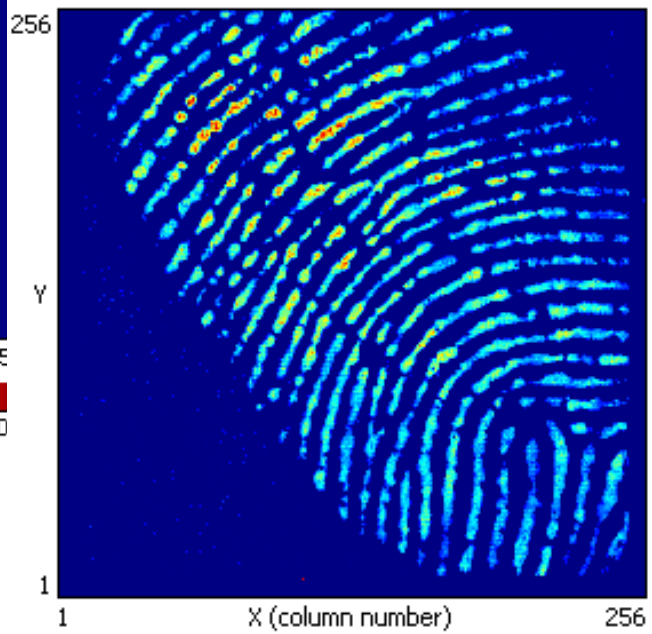


Vertical stripes





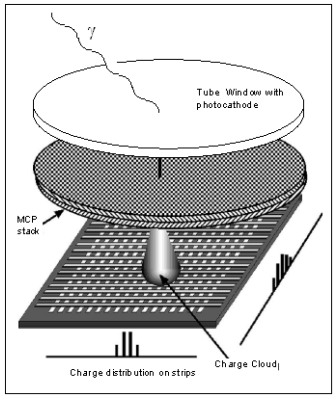
University of Twente Logo



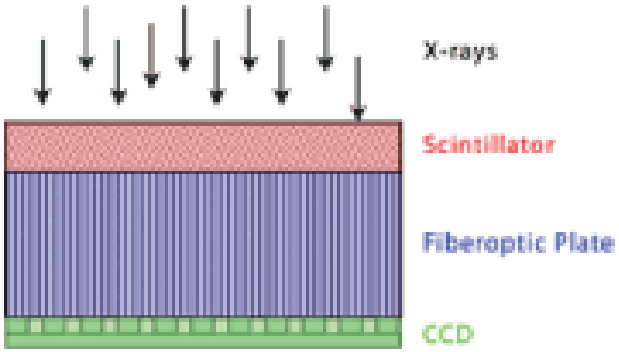
Fingerprint on window

Other tastes of Pizza

- Semiconductors on a chip
  - Amorphous silicon: shown (e.g. Wyrsch et al.)
  - Polycrystalline silicon: first steps made
  - CIGS: rad-hard!!
- Integrate an MCP?
- Grow a scintillator on an APS sensor?



Vallerga et al.
Melai et al.



SigmaDigitalXray

Outlook

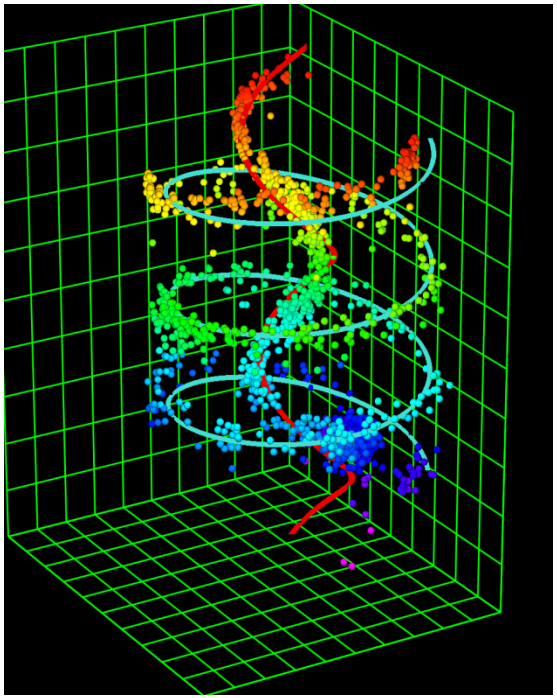
Pizza technology can supply:

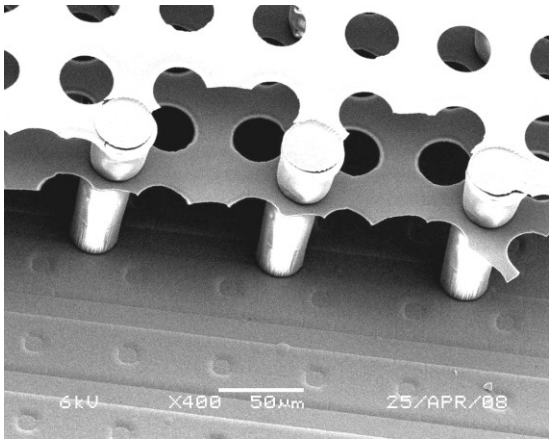
- Faster
- More accurate
- Lower-mass
- Cheaper-per-channel

gaseous radiation imaging detectors

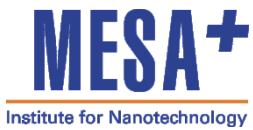
But further work is required!!

- Upscaling to dm^2 – m^2 areas
- Ultimate resolution
- Radiation / ageing tests
- ASIC design





Thanks…



My low-temperature coworkers:

- Members of my group
- Yevgen Bilevych, Marten Bosma, Max Chefdeville, Harry van der Graaf, Martin Fransen, Jan Visschers, Jan Timmermans at Nikhef
- GridPix friends: Bonn, Saclay, SMC, IZM

Our sponsors:

- The Dutch Technology Foundation STW; FOM
- The Dutch Ministry of Economic Affairs
- NXP Research

- …and the Medipix consortium

Further reading

Pizza technology:

- J. Schmitz, Adding functionality to microchips by wafer post-processing, Nucl. Instr. And Meth. A 576 (2007) pp. 142–149.
- J. Schmitz, The InGrid chip post-processing technology for radiation imaging, Proc. Of Science 2010 (available online).

InGrid radiation imager:

- V. M. Blanco Carballo et al.,
  IEEE Electron Device Letters 29 (6) pp. 585-588 (2008).
- J. Melai et al., accepted for Nucl. Instr. Meth. A. 2010.