ABSTRACT:
With the successful start up of the LHC the experiments are already planning the upgrades which are necessary to maintain and enhance the physics output over the next decade and beyond. At the LHCb experiment there is an opportunity to massively increase the data taking capabilities, independently of the planned LHC luminosity increases, by modifying the electronics architecture to be able to readout the entire detector at 40 MHz and perform all trigger algorithms in software. One of the implications of this scheme is the need to completely replace the silicon vertex detector of LHCb, or VELO. For this a new readout ASIC is being developed, dubbed VELOPix, which is based on the Timepix/Medipix family of chips. This seminar introduces the LHC upgrade landscape and the motivation for the LHCb upgrade, and describes the R&D steps which are currently in place to develop the new chip and the associated upgraded pixel vertex detector. The installation of the LHCb upgrade is planned for the long LHC shut down in 2017/2018, and the LHCb Upgrade LOI has been recently presented to the LHCC and can be viewed at https://indico.cern.ch/conferenceDisplay.py?confId=130706.